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THIRD
EDITION

SCR MANUAL

SILICON CONTROLLED RECTIFIER MANUAL

Including The Light Activated SCR
And Gate Turn-Off Switch

Theory / *Ratings* / *Applications*

THIRD
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SILICON CONTROLLED RECTIFIER MANUAL

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FOREWORD

Here is the Third Edition of the *original* General Electric SCR Manual. Earlier editions have been standard references in the fast-moving SCR field, and have been quoted and referenced countless times throughout the world. The new Third Edition introduces many new SCR types that cover a wide range of current and voltage as well as SCR's with useful specialized characteristics. Chapters on phase control, inverters, and static switches have been completely rewritten to reflect refinements and new circuit developments in these areas and to make this information more generally useful than before. Other chapters from previous editions have been heavily revised with up-dated information, and all incorporate the new terminology being established by standards activities in the semiconductor industry. New chapters cover the exciting new "first cousins" of the SCR: the gate turn-off switch and the light activated SCR. Many readers will also welcome the new chapter on reliability aspects of power semiconductors.

And to help you select some of the other important components needed in SCR circuits, we've listed several of our G-E sister departments that manufacture associated electronic components in Chapter 21.

All told, over half the Third Edition is of previously unpublished and useful application information.

This new edition of the SCR Manual is a continuing part of General Electric's leading role in which the first SCR was developed in 1957 and since brought to today's maturity. It is our hope that you will find this Manual useful and informative.

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An Introduction to the Silicon Controlled Rectifier

The Silicon Controlled Rectifier has come a long way since General Electric introduced it in 1957, and a great deal of the progress has come since the publication of the second edition of the SCR Manual 2½ years ago. If you are already familiar with the SCR and wish guidance in more sophisticated applications, jump ahead into our new SCR Manual and explore some of the intriguing things we've prepared for you. If you have heard of the SCR but would like to start from scratch in learning how it can help you, as indeed all of us were doing just a short time ago, we suggest that you obtain a copy of the General Electric SCR Hobby Manual. The term "Hobby Manual" is somewhat of a misnomer. It is a serious engineering effort with some 20 ingenious circuits of considerable value to all. However it was written by our Application Engineers on the assumption that the reader, although learned in his own field of competence, is new to the SCR and most other semiconductors as well.

The Hobby Manual begins with a straightforward introduction to the world of semiconductors, how to use them, how to troubleshoot circuits. The circuits include AC and DC motor speed controls, lamp dimmers, time delay circuits, and very high gain detector circuits. The Hobby Manual circuits use the G-E Hobby/Experimental line of semiconductors available from G-E electronic device distributors throughout the country. It is thus the simplest way to obtain a basic education on the care and feeding of the SCR, the light activated SCR, sensors such as the magnetic reed switch and cadmium sulphide photo cell, and the unijunction transistor.

A BRIEF DESCRIPTION OF THE SCR

The SCR is a semiconductor—a rectifier—a static latching switch capable of operating in microseconds—and a sensitive amplifier. It isn't an overgrown transistor, since it has far greater power capabilities, both voltage and current, under continuous and surge conditions.

As a *silicon semicondutcor*—the SCR is compact, static, capable of being hermetically sealed, silent in operation and free from the effects of vibration and shock. A properly designed and fabricated SCR has no inherent failure mechanism. When properly chosen and protected, it should have virtually limitless operating life even in harsh atmospheres. Thus countless billions of operations can be expected, even in explosive environments.

As a *rectifier*—the SCR will conduct current in only one direction. But this serves as an advantage when the load requires DC, for here the SCR serves both to control *and* rectify—as in a regulated battery charger.

As a *latching switch*—the SCR is an ON-OFF Switch, unlike the vacuum tube or transistor which are basically variable resistances (even though they too can be used as on-off switches). The SCR can be turned on by a momentary application of control current to the gate (as short a pulse as a fraction of a microsecond will do), while tubes or transistors (and the basic relay) require a continuous ON signal. In short the SCR *latches* into conduction, providing an inherent memory useful for many functions. The SCR can be turned ON in 1 to 4 microseconds, and OFF in 10 to 20 microseconds; further improvements in switching speed are being made all along.

Just as a switch or relay contact is commonly rated in terms of the current it can safely carry and interrupt, as well as the voltage at which it is capable of operating, the SCR is rated in terms of peak voltage and forward current. General Electric offers a complete family of SCR's with current carrying capacities from ½ amp to 470 amps RMS, and up to 1100 volts at this writing. (See Frontispiece.) Higher voltage and current loads are readily handled by series and parallel connection of SCR's.

As an *amplifier*—the smallest General Electric SCR's can be latched into conduction with control signals of only a few microwatts and a few microseconds duration. These SCR's are capable of switching up to 400 watts. The resulting control power gain of approximately 100 million makes the small SCR one of the most sensitive control devices available. With a low cost unijunction transistor firing circuit driving the larger SCR's (Chapter 4), stable turn-on control power gains of many billions are completely practical.

This extraordinary control gain makes possible inexpensive control circuits using very low level signals, such as produced by Thermistors, cadmium sulfide light sensitive resistors, and other transducers.

One of the most impressive features of the SCR is the *new low cost* of most of the circuits you'll find in the Manual.

In many applications, the SCR circuit will provide greater reliability at lower cost than conventional controls which utilize:

Thyratrons . . . Relays . . . Magnetic Amplifiers and Saturable Reactors . . . Contactors . . . Variable Autotransformers . . . Fuses . . . Timers . . . Rheostats . . . Vacuum Tubes . . . Power Transistors

Welcome to the exciting world of the new SCR circuits and applications. Please bear in mind that the material in this Manual is intended only as a respectful guide to circuit approaches. Our years of experience in offering application help shows that, given some basic starting points like those in this Manual, you the circuit designer inevitably come up with the best approach for your specific problems.

Please remember these two convenient starting points:

—The new SCR Hobby Manual as a review of some basic concepts.

—The SCR Application Index as a road map to the circuits that will prove most useful to you (see page 402).

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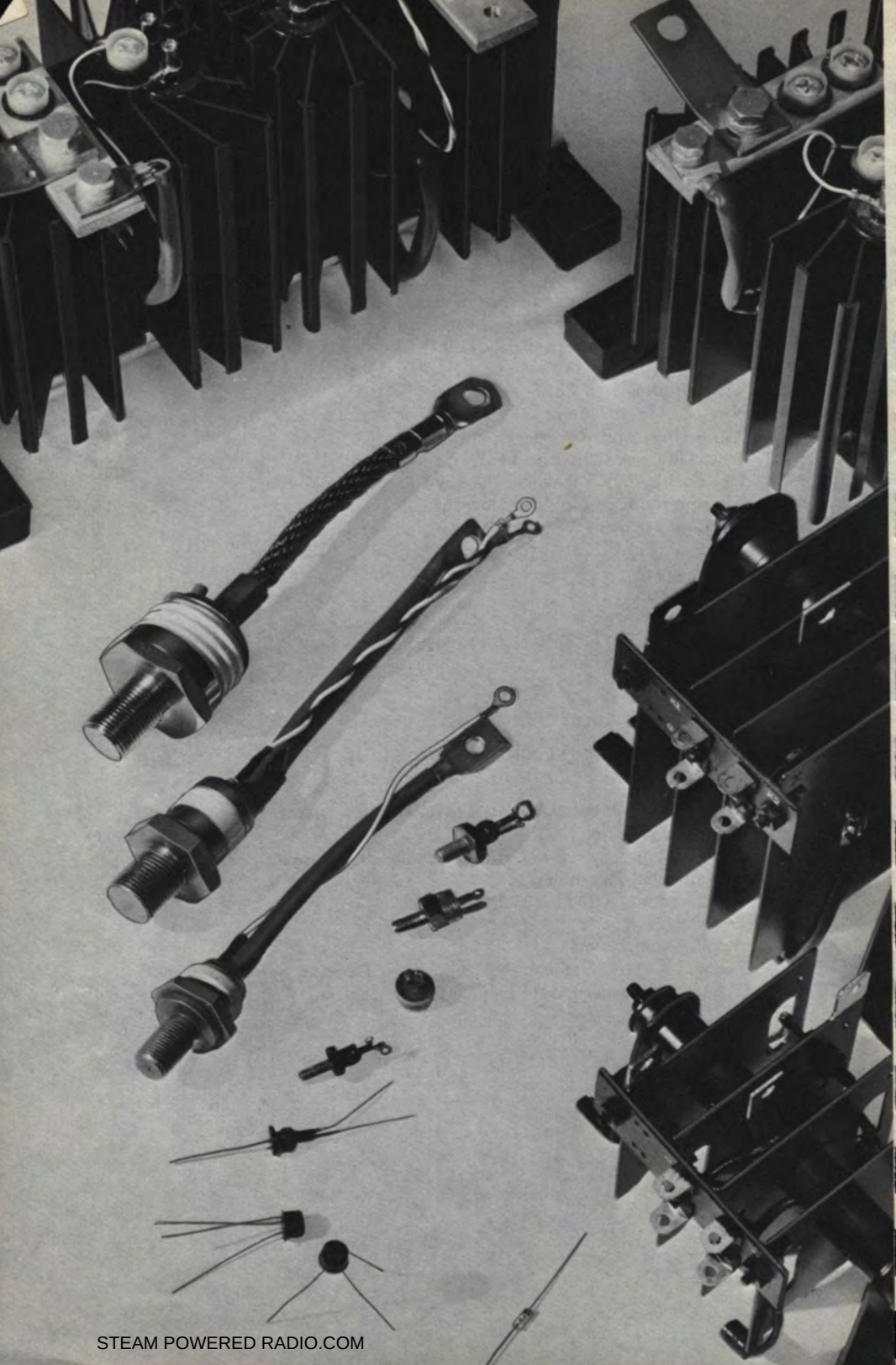


Construction and Basic Theory of Operation

1.1 INTRODUCTION

The silicon controlled rectifier (SCR) is a p-n-p-n semiconductor switch, whose bistable action depends on regenerative internal feedback. Other members of the p-n-p-n family include the silicon controlled switch (SCS), gate turn-off switch (GTO), light activated silicon controlled rectifier (LASCR), and four layer (Shockley) diode.

1.2 CLASSIFICATION OF p-n-p-n DEVICES

The heart of a p-n-p-n device is its four-layered "pellet" of alternate p- and n-type semiconductor. This semiconductor is almost always silicon, although germanium has been used. Devices with the two endmost layers only connected to external terminals (anode, cathode) are called four layer diodes, those with three layers accessible (anode, cathode, p-gate) are called SCR's or GTO's, while the SCS has all four layers externally available (anode, cathode, p-gate, n-gate).*

1.3 SCR CONSTRUCTION

The successful and reliable operation of an SCR is predicated on its proper design and construction. The actual fabrication methods chosen for a particular SCR type depend a great deal on the service expected from that SCR. A seventy ampere SCR destined for use in a harsh military environment may differ radically in design from a seven ampere device intended for the light industrial market.

Device fabrication starts with the preparation of the silicon pellet. First, p-type impurities are gaseously diffused into thin discs of n-doped silicon to form large-area p-n-p wafers. Where many finished pellets can be economically derived from a single wafer, as in the manufacture of small, low current SCR's, a second diffusion step is generally used to complete the p-n-p-n structure. Each wafer is selectively masked by an oxidation/etching process (see Figure 1.1), and subsequently re-diffused with n-type impurities.

Figure 1.1 Diffused SCR Manufacture

* Three terminal devices with anode, cathode and n-gate only brought out externally are usually referred to as "complementary" SCR's or GTO's.

The p-n-p-n wafers so formed are then diced up into finished pellets. In the manufacture of higher-current SCR's, where only a limited number of pellets (sometimes only one) can be obtained from each wafer, it is often more convenient to pelletize the original p-n-p wafers *before* adding the final n-region. Where this is the case, precision alloying techniques are used to fuse a gold-antimony preform into each p-n-p pellet, thus forming the required p-n-p-n structures. Figure 1.2 shows an alloy-diffused SCR pellet.

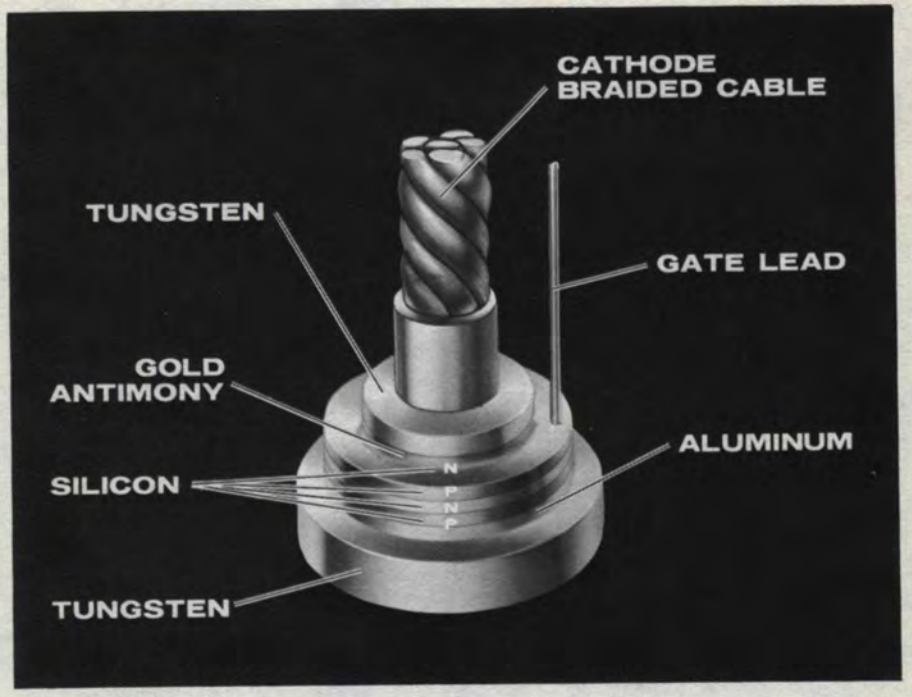


Figure 1.2 Alloy-Diffused SCR Pellet

In order to protect the fragile silicon junctions against thermal and mechanical stresses, the silicon pellet is usually brazed between substantial plates of molybdenum or tungsten, materials which have a similar coefficient of expansion to silicon. In small, lead-mounted SCR's, a bottom back-up plate only is used, and this plate doubles as part of the device encapsulation. In the larger SCR's, particularly

those designed for operation between wide temperature extremes or where severe thermal cycling is expected, the bottom plate is *hard-soldered* to a copper stud. The copper stud serves as anode terminal, base for the device housing, and thermal path for conducting the SCR heat losses to the ambient. For this latter reason the stud is usually threaded or bolted to a heatsink. Use of hard solder with this type of construction minimizes the possibility of thermal fatigue destroying the joint between copper and back-up plate when the SCR is subjected to the temperature induced stresses of wide and frequent thermal cycling. Hard solder is used for the joint between cathode-plate and cathode terminal for the same reason. Figure 1.3 shows a section through a typical thermal-fatigue-free, high current SCR.

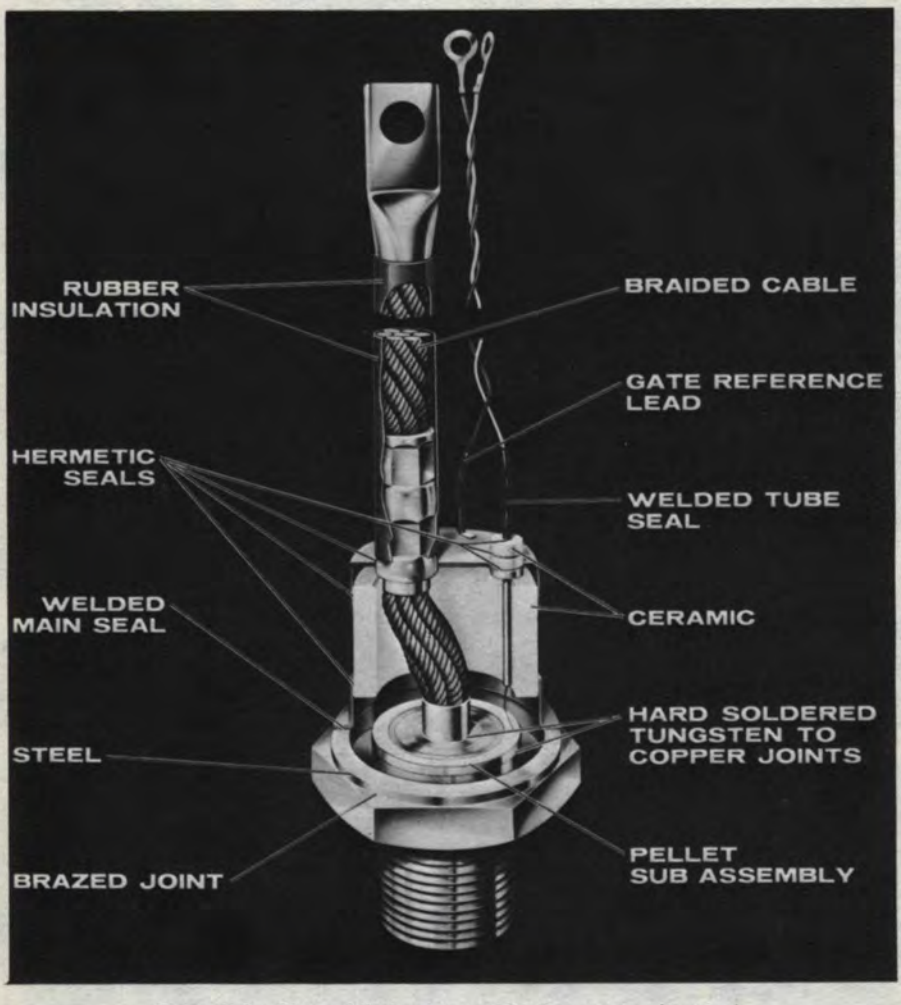


Figure 1.3 Thermal Fatigue Free SCR Construction (Section)

When an SCR is designed specifically for use in the light industrial and consumer markets, environments characterized by limited temperature excursions and absence of wide range cyclical loading, the premium-type structure described

above is not required. Here, the silicon pellet is mounted *directly* onto the copper stud, or case, with a special tin-lead solder alloy. The solder joint then absorbs the stresses set up by differential expansion between silicon and copper. *Providing these stresses are not too great*, this "soft solder" construction is satisfactorily thermal fatigue free. In addition to making possible a lower-cost device, the method allows better heat transfer from silicon to copper, which reduces cell heatsinking requirements.

The entire SCR assembly is fabricated in a super-clean environment to assure long term stability of the SCR's electrical characteristics. To maintain the stability of these characteristics throughout the long life of the SCR, the finished assembly is sealed off from the outside atmosphere by welded hermetic seals. Electrical connections are also made by welding. Extensive electrical and mechanical tests at room temperature and both extremes of the operating temperature range assure that the individual SCR's meet their specification sheet ratings and characteristics. Cycled life tests on significant samples continuously monitor and control the long-term reliability of SCR's coming off the production line.

1.3.1 SCS Construction

The SCS is essentially a low current low voltage n-p-n diffused base transistor with a third junction added to form a p-n-p-n device. For further details on the design and construction of this device see 7th Edition Transistor Manual available from General Electric Semiconductor Products Department, Electronics Park, Syracuse, N. Y.

1.3.2 LASCR Construction

The light activated SCR (LASCR) consists of an all-diffused silicon p-n-p-n pellet mounted in a hermetically sealed TO-5 transistor package provided with a translucent "window" in its encapsulation as shown in Figure 1.4.

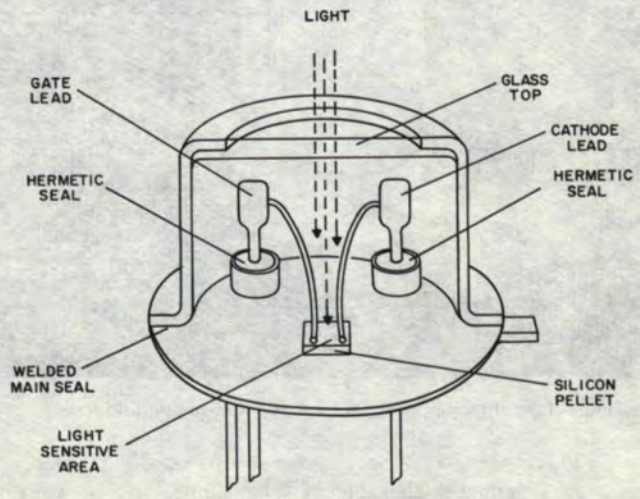


Figure 1.4 LASCR Construction Details

1.4 TWO TRANSISTOR ANALOGY OF p-n-p-n OPERATION

A p-n-p-n structure is best visualized as consisting of two transistors, a p-n-p and an n-p-n interconnected to form a regenerative feedback pair as shown in Figure 1.5. Current gain around the internal feedback loop $G = h_{FE1} \times h_{FE2}$, where h_{FE1} and h_{FE2} are the common emitter current gains of the indivudual transistor sections. If I_{CO1} is the collector to base leakage current of the n-p-n, and I_{CO2} is the leakage of the p-n-p, then:

For the p-n-p section: $I_{C1} = h_{FE1}\ (I_{C2} + I_{CO1}) + I_{CO1}$

For the n-p-n section: $I_{C2} = h_{FE2}\ (I_{C1} + I_{CO2}) + I_{CO2}$ and total anode-to-cathode current $I_A = (I_{C1} + I_{C2})$.

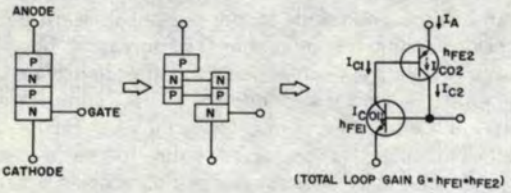


Figure 1.5 Two Transistor Analogue of SCR

Solving these three equations for I_A gives

$$I_A = \frac{(1+h_{FE1})\ (1+h_{FE2})\ (I_{CO1}+I_{CO2})}{1-h_{FE1} \cdot h_{FE2}} \qquad 1.1$$

With proper bias applied (*positive* anode to cathode voltage), h_{FE1} and h_{FE2} are both low, and G is much less than unity. The denominator of Equation 1.1 approaches one, and I_A is little higher than the sum of the individual transistor leakage currents. Under these conditions the p-n-p-n structure is said to be in its *forward blocking* or high impedance "off" state. The switch to the low impedance "on" state is initiated simply by raising the loop gain G to unity. Inspection of Equation 1.1 shows that as $h_{FE1} \cdot h_{FE2} \rightarrow 1$, $I_A \rightarrow \infty$. Physically, as the loop gain approaches one and the circuit starts to regenerate, each transistor drives its mate into saturation. Once in saturation, all junctions assume a forward bias, and total potential drop across the device approximates that of a single p-n junction. Anode current is limited only by the external circuit.

The p-n-p-n structure may also be analysed in terms of its component transistor "alphas." The p-n-p section has an α_1 which defines the fraction of hole current injected at its emitter that reaches its collector (Figure 1.6).

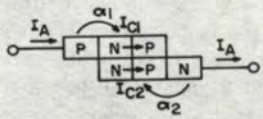


Figure 1.6 "Alpha" Analysis of SCR Operation

$$I_{C1} = \alpha_1 I_A$$

The n-p-n section similarly has an α_2 which defines the fraction of electron current injected at its emitter that reaches its collector.

$$I_{C2} = \alpha_2 I_A$$

Total anode current must equal the sum of these two components *plus* a leakage term:

$$I_A = \alpha_1 I_A + \alpha_2 I_A + I_{CX}$$

where I_{CX} is the leakage current of the center junction. Rearranging and solving for I_A gives

$$I_A = \frac{I_{CX}}{1 - (\alpha_1 + \alpha_2)} \qquad 1.2$$

Equation 1:2 is the "alpha" equivalent of Equation 1:1 When $(\alpha_1 + \alpha_2) << 1$ $I_A \rightarrow I_{CX}$ and this corresponds to the p-n-p-n forward blocking state. When $(\alpha_1 + \alpha_2) \rightarrow 1$, $I_A \rightarrow \infty$, and this corresponds to the p-n-p-n forward conduction state.

There are several mechanisms available for increasing h_{FE} in a transistor, so that in the p-n-p-n structure $h_{FE1} \cdot h_{FE2} \rightarrow 1$, and the device may be switched on. All make use of the emitter-current dependence of h_{FE}. In most silicon transistors, h_{FE} is quite low at low emitter currents, but increases fairly rapidly as emitter current is increased. This effect (Figure 1.7) is due to the presence in the silicon of special impurity centers. Any mechanism which causes a temporary increase in transistor emitter current is therefore potentially capable of turning on a p-n-p-n device. The most important of these mechanisms are:

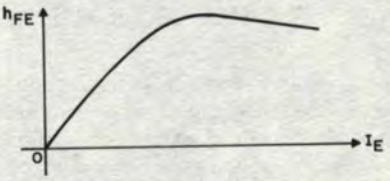


Figure 1.7 Emitter-Current Dependence of h_{fe} In A Silicon Transistor

1. Voltage. As the collector-to-emitter voltage of a transistor is increased, eventually a point is reached where the energy of the (leakage) current carriers arriving at the collector junction is sufficient to dislodge additional carriers. These carriers in turn dislodge more carriers, and the whole junction goes into a form of avalanche breakdown characterized by a sharp increase in collector current. In a p-n-p-n device, when the avalanche current makes $G \rightarrow 1$, switching takes place. This is the turn-on mechanism normally employed to switch four layer diodes into conduction.

2. Rate of change of voltage. Any p-n junction has capacitance—the larger the junction area, the larger the capacitance. If a step function of voltage is impressed suddenly across the anode-to-cathode terminals of a p-n-p-n device, a charging current i will flow from anode to cathode to charge the device capacitance:

$$i = C\, dv/dt$$

When i equals the value necessary for $G \rightarrow 1$, the device will switch on. This phenomenon is known as the "dv/dt effect."

3. Temperature. At high temperatures, leakage current in a silicon p-n junction doubles approximately with every 8°C increase in junction temperature.

When the temperature generated leakage current in a p-n-p-n structure has risen sufficiently for G→1, switching occurs.

4. Transistor Action. Collector current is increased in conventional transistor manner by temporarily injecting additional ("gate") current carriers into one of the transistor base regions. This is the mechanism normally employed to turn-on SCR's, SCS', GTO's, and other p-n-p-n devices which have an external connection ("gate" lead) to one or more of the transistor bases.

5. Radiant energy ("light"). Incident radiant energy within the spectral bandwidth of silicon (Figure 11.4) impinging on and penetrating into the silicon lattice releases considerable numbers of hole-electron pairs. When the resultant device leakage current climbs above the critical level for G→1, triggering will ensue. This triggering mechanism makes possible the light activated SCR. In these devices a translucent "window" is provided in the device encapsulation in order that "light" may reach the silicon pellet. The LASCR, because it is provided with a gate lead, may be triggered either by light or by electrical gate current.

1.5 V-I CHARACTERISTICS OF p-n-p-n DEVICES

Figure 1.8 illustrates the V-I characteristics of a typical gate-controlled p-n-p-n device. In the forward blocking region, increasing the forward voltage does not tend to increase leakage current until the point is reached where avalanche multiplication begins to take place. Past this point, the leakage current increases quite rapidly until the total current through the device is sufficient to raise the internal loop gain ≥ 1. At this point the device will go into the high conduction region, provided that anode current remains in excess of a minimum value called the *holding current*. When anode current drops below the holding current, the p-n-p-n device reverts to its forward blocking state. In the reverse direction the p-n-p-n structure looks like two reverse-biased p-n junctions in series, so that it exhibits characteristics very similar to an ordinary back-biased silicon rectifier. For most commercially available devices (SCR, SCS, LASCR, four layer diode), the peak *reverse* voltage capability is designed to be at least equal in magnitude to the minimum forward breakover voltage. Some GTO's however, have a lower voltage capability in the reverse direction than in the forward direction.

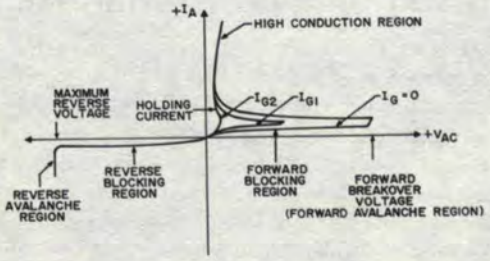


Figure 1.8 V-I Characteristics of a PNPN Device

For increasing magnitudes of gate current, the region of characteristics between breakover current and holding current (Figure 1.8) is narrowed and the forward breakover voltage is reduced. For sufficiently high gate currents, the entire forward blocking region is removed, and the V-I characteristics of a p-n-p-n device are essentially identical to those of a p-n rectifier.

In typical operation the gate-controlled p-n-p-n device is biased well below its minimum forward breakover voltage, and triggering is accomplished by injecting current into the gate lead. ("Light" is of course used in place of gate current to trigger the LASCR.) This is a very advantageous mode of operation, since it is possible to use a device with a forward breakover voltage much higher than any voltage likely to be encountered in the circuit, and to use only a moderate amount of trigger power to start the high conduction state. Circuit design and reliability are thus greatly enhanced. Once the gate has been used to trigger an SCR or SCS into conduction it loses control, and the only method of turning either of these devices off is to reduce anode current below the holding current level. *(This applies to LASCR likewise, once it has been triggered.) Typically a ten to fifty microsecond gate pulse will initiate conduction in a gate-controlled p-n-p-n switch.

As already mentioned, leakage current through a p-n-p-n device increases with temperature. The forward breakover voltage therefore tends to be quite temperature sensitive. At a high enough temperature (well above its maximum *rated* temperature) the p-n-p-n device loses completely its ability to block forward voltage and assumes characteristics just like a p-n diode.

In smaller SCR's, SCS', LASCR's, or GTO's this temperature effect on the breakover voltage can be minimized by extracting the forward leakage current from the gate. This prevents current from passing through the emitter of the n-p-n section of the device and maintains a low alpha in this section. It is also possible to actually increase the forward breakover voltage point on some small SCR's by this means. The effect of negative gate current on the forward blocking characteristics, however, becomes negligible on higher current SCR's due to the ineffectiveness of the gate in removing leakage current from the entire broad area of the n-p-n base region.

As might be expected, the gate cathode V-I characteristics of a gate-operated p-n-p-n device are essentially those of a p-n junction diode. Since the increase in h_{FE} with current is utilized, these devices are *current triggered* as opposed to voltage triggered, like a gas thyratron. This distinction must be kept in mind when designing triggering circuits, in that a relatively low impedance voltage source, or a current source is required.

1.6 SCR (& LASCR) TURN-OFF MECHANISM

When the SCR is in the conducting state, each of the three junctions of Figure 1.9 are in a condition of forward bias and the two base regions (B_P, B_N) are heavily saturated with holes and electrons (stored charge).

To turn-off the SCR in a minimum time, it is necessary to apply a reverse voltage. When this reverse voltage is applied the holes and electrons in the vicinity of the two end junctions (J_1, J_3) will diffuse to these junctions and result in a reverse current in the external circuit. The voltage across the SCR will remain at about +0.7 volts as long as an appreciable reverse current flows. After the holes and electrons in the vicinity of J_1 and J_3 have been removed, the reverse current will cease and the junctions J_1 and J_3 will assume a blocking state. The reverse voltage across the SCR will then increase to a value determined by the external circuit. Recovery of the SCR is not complete, however, since a high concentration of holes and electrons still exists in the vicinity of the center junction (J_2).

* The gate turn-off switch (GTO), as its name suggests, can be turned off by means of its gate terminal. See Section 1.7.

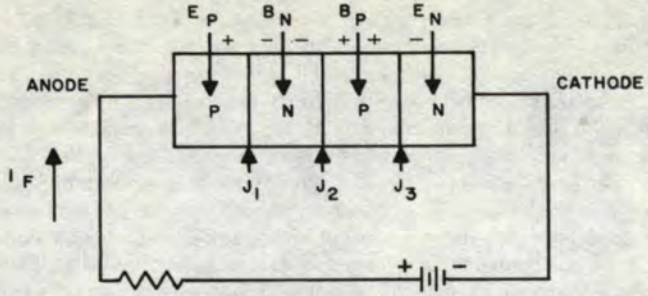


Figure 1.9 Silicon Controlled Rectifier Biased in Conducting State (Gate Open Circuited)

This concentration decreases by the process of recombination in a manner which is largely independent of the external bias conditions. After the hole and electron concentration at J_2 has decreased to a low value, J_2 will regain its blocking state and a forward voltage (less than V_{BO}) may be applied to the SCR without causing it to turn-on. The time that elapses after the cessation of forward current flow and before forward voltage may safely be reapplied is called the SCR "turn-off time," t_o, and is usually in the order of 10-15 microseconds long.

1.7 GATE TURN-OFF SWITCH

The gate turn-off switch is a four layer p-n-p-n similar in construction to the SCR. Like the SCR, the GTO is triggered into conduction by raising its loop gain to unity. In the simple two transistor p-n-p-n analogue of Figure 1.5, with the device switched on, assume that h_{FE1} equals h_{FE2} so that equal currents flow in each transistor section. If the p-n-p transistor's collector current were diverted away from the n-p-n transistor's base region and out of the gate lead, the n-p-n transistor would cut-off, $h_{FE1} \times h_{FE2}$ would drop below unity, and the p-n-p-n device would revert to its forward blocking state. Turn-off gain, defined as the ratio of anode current flowing prior to turn-off to negative gate current required to effect turn-off, in this case would be at least two (2). Practically, SCR turn-off in this fashion is prevented by the inability of its small ohmic gate contact to extract the necessary (substantial) negative gate current from the *whole* of the p-type gate region. In the gate turn-off switch however, this situation is alleviated by increasing the active gate contact area, and by reducing the gate current required for turn-off. Referring again to Figure 1.5 if h_{FE2} is made much less than unity when the device is in its "on" state, and h_{FE1} is made greater than unity to maintain $h_{FE} \cdot h_{FE1} = 1$, only a small percentage of the total anode current will flow in the collector of the p-n-p transistor. It is this current that is withdrawn to turn the GTO "off." For a typical device, gains from 5 to 25 are realizeable depending on current, temperature gate pulse duration and other variables. Gate turn-off switches can be turned off like conventional SCR's, if so desired.

1.8 COMPARISON OF SCR WITH OTHER SEMICONDUCTORS

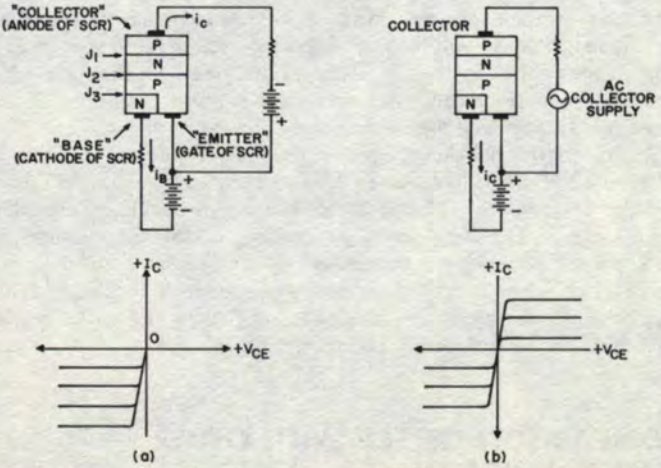
It will be noted that the low current h_{FE} of the p-n-p and n-p-n parts of the SCR must be low in order to have the device block in the forward direction. In

an ordinary three layer silicon power transistor, it is desirable to have h_{FE} as high as possible in order to achieve a high current gain. Unfortunately, however, high h_{FE} is obtained in most silicon transistors by using very thin base regions, and a thin base between two low resistivity regions is incompatible with high voltage. The wide base regions in the SCR, necessary to achieve low h_{FE} are compatible with high voltages so that the SCR is inherently a higher voltage device. The use of wide base regions is also an advantage from the standpoint of ease of manufacture and reproducibility of characteristics. An advantage of the SCR over power transistors is the amount of drive necessary to full conduction. In many silicon power transistors, it is necessary to inject up to half an ampere of continuous base current in order to conduct 5 amperes from collector to emitter. In an SCR, the amount of current conducted is dependent only on the external circuit once the device has been triggered. Thus a trigger current of 50 ma applied for only a few microseconds is all that is necessary to allow conduction of any current from a few milliamperes to hundreds of amperes. The high current capabilities of the SCR, as contrasted to a transistor, are due to more effective use of junction area for current conduction.

When compared to SCR's of equivalent current rating in DC applications, the GTO permits greatly simplified commutating (turn-off) circuitry and is able to operate at much higher frequencies due to its inherently faster turn-off mechanism. In the GTO, stored charge in the vicinity of the center junction is "cleaned out" rapidly by the action of the turn-off gate signal. In general, however, the GTO will have a higher forward voltage drop, higher holding current, and require more gate trigger current than its SCR counterpart. The GTO does retain the high voltage capabilities of the SCR.

1.9 p-n-p-n DEVICE USED AS REMOTE BASE TRANSISTOR

As already described, a p-n-p-n structure may be visualized as consisting of two interconnected transistors. When the structure is conventionally biased, i.e.



(a) p-n-p-n Structure Biased as p-n-p Transistor

(b) p-n-p-n Structure Used as Symmetrical Transistor

Figure 1.10 Remote Base Transistor

positive anode to cathode voltage, *positive* gate to cathode voltage, the transistors act as a regenerative pair and give the p-n-p-n device its normal bistable characteristics. A p-n-p-n structure may be biased however, so that the transistors are *unable* to regenerate, and in this case the bistable action is eliminated. The device, when so biased, exhibits the linear characteristics of an amplifier. Referring to Figure 1.11, a negative bias on the base lead with respect to the emitter lead causes electrons to be injected across junction J3 for collection at J2. Upon collection at J2 these electrons furnish base drive for the p-n-p section in much the same way as if a lead were attached directly to it. Hence the name "remote base" transistor. Common-emitter current gains (beta) vary from much less than unity to about five (5), depending on the characteristics of the parent p-n-p-n device. Since in most cases the "inverse beta"* is approximately equal to the forward beta, the devices are also usable as symmetrical AC amplifiers or switches (Figure 1:10).

REFERENCES

1. Moll, et al "PNPN Transistor Switches," Proceedings IRE, Vol. 44, September 1956, p 1174-1182.

2. Aldrich, Holonyak, "Multi-Terminal PNPN Switches," Proceedings IRE, Vol. 46, June 1958, p 1236-1239.

3. Gentry, Gutzwiller, Holonyak and Von Zastrow, "Semiconductor Controlled Rectifiers . . . Principles and Application of p-n-p-n Devices," book to be published 1964 (Prentice-Hall).

* Beta with collector used as the emitter and vice versa.

2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

Figure 2.1 shows graphical symbols of the types of semiconductors discussed and employed in the circuits of this Manual. Since popular and historical usage in some cases deviates from ASA Standard Y32.2-1962, both the popular and the

NAME OF DEVICE	ASA STANDARD Y32. 2 - 1962	POPULAR USAGE AS USED IN THIS MANUAL
RECTIFIER DIODE		
ZENER OR BREAKDOWN DIODE		
SEMICONDUCTOR (SILICON) CONTROLLED RECTIFIER (SCR)		
GATE TURN-OFF SWITCH (GTO) (PNPN - TYPE)		
NPN TRANSISTOR		
UNIJUNCTION TRANSISTOR		
PNP TRANSISTOR		
SILICON CONTROLLED SWITCH (SCS)		
LIGHT ACTIVATED DIODE SWITCH (LAS) (PNPN TYPE)		
LIGHT ACTIVATED TRIODE SWITCH (LASCR) (PNPN TYPE)		

A = ANODE
B = BASE
E = EMITTER
G = GATE

G_A = GATE ON N REGION
G_C = GATE ON P REGION
K = CATHODE

Figure 2.1 Semiconductor Graphical Symbols

standard symbols are shown where this is the case. For convenience and to differentiate between various types of semiconductors for which the Standard does not recommend different symbols, this Manual employs the "popular usage" symbols throughout.

2.2 SCR TERMINOLOGY

The following tabulation defines the terminology used in SCR specifications. The new symbols are from the proposed IEEE Standards on Solid State Devices (4/16/63) wherever applicable and are used throughout this Manual. The previously used symbol is listed for reference purposes. Other symbols used in this Manual are defined in the section in which they are used.

2.2.1 SCR Ratings

Ratings are limiting values assigned by the manufacturer, which, if exceeded, may result in malfunction of the device or permanent impairment of device performance or life.

Terminology	New Symbol	Old Symbol	Definition
Repetitive Peak Reverse Voltage or Working Peak Reverse Voltage, gate open	V_{ROM}(rep)	PRV	Maximum allowable instantaneous value of repetitive reverse (negative) voltage that may be applied to the SCR anode terminal with gate terminal open. While this value of voltage does not necessarily represent a "breakdown" voltage, it should never be exceeded except by the transient rating if the device has such a rating. General Electric SCR's are capable of handling this voltage satisfactorily with negative gate voltage also.
Non-Repetitive Peak Reverse Voltage, gate open	V_{ROM}(non-rep)	PRV_{trans}	Maximum allowable instantaneous value of reverse (negative) voltage including all non-repetitive transient voltages, but excluding all repetitive transient voltages, that may be applied to the SCR anode terminal with gate terminal open. General Electric SCR's are capable of handling this voltage satisfactorily with negative gate voltage also.
Peak Forward Blocking Voltage, gate open	V_{FOM}		Maximum instantaneous value of forward blocking voltage (anode terminal positive) including transient voltages permitted by the manufacturer under stated conditions and which will not switch the SCR to the on-state.

Terminology	New Symbol	Old Symbol	Definition
Peak Forward Voltage	PFV	PFV	Maximum instantaneous value of forward voltage permitted by the manufacturer under stated conditions and which may cause the SCR to switch to the on-state. If anode breakover occurs at a voltage lower than the PFV, no damage to the SCR will occur.
Average Forward Current, On-State	$I_{F(AV}$		Maximum continuous DC current which may be permitted to flow in the forward direction (from anode to cathode) under stated conditions of frequency, temperature, reverse voltage, and current waveform.
	I_O	I_F	$I_{F(AV)}$ under specific condition of half-wave rectified sine-wave current, 180° conduction angle.
RMS Forward Current, On-State	I_f	I_{RMS}	Maximum continuous RMS current which may be allowed to flow in the forward direction under stated conditions. "Average forward current" rating above applies simultaneously.
Peak One-Cycle Surge Foward Current	I_{FM}(surge)	I_{surge}	Maximum allowable non-recurrent peak current of a single forward cycle (8.3 milliseconds duration) in a 60-cps single-phase resistive load system. The surge may be preceded and followed by maximum rated voltage, current, and junction temperature conditions, and maximum allowable gate power may be concurrently dissipated. However, specified limitations on anode current during switching should not be exceeded.
I squared t	I^2t	I^2t	This is a measure of maximum forward non-recurring (100–500 times in life of SCR) overcurrent capability for very short pulse durations (8.3 milliseconds or less, unless otherwise specified). I is in RMS amperes, and t is pulse duration in seconds. The same conditions as listed above for I_{FM}(surge) apply.

Terminology	New Symbol	Old Symbol	Definition
Peak Reverse Gate Voltage	V_{GRM}	$V_{G(Reverse)}$	Maximum allowable peak voltage between the gate terminal and the cathode terminal when the junction between the gate region and the adjacent cathode region is reverse biased.
Peak Gate Power Dissipation	P_{GM}	P_G	Maximum instantaneous value of gate power dissipation permitted between gate and cathode terminals.
Average Gate Power Dissipation	$P_{G(AV)}$	P_G	Maximum value of gate power dissipation averaged over a full cycle permitted between gate and cathode terminals.

2.2.2. SCR Characteristics

Characteristics are measurable properties or attributes of a device which are inherent to its design.

Forward Break-over Voltage	$V_{(BR)F*}$	V_{BO}	Maximum positive voltage on the anode terminal with respect to the cathode terminal for which the small-signal resistance is zero with stated gate termination. This is also the voltage at which an SCR switches into the conductive state.
Instantaneous Forward Current, On-State	i_F	i_F	Instantaneous value of anode current flowing into the SCR in the conducting state.
Instantaneous On-Voltage (Forward Voltage Drop)	v_F	v_F	Instantaneous voltage drop between anode and cathode terminals during conduction of current from anode to cathode terminals while the device is in the on-state.
Full Cycle Average On-Voltage (Forward Voltage Drop)	$V_{F(AV)}$	$V_{F\ Avg}$	On-voltage averaged over one complete cycle with stated forward current flowing in a 60 cps single phase half wave rectifier with resistive load and no firing angle delay.
Instantaneous Forward Gate Current	i_{GF}	i_G	Instantaneous current flowing between gate and cathode terminals in a direction to forward bias the gate junction.

Terminology	New Symbol	Old Symbol	Definition
Instantaneous Forward Gate Voltage	v_{GF}	v_G	Instantaneous forward voltage between gate and cathode terminals with anode terminal open.
DC Gate Trigger Current	I_{GT}	I_{GF}	Forward gate current required to trigger an SCR with anode terminal at +6 volts with respect to cathode terminal and with SCR at stated temperature conditions.
DC Gate Trigger Voltage	V_{GT}	V_{GF}	Gate voltage with I_{GT} flowing but prior to start of anode conduction.
Effective Irradiance to Trigger	H_{ET}	—	The amount of incident radiant flux density which is effective in causing a light activated device to switch to the conducting state. This is the integral of the product of the spectral response curve of the cell and the spectral distribution of the energy source, expressed in watts per square centimeter, which causes the device to switch.
Holding Current	I_H	I_H	Value of i_F below which SCR returns to forward blocking state after having been in forward conduction under stated temperature and gate termination conditions.
Instantaneous Forward Blocking Current	I_{F*}	i_s	Instantaneous anode current at stated conditions of forward blocking voltage, junction temperature, and gate termination.
Instantaneous Reverse Blocking Current	i_{R*}	i_R	Instantaneous anode current at stated conditions of negative anode voltage, junction temperature, and gate termination.
Delay Time	t_d	t_d	Time interval between the time the gate current pulse reaches 10% of its final value and the time when the resulting forward current reaches 10% of its maximum value during switching from the off-state to the on-state into a resistive load under stated conditions.

Terminology	New Symbol	Old Symbol	Definition
Rise Time	t_r	t_r	Time interval between the time the forward current reaches 10% of its maximum value and the time the forward current reaches 90% of its maximum value during switching from the off-state to the on-state into a resistive load under stated conditions.
Turn-On Time	t_{on}	t_{on}	Sum of delay time and rise time.
Turn-Off Time	t_{off}	t_o	Time interval required for gate to regain control of forward blocking characteristic after forward conduction under stated circuit and temperature conditions.
Thermal Resistance	θ	R_T	Temperature rise per unit power dissipation of a designated junction above the temperature of a stated external reference point under conditions of thermal equilibrium. For stud mounted devices, Θ is expressed in °C/watt between junction and the center of one flat side of the hex. (See Chapter 16)
Transient Thermal Impedance	$\theta_{(t)}$	r_T	Temperature rise per unit power dissipation of junction above stated reference point for specified period of time after application of step increase of junction power dissipation with device case or ambient temperature held constant.
Junction Temperature	T_J	T_J	Junction temperature.
Case Temperature	T_C	T_C	Case Temperature.
Ambient Temperature	T_A	T_A	Ambient temperature.
Storage Temperature	T_{stg}	—	Storage temperature.

NOTE: Symbol to be used where asterisk (*) is shown in above tables:

O = Gate terminal is open-circuited or device has no gate terminal.

S = Gate terminal is short-circuited to the terminal of the adjacent region.

R = Gate terminal is returned to the terminal of the adjacent region through a stated resistance.

V = Gate terminal is biased with respect to the adjacent region at stated voltage.

Ratings and Characteristics Of Silicon Controlled Rectifiers

3.1 JUNCTION TEMPERATURE

The operating junction temperature range of SCR's varies for the individual types. A low temperature limit may be required to limit stress in the silicon crystal to safe values. This type of stress is due to the difference in the thermal coefficients of expansion of the materials used in fabricating the cell subassembly. The upper operating temperature limit is imposed because of the temperature dependence of $V_{(BR)F}$, the forward breakover voltage, and because of thermal stability considerations. The upper storage temperature limit in some cases may be higher than the operating limit. It is selected to achieve optimum reliability and stability of characteristics with time.

Methods for determining the load current carrying limits of SCR's limit the peak temperature reached by the junction to a value not exceeding the maximum operating temperature. (Exception is taken for non-recurrent phenomena of very short duration, such as fault currents during an accidental short circuit.) The rating methods for continuous and recurrent loads assume uniform temperature across the entire semiconductor junction area. Since there are three junctions in an SCR, a composite temperature as indicated by the variation in anode to cathode forward voltage drop with temperature is used as a means of defining junction temperature.

3.2 POWER LOSSES

Heat is generated in the junction region by electrical losses that may be classified into five types:

a. Forward voltage drop during load current conduction.
b. Forward leakage current during forward blocking.
c. Reverse leakage current during reverse blocking.
d. Losses in the gate circuit due to triggering signal.
e. Losses occurring during switching.

Forward conduction losses are the major source of junction heating for normal duty cycles and power frequencies. Figure 3.1 gives forward conduction loss in average watts for the C35 (2N681 Series) SCR as a function of average current in amperes for various conduction angles. This type of information is given on the specification sheet for each type of SCR. These curves are based on a current waveform which is the remainder of a half-sine wave which results when delayed angle triggering is used in a single phase resistive load circuit. They are conservative for rectangular current waveforms with the same average value and conduction angle. These power curves are the integrated product of the instantaneous anode current and forward voltage drop. This integration can be performed graphically or analytically for conduction angles other than those listed, using the forward voltage-current characteristic curves for the specific device.

Both the forward and reverse blocking losses are determined by integration of the appropriate blocking E-I curves on the specification sheet.

Gate losses are negligible for pulse types of triggering signals. Losses may become more significant for gate signals with a high duty cycle, or for SCR's in a TO-5 or smaller package.

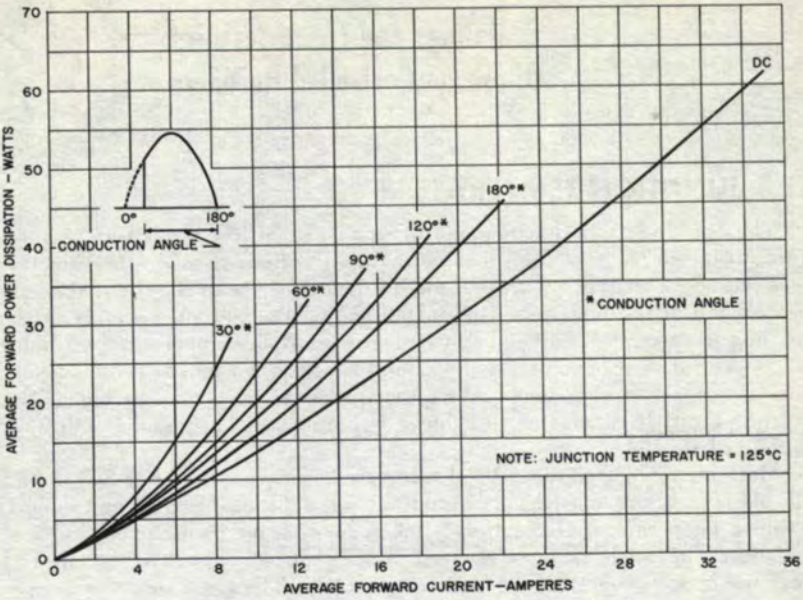


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Figure 3.1 Average Forward Power Dissipation For C35 Series SCR

The losses may be calculated from the gate E-I curves shown on the Triggering Characteristics for the specific type of SCR. Highest gate dissipation will occur for an SCR whose gate characteristics intersect the gate circuit load line at its midpoint. For a more detailed discussion of the gate characteristic and its load line, see Chapter 4.

Turn-on switching ratings are discussed in Section 3.7. Turn-off is discussed in Chapter 5.

3.3 THERMAL RESISTANCE

The heat developed at the junctions by the foregoing power losses flows into the stud and thence to the heatsink. The junction temperature rises above the stud, or case, temperature in direct proportion to the amount of heat flowing from the junction and the thermal resistance of the device to the flow of heat. The following equation defines the relationship under steady-state conditions:

$$T_J - T_C = P\theta \qquad (3.1)$$

where T_J = average junction temperature, °C
T_C = case temperature, °C
P = average heat generation at junction, watts
θ = steady-state thermal resistance between junctions and bottom face of hex or case, °C/watt

Equation 3.1 can be used to determine the allowable power dissipation and thus the continuous pure DC forward current rating of an SCR for a given case temperature through use of the forward E-I curves. For this purpose, T_J is the maximum allowable junction temperature for the specific device. The maximum values of θ and T_J are given in the specifications.

3.4 TRANSIENT THERMAL IMPEDANCE

Equation 3.1 is not satisfactory for finding the peak junction temperature when the heat is applied in pulses such as the recurrent conduction periods in an AC circuit. Solution of Equation 3.1 using the peak value of P is over-conservative in limiting the junction temperature rise. On the other hand, using the average value of P over a full cycle will underestimate the peak temperature of the junction. The reason for this discrepancy lies in the thermal capacity of the semiconductor, that is, its characteristic of requiring time to heat up, and its ability to store heat.

Compared to other electrical components such as transformers and motors, semiconductors have a relatively low thermal capacity, particularly in the immediate vicinity of the junction. As a result, devices like the SCR heat up very quickly upon application of load, and the temperature of the junction may fluctuate during the course of a cycle of power frequency. Yet, for very short overloads this relatively low thermal capacity may be significant in arresting the rapid rise of junction temperature. In addition, the heatsink to which the semiconductor is attached may have a thermal time constant of many minutes. Both of these effects can be used to good advantage in securing attractive intermittent and pulse ratings sometimes well in excess of the published continuous DC ratings for a device.

The thermal circuit of the SCR can be simplified to that shown in Figure 3.2. This is an equivalent network emanating in one direction from the junctions and with the total heat losses being introduced at the junctions only. This simplification is valid for current amplitudes at which I^2R losses are small in comparison with the junction losses. In Figure 3.2 the ambient is the reference level. If a small stud type device is mounted to an infinite heatsink, the heatsink temperature can be used as a reference. However, with larger devices, the case to heatsink thermal resistance is relatively large compared to the junction-case thermal resistance. In such cases the case or hex temperature should be used as a reference.

When a step pulse of heating power P is introduced at the junctions of the SCR (and of the thermal circuit) as shown in Figure 3.3A, the junction temperature will rise at a rate dependent upon the response of the thermal network. This is represented by the curve T_{heat} in Figure 3.3B. After some sufficiently long time t_1, the junction temperature will stabilize at a point $\Delta T = P\,\theta$ above the ambient (or case) temperature. This is the steady-state value which is given by Equation 3.1. θ is the sum of R_1 through R_n in the equivalent thermal circuit of Figure 3.2.

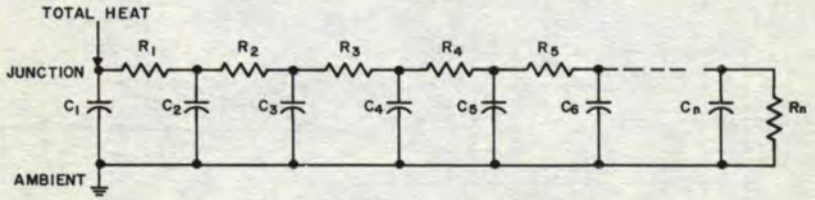

Figure 3.2 Simplified Equivalent Thermal Circuit for SCR

If the power input is terminated at time t_2 after the junction temperature has stabilized, the junction temperature will return to ambient along the locus indicated by T_{cool} in Figure 3.3B. It can be shown that curves T_{heat} and T_{cool} are conjugates of one another,[1] that is,

$$T_{cool} = \Delta T - T_{heat} = P\,\theta - T_{heat} \tag{3.2}$$

By dividing the instantaneous temperature rise of curve T_{heat} in Figure 3.3B by the power P causing the rise, the dimensions of the ordinate can be converted

from °C to °C/watt. This latter set of dimensions is that of thermal resistance, or as it is more precisely termed: the transient thermal impedance $\theta_{(t)}$. Figure 3.4 shows a plot of transient thermal impedance for the C35 SCR both when mounted to an infinite heatsink and to a four-inch square copper fin.

Transient thermal impedance information for a device can be obtained by monitoring junction temperature at the end of a well-defined power pulse or after a known steady-state load has been removed. Junction temperature is measured by use of one of the temperature-sensitive junction characteristics such as forward voltage drop at low currents. Conversion of heating data to cooling data, or vice versa, can be accomplished through the use of Equation 3.2.

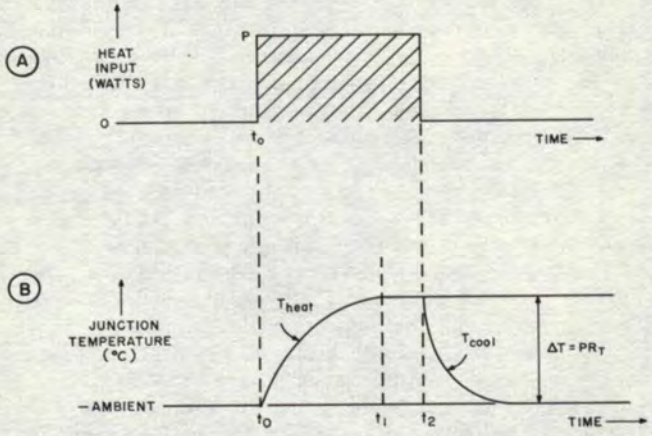

Figure 3.3 Response for SCR Junction to Step Pulse of Heating Power

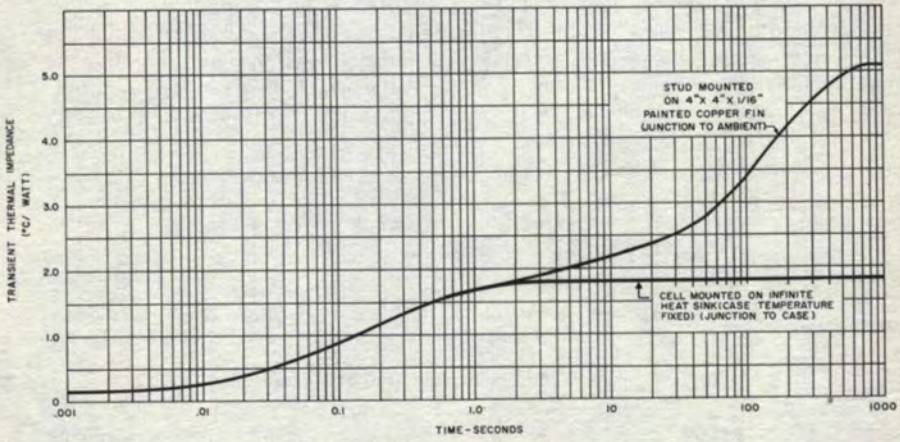

Figure 3.4 Transient Thermal Impedance of C35 SCR

In order to be able to use the transient thermal impedance curve with confidence in equipment designs, the curve represents the highest values of thermal impedance for each time interval that can be expected from the manufacturing distribution of the products. An additional slight safety factor is included to provide conservative application under all types of repetitive pulse loads.

The transient thermal impedance curve approaches asymptotic values at both the long time and short time extremes. For very long time intervals the transient thermal impedance approaches the steady-state thermal resistance θ.

For times less than 1 millisecond the value at 1 millisecond may be extrapolated by $1/\sqrt{t}$. For example the C35 transient thermal impedance at 10 μ seconds may be estimated as $\frac{.06}{\sqrt{10^{-3}/10^{-5}}} = .006°C/W$. However, the extrapolated values are valid only for times after the SCR has turned on fully. These values should, in other words, not be used during the switching interval (see Section 3.7). It is, furthermore, not suggested to extrapolate below 10 μ seconds. For maximum utilization of semiconductor devices in the microsecond region additional factors must be considered and other methods of rating and life testing must be used.

3.5 RECURRENT AND NON-RECURRENT CURRENT RATINGS

3.5.1 When a semiconductor device is applied in such a manner that its maximum allowable peak junction temperature is not exceeded at anytime the device is applied on a *recurrent* basis. Any condition that is a normal and repeated part of the application or equipment in which the semiconductor device is used must meet this condition if the device is to be applied on a recurrent basis. Section 3.6 gives methods of checking peak junction temperature. These enable the designer to properly apply the device on a recurrent duty basis.

A class of ratings that makes the SCR truly a power semiconductor are the *non-recurrent* current ratings. These ratings allow the maximum (recurrent) operating junction temperature of the device to be exceeded for a brief instant. This gives the device an instantaneous overcurrent capability allowing it to be coordinated with circuit protective devices. The specification bulletin gives these ratings in terms of surge current and I^2t. These ratings, then, should only be used to accommodate unusual circuit conditions not normally a part of the application, such as fault currents. Non-recurrent ratings are understood to apply to load conditions that will not occur more than a limited number of times in the course of the operating life of the equipment in which the SCR is finding application. For most SCR's this number of times is in the order of from one hundred to several hundred. Operation beyond this point may lead to a permanent degradation of the device's characteristics. Also, non-recurrent ratings are understood to apply only when they are not repeated before the peak junction temperature has returned to its maximum rated value or less.

3.5.2 Average Current Rating (Recurrent)

This is perhaps the most basic of current ratings. It is shown in the specification sheet as for the C35 series SCR in Figure 3.5. These curves specify the maximum allowable average anode current ratings of the SCR as a function of case temperature and conduction angle. Points on these curves are selected so that the junction temperature under the stated conditions does not exceed the maximum allowable value. The maximum rated junction temperature of the C35 SCR is 125°C.

The curves of Figure 3.5 include the effects of the small contribution to total dissipation by reverse blocking, gate drive, and switching up to 400 cps. For devices which are lead mounted or housed in small packages, like the TO-5 or TO-18, the forward current rating may be substantially affected by gate drive dissipation. Where this becomes important it is so indicated on the specification sheet.

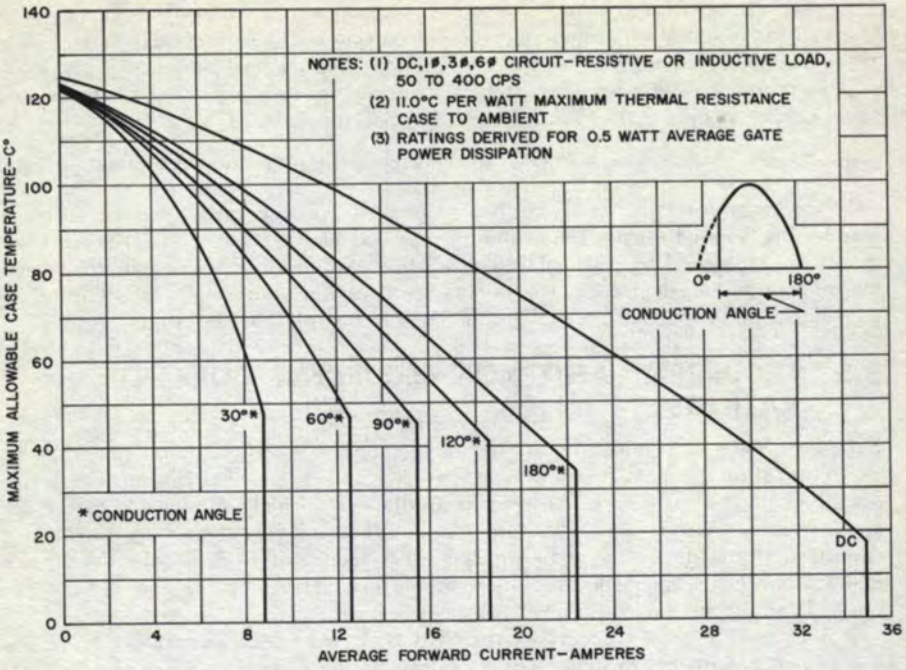

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Figure 3.5 Maximum Average Current Ratings for C35 Series SCR

If the C35 in a single phase resistive load circuit is triggered as soon as its anode swings positive, the device will conduct for 180 electrical degrees. If the case temperature is maintained at 80°C or less, the C35 is capable of handling 13 amperes average current as indicated in Figure 3.5. If the triggering angle is retarded by 120 degrees, the C35 will conduct for only the 60 remaining degrees of the half cycle. Under these conditions, the maximum rated average current at 80°C stud temperature is 9 amperes, substantially less than for 180 degrees conduction angle.

3.5.3 RMS Current (Recurrent)

It will be noted in Figure 3.5 that the curves for the various conduction waveshapes have definite end points. These points represent identical RMS values and as such give an RMS rating implicit in the curves of Figure 3.5.

For example, the C35 is rated 35 amperes DC or $\frac{35}{1.57} = 22.3$ amperes average in a half-wave, or 180° conduction angle, circuit. The factor 1.57 is the form factor giving the ratio of RMS to average values for a sinusoidal waveform. By the definition of RMS values, the RMS and average values are identical for a direct current. The RMS current rating, as shown on the specification sheet for individual SCR's, is necessary to prevent excessive heating in resistive elements of the SCR, such as joints, leads, etc.

The RMS current rating can be of importance when applying semiconductors to high peak current, low duty cycle waveforms. Although the average value of the waveform may be well within the ratings, it may be that the allowable RMS rating is being exceeded.

3.5.4 Arbitrary Current Waveshapes And Overloads (Recurrent)

Recurrent application of arbitrary waveshapes, varying duty cycles, and overloads requires that the maximum peak allowable junction temperature of the SCR not be exceeded at any time. Section 3.6 gives information for determining this.

3.5.5 Surge And I^2t Ratings (Non-Recurrent)

In the event that a type of overload or short circuit can be classified as non-recurrent, the rated junction temperature can be exceeded for a brief instant, thereby allowing additional overcurrent rating. Ratings for this type of non-recurrent duty are given by the Surge Current curve and by the I^2t rating.

Figure 3.6 shows the maximum allowable non-recurrent surge current at rated load conditions. Note that the junction temperature is assumed to be at its maximum rated value (125°C for the C35); it is therefore apparent that the junction temperature will exceed its rated value for a short time.

The data shown in this curve are values of peak rectified sinusoidal waveforms on a 60 cycles per second basis in a half-wave circuit. The "one-cycle" point, therefore, gives an allowable non-recurrent half sine wave of 0.00834 seconds' duration (half period of 60 cycle frequency) of a peak ampliutde of 150 amperes. The "20 cycle" point shows that 20 rectified half sine waves are permissible (separated by equal "off" times), *each* of an *equal* amplitude of 80 amperes.

I^2t ratings apply for non-recurrent overloads shorter than one cycle. For such times the SCR behaves essentially like a resistance with a fixed thermal capacity and no power dissipating means, and displays a current capability which can be expressed as a constant I^2t, where I is the RMS value of current over an interval t. The I^2t rating of the SCR is given in the specifications. This rating assumes that the SCR is already in the conducting state. If the SCR is turned on into a fault, the current-time relationships (di/dt) during the turn-on interval must be within the device's switching capabilities. Section 3.7 discusses turn-on switching dissipation in greater detail.

Provided the above precautions are observed, fault and overcurrent protection can be approached in the same manner as for power rectifier diodes. Protection methods are discussed in Chapter 13.

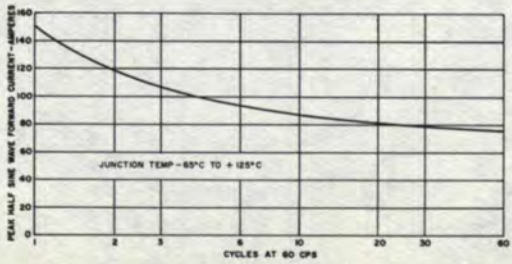

Figure 3.6 Maximum Allowable Non-Recurrent Peak Surge Forward Current at Rated Load Conditions for C35 Series SCR

3.6 BASIC LOAD CURRENT RATING EQUATIONS

3.6.1 In order for a device to be properly applied for recurrent load duty its maximum allowable peak operating junction temperature must not be exceeded. By knowing the dissipation of a semiconductor device and its thermal response it is possible to meet this requirement.

The information given on the G-E specification sheet, in conjunction with the proper equation in Figure 3.7, allows the designer to calculate power semiconductor ratings for a variety of conditions.*

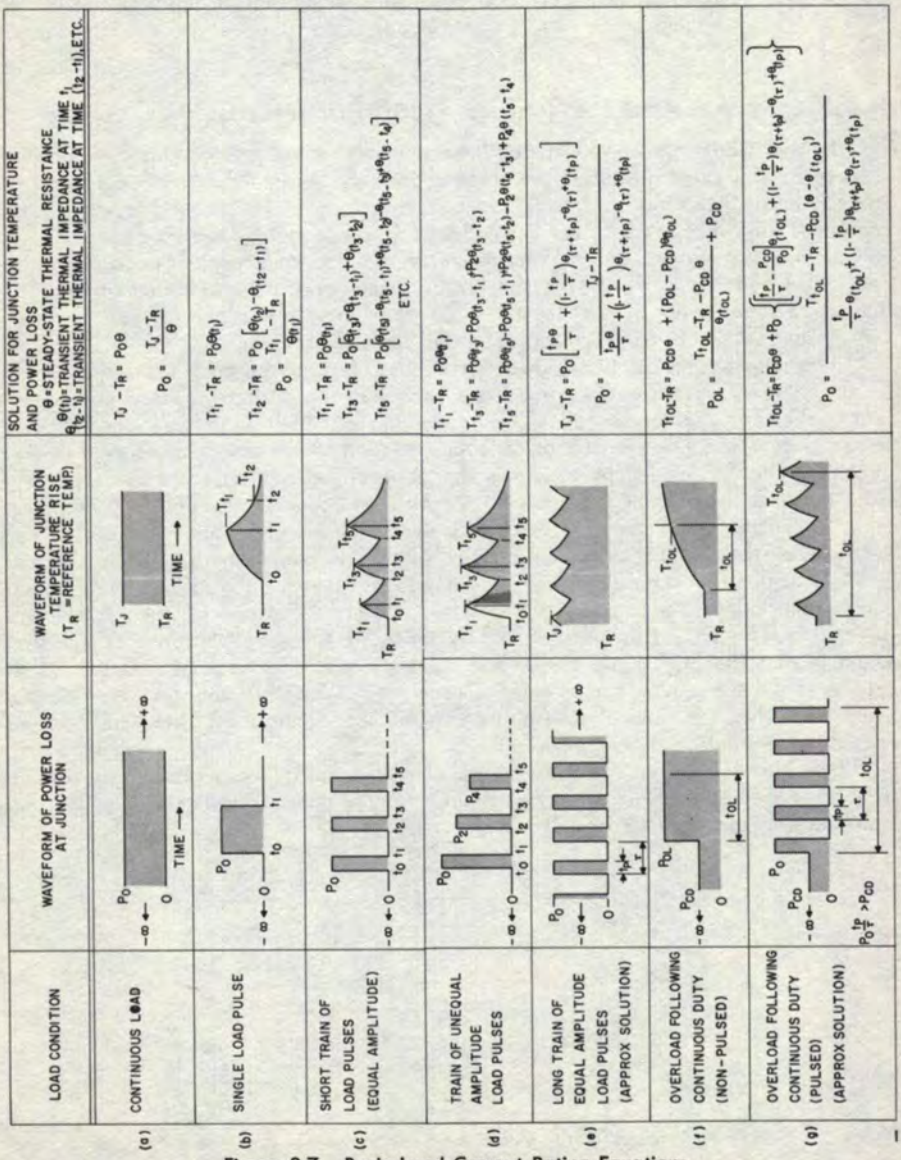

Figure 3.7 Basic Load Current Rating Equations

*For detailed development and discussion of these equations, write for Application Note 200.9, "Power Semiconductor Ratings Under Transient and Intermittent Loads."

3.6.2 Treatment Of Irregularly Shaped Power Pulses—Approximate Method

In the preceding section solutions for junction temperature were given in response to step functions of power input. In many practical applications, the power pulse is not of this ideal shape for computation, and appropriate approximations must be made to convert the actual waveshape into a rectangular form if the subsequent calculations are to be made as outlined.

Figure 3.8A illustrates the arbitrary waveshape of a power pulse that reoccurs at a period of τ seconds and has a peak value of P_{pk} watts and a full-cycle average of P_{avg} watts. For the purpose of calculating peak junction temperatures, this waveshape can be approximated by the rectangular waveshape of Figure 3.8B. This rectangular waveshape is selected to have the identical values of peak power P_{pk} and average power P_{avg} as Figure 3.8A by altering the pulse duration by a constant N to maintain the peak to average relationship. N is defined as the ratio of P_{avg} to P_{pk}.

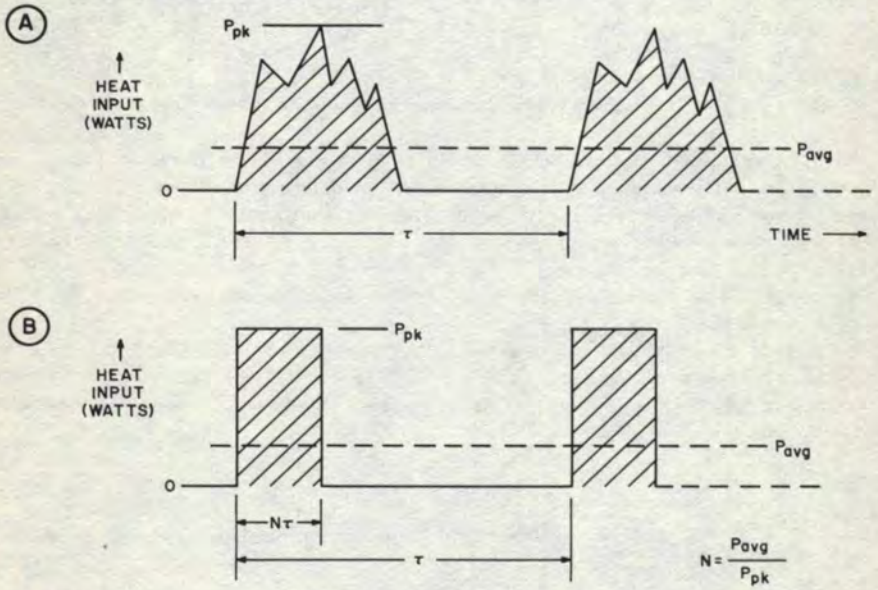

Figure 3.8 Approximating Irregularly Shaped Heating Pulse with Rectangular Waveshapes

This translation into rectangular pulses of power ensures a "worst case" approximation since a rectangular pulse of power will always have an effect on temperature rise which is equal to or greater than the effect of any other pulse having the same peak and average power. In other words, a rectangular power pulse will raise the junction temperature higher than any other waveshape with the same peak and average values since it concentrates its heating effects into a shorter period of time, thus minimizing cooling during the pulse.

Figure 3.9A illustrates a case where a similar type of approximation can be used to shorten the calculations for peak junction temperature when the problem would otherwise be too laborious. It involves the case where a sequence of power pulses is periodically interrupted by a longer "off" period of zero power. This is

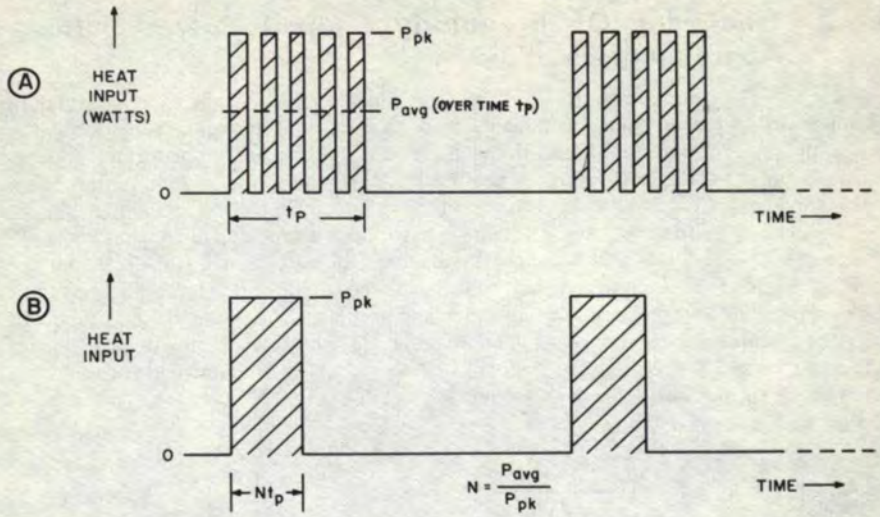

Figure 3.9 Approximating Bursts of Pulses with Single Rectangular Pulse of Power

typical of any repetitive or cyclical on-off type of load. Each burst of pulses can be represented by a single square-wave with introduction of only a relatively small error. This error will always yield a junction temperature higher than actual, and will thus provide a conservative application. In the equivalent waveshape shown in Figure 3.9B, the peak value of power P_{pk} is maintained the same as in Figure 3.9A. The duration of the equivalent rectangular waveshape is reduced to Nt_P where N is defined as P_{avg}/P_{pk}.

Sample Problem: Half wave sinusoidal current flows through a C35 SCR at 60 cps. The full cycle average value of this current is 10 amperes. Approximate the heating effect of a sequence of four cycles of current by a single rectangular wave of power.

Solution:

$$I_{peak} = \pi\, I_{avg} = 10\pi = 31.4 \text{ amperes}$$

$V_{peak} = 1.7$ volts at 31.4 amps from published specifications on C35

$$P_{peak} = I_{peak} \times V_{peak} = 31.4 \times 1.7 = 53.4 \text{ watts}$$

Full cycle average $P = 16$ watts at 10 amps average current from published specifications on C35

P_{avg} over 3½ cycles (actual duration of heating) $= 16 \times \frac{4}{3\frac{1}{2}} = 18.3$ watts

$$N = P_{avg}/P_{peak} = 18.3/53.4 = 0.34$$

$$t = 3.5 \text{ cycles} \times 1/60 \text{ cps} = .0585 \text{ second}$$

$$Nt = 0.34 \times .0585 = 0.020 \text{ second}$$

Thus the heating effect of the four cycles of current can be approximated by a single rectangular pulse of power with amplitude of 53.4 watts and a duration of 0.020 second. This is a conservative approximation.

3.6.3 The Effect of Heatsink Design on the Transient Thermal Resistance Curve

Since the heatsink is a major component in the heat transfer path between junction and ambient, its design affects the transient thermal impedance curve (Figure 3.4) substantially. When a semiconductor is manufactured and shipped to the user in a stud-mounted version, the manufacturer has no control over the ultimate heatsink and can only provide data on the heat transfer system between junction and stud, which is the part he manufactured. These type of data are presented in Figure 3.4 as the "Cell Mounted to Infinite Heatsink" curve.

The equipment designer can use this curve in developing a transient thermal impedance curve for the cell when mounted to a particular heatsink of his own design by means of a few simple calculations. These calculations assume that the temperature throughout the heatsink is uniform even under transient loading, thus permitting the heatsink to be represented by a single time constant. This is a good assumption for fins of relatively thick cross-section and fin effectiveness close to unity. This approach also assumes that the thermal capacity of the heatsink is large compared to the thermal capacity of the cell. By adding the calculated (or measured) transient thermal impedance of the fin to the "Infinite Heatsink" curve for the cell, the applicable curve can be plotted for the complete thermal system. The method can best be explained through an example illustrating how the second curve on Figure 3.4 (4″ x 4″ fin) can be calculated.

3.6.4 Example of Calculating the Transient Thermal Impedance Curve For a Specific Heatsink Design

Problem: A cell is mounted on a painted copper fin 1/16″ thick and 4″ on a side. The fin is subjected to free convection air conditions. Find the transient thermal impedance curve for a device mounted on this fin if the infinite heatsink curve in Figure 3.4 represents the thermal characteristics of the stud-mounted semiconductor. Assume that the stud to fin contact resistance is negligible.

Solution: From fin design curves (See Chapter 16):

$h_r = .005$ watt/inch^2 °C $\qquad h_c = .005$ watt/inch^2 °C

$h_{total} = h_r + h_c = .010$ watt/inch^2 °C

Fin thermal conductance $k = h \times A = .01 \times 4 \times 4$ inches$^2 \times 2$ sides $= 0.32$ watt/° C

Fin thermal resistance $\theta_f = \dfrac{1}{k} = \dfrac{1}{0.32} = 3.1$ °C/watt

Fin thermal capacity $C = c\rho V = \dfrac{175 \text{ watt-seconds}}{\text{lb °C}} \times 0.32 \text{ lb/in}^3$

$$\times 4 \text{ in.} \times 4 \text{ in.} \times 1/16 \text{ in.} = \frac{56 \text{ watt-seconds}}{\text{°C}}$$

Thermal RC time constant $= 3.1$ °C/watt $\times \dfrac{56 \text{ watt-seconds}}{\text{°C}} = 174$ seconds

Equation of transient fin thermal impedance, $\theta_{(t)F}$:

$$\theta_{(t)F} = \theta_F(1 - e^{-t/RC}) = 3.1\ (1 - e^{-t/174})$$

The values of $\theta_{(t)F}$ are added to the infinite heatsink curve to secure the over-all $\theta_{(t)}$ of the system as indicated in Figure 3.4. Note that this fin makes a negligible contribution to the over-all thermal impedance of the cell-heatsink system at periods of time one second or less after application of power. In this area the fin behaves like an infinite heatsink, that is, one of zero thermal resistance. The fin-heatsink system reaches equilibrium around 1000 seconds. Thereafter the thermal capacity is no longer effective in holding down the junction temperature.

3.7 TURN-ON SWITCHING RATINGS

In many cases the SCR may be assumed to turn on instantaneously. This assumption is valid if the rate of rise of anode current (di/dt) is slow compared to the time required for the semiconductor junctions to reach a state of full forward conduction at uniform current density. The current ratings discussed in the preceding sections are based on such a condition of uniform current density. In other words, the peak junction temperature, on which the recurrent and nonrecurrent current ratings are based, is assumed to occur uniformly across the entire junction interfaces.

In cases where the rate of rise of anode current (di/dt) is very rapid compared to the spreading velocity of the turn-on process across the junctions, local "hot spot" heating will occur due to high current density in those junction regions that have started to conduct.[7] Particularly, if the SCR is switched from a high blocking voltage at a very large value of di/dt, turn-on switching dissipation in localized regions of the SCR may lead to an excessive temperature rise and cause device failure at a "hot spot."

Figure 3.10 shows maximum allowable anode turn-on current as a function of time for the G-E C35 type SCR (2N681 series). Figure 3.10 is valid up to switching frequencies of 400 cps. At higher frequencies the average contribution of the turn-on switching dissipation to the junction temperature rise above its case temperature may require additional derating of operating case temperature. For the sake of illustration in the use of these curves, it is desired to find the allowable peak of a sinusoidal current pulse of a duration of 150 microseconds when switching from 800 volts. Cutting a template of a sinusoidal waveform from log-log paper of the same scale, and placing it to the right and under the rating curves, yields the desired answer. The sinusoid is shown in Figure 3.10 with its ascending portion tangential to the heavy "800 volt" line and its peak at half of the desired pulse duration or 75 microseconds. The peak current amplitude can then be seen to be about 525 amperes for the C35 type when switching from 800 volts.

If initial linear rate of rise of anode current is required for a specified period of time, values may be read directly from Figure 3.10. For example, when switching from 200 volts, the anode current should not exceed about 85 amperes at 1 microsecond.

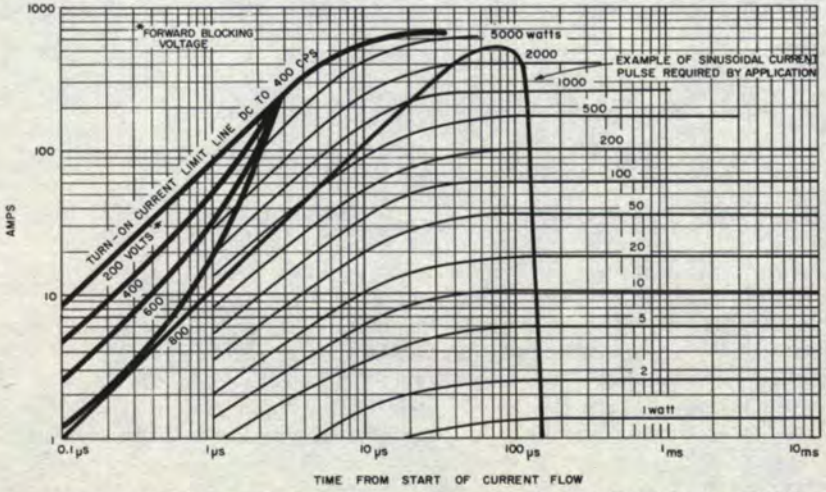

Figure 3.10 Maximum Allowable Anode Turn-On Current (For C35 Type SCR)

A test for the relative turn-on performance of an SCR is to subject the device to a sinusoidal current pulse of known duration t_p and an amplitude known to be within the capability of the device. If the voltage drop across the device is observed at the current peak at time $t_p/2$, a measure of the current density in the device at that time is obtained. A lower voltage drop indicates a greater amount of active device area turned on, and thus better turn-on switching, or di/dt, performance. Relative tests of this nature can be conducted in the test circuit shown in Figure 18.9. For test values for particular devices please consult the factory.

3.7.1 Saturable Reactor For Increasing Turn-on Switching Capability

A saturable reactor inserted in series with the SCR during its turn-on switching interval will greatly reduce the aforementioned switching dissipation in the SCR.[8] When the SCR is triggered on, the amount of current that will flow during the turn-on interval is limited to the magnetizing current of the reactor. The reactor is designed to go into magnetic saturation after the SCR has turned on. Then the reactor switches the current at a time when the SCR has attained uniform current density across all junctions. The SCR's full active area is, therefore, available to assume full load current at minimum dissipation. Since the load current is delayed, the output of the SCR-reactor combination is delayed relative to the SCR trigger signal. Realistic pulse repetition rates are achievable by this technique, notably in many pulse modulator applications.

The delay time t of the saturable reactor is given by the time to saturate

$$t_s = \frac{NA\triangle B}{E} \text{ (seconds), where} \qquad (3.3)$$

N = number of turns

A = cross sectional area of core in square centimeters

$\triangle B$ = total flux density change in Gauss

E = maximum circuit voltage being switched in volts

The current required at the time of saturable reactor switching I_s should be made small compared to the peak load current being switched. It is:

$$I_s = \frac{H_s\, l_m}{0.4\pi N} \text{ (amperes), where} \qquad (3.4)$$

H_s = magnetizing force required for core flux to reach saturation flux density B_s in Oersteds (1 Oersted = 2.021 ampere-turns/inch)

l_m = mean length of core in centimeters

N = number of turns

Provision must be made to properly reset the core before the next current pulse. Depending on the details of the circuit, reset may be accomplished by the resonant reversal of current or by auxiliary means.

3.8 VOLTAGE RATINGS

3.8.1 The voltage ratings of SCR's are designated by the suffix letter in the model number of the device (e.g., C35B) or by its JEDEC number. The designation is

translated in the specifications and defines the continuous peak voltage which the device will withstand in both the forward and reverse directions without breaking down. It is applicable to any junction temperature within the specified operating range. This symmetry of forward and reverse voltage ratings is characteristic of all standard SCR's today. The following discusses each voltage rating in more detail.

3.8.2 Reverse Voltage

In the reverse direction (anode negative with respect to cathode), the SCR behaves like a conventional silicon rectifier diode. General Electric assigns two types of reverse voltage ratings: repetitive peak reverse voltage with gate open, V_{ROM}(rep) (formerly designated by "repetitive PRV"); and non-repetitive peak reverse voltage with gate open, V_{ROM}(non-rep) (formerly designated by "non-repetitive PRV").

If these ratings are substantially exceeded, the device will go into breakdown and may destroy itself. Where transient reverse voltages are excessive, additional V_{ROM} margin may be built into the circuit by inserting a diode rectifier of equivalent current rating in series with the controlled rectifier to assist it in handling reverse voltage. For a detailed discussion on voltage transients, see Chapter 14.

A specified minimum heatsink is required for the device to meet its maximum V_{ROM}(rep) rating. The reverse stability criterion of a semiconductor rectifier requires that the total junction-to-ambient thermal resistance be kept below a critical maximum value.[2] The size of the required minimum heatsink is always very small (high thermal resistance) compared to the heatsink normally applied to the device in order to achieve its full current output rating.

3.8.3 Forward Voltage

The minimum forward breakover voltage $V_{(BR)FX}$ is given on the specification bulletin at maximum allowable junction temperature (worst case). The larger SCR's are specified for a minimum forward breakover voltage with the gate open, $V_{(BR)FO}$; smaller SCR's may be characterized for a voltage $V_{(BR)FR}$ with a specified gate-to-cathode bias resistor.

Forward voltage blocking ratings are sensitive to temperature, gate drive, and rate of rise of forward voltage (dv/dt). As temperature increases, $V_{(BR)FX}$ tends to decrease; it is, therefore, important that $V_{(BR)FX}$ be specified at maximum junction temperature. As gate drive is increased, $V_{(BR)FX}$ decreases. This characteristic is used for turning the SCR "on" by means of the gate and is discussed in Chapter 4. Rate of voltage rise is discussed in Section 3.9.

3.8.4 Peak Forward Voltage (PFV)

An SCR can be turned on in the absence of any gate drive by exceeding its forward breakover voltage $V_{(BR)FX}$ at the prevailing temperature conditions. Although SCR's, in contrast to four layer diodes, are designed to be brought into conduction by means of driving the gate, breakover in the forward direction is non-destructive for some of the older types of SCR's, provided it takes place below a value noted in the specification sheet as Peak Forward Voltage (PFV). Voltage beyond the PFV rating may cause degradation of some SCR's, and eventual failure. Figure 3.11 illustrates the relationship of PFV to $V_{(BR)FO}$.

It will be noted that usually a given SCR has a single PFV rating independent of its V_{ROM} (rep)-$V_{(BR)FX}$ voltage class designation. This is due to the fact that the limit on PFV is not an inherent characteristic of the bulk properties of the semi-

conductor junction but rather one of the construction of the device and the pellet surface properties of the entire line of a particular device class.

The PFV rating is often of practical importance when SCR's are tested for $V_{(BR)FX}$ at room temperature; often a unit will have a $V_{(BR)FX}$ beyond its PFV rating at temperatures lower than maximum rated junction temperature. A proper test for $V_{(BR)FX}$ under these circumstances would be to conduct it at the elevated temperature at which the minimum $V_{(BR)FX}$ for the device is specified.

In applications where the PFV rating of an SCR may be exceeded it is suggested that a network be connected anode to gate so that the device will trigger by gate drive rather than by forward breakover. A zener diode may be used to effect gate triggering at a predetermined level, or a Thyrector diode may be used to obtain a similar action.

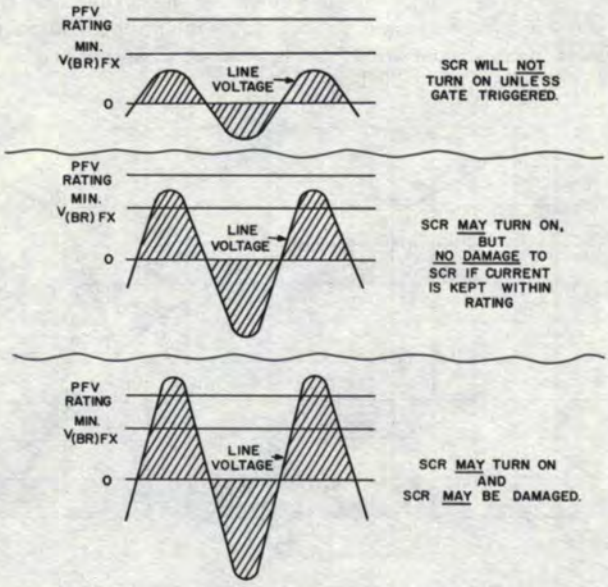

Figure 3.11 Significance of $V_{(BR)FO}$ and PFV

Many of the more recent SCR's (e.g. C80's, C45's, etc.) are not assigned PFV ratings due to improved design and manufacturing techniques. These types, therefore, do not indicate a PFV rating on the specification sheet. SCR types that do not have assigned PFV ratings may be switched into conduction by anode voltage breakover subject to the turn-on current (di/dt) limitations discussed in Section 3.7.

3.9 RATE OF RISE OF FORWARD VOLTAGE (dv/dt)

A high rate of rise of forward (anode-to-cathode) voltage may cause an SCR to switch into the "on" or low impedance forward conducting state. In the interest of circuit reliability it is, therefore, of practical importance to characterize the device with respect to its dv/dt withstand capability.

General Electric SCR's are characterized with respect to dv/dt withstand capability in two contexts:

1. The so-called static dv/dt withstand capability. This specification covers the case of initially energizing the circuit or operating the device from an anode voltage source which has superposed fast rise-time transients. Such transients may arise from the operation of circuit switching devices or result from other SCR's operating in adjacent circuits. Interference and interaction phenomena of this type are discussed further in Chapter 15.
2. The maximum allowable rate of reapplication of forward blocking voltage, while the SCR is regaining its rated forward blocking voltage $V_{(BR)FX}$, following the device's turn-off time t_{off} under stated circuit and temperature conditions. In this context dv/dt is an important part of the overall SCR turn-off time characterization. This type of dv/dt specification is covered in more detail in Chapter 5.

Figure 3.12 shows the typical static dv/dt withstand capability of the General Electric C38 type medium current SCR as a function of temperature with its gate open. The rate of rise of anode voltage shown on the ordinate is the slope of a straight line starting at zero anode voltage and extending through the one time constant (τ) point on an exponentially rising voltage. The upper right hand portion of Figure 3.12 illustrates this definition.

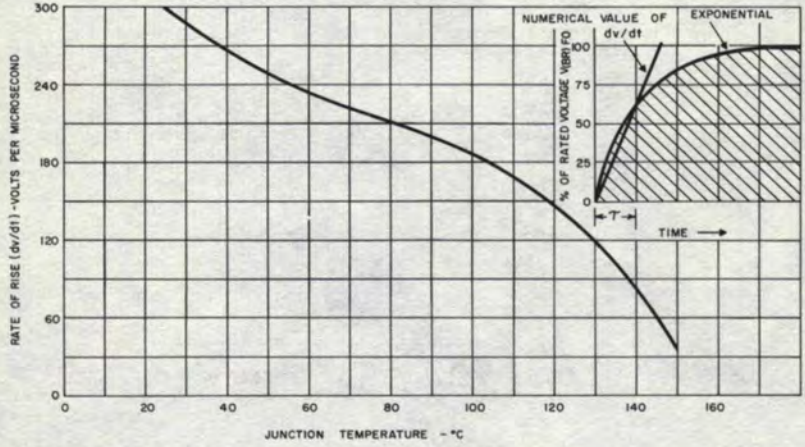

Figure 3.12 Rate of Rise (dv/dt) of Forward Voltage That Will Not Turn On SCR

The definition used in Figure 3.12 is the one that has come into standard industry usage. Some specification sheets give the time constant τ under specified conditions rather than a curve like Figure 3.12.

It will be noted that

$$\tau = \frac{0.632 \times \text{Rated SCR Voltage } (V_{(BR)FX})}{dv/dt} \tag{3.5}$$

The initial dv/dt withstand capability will be recognized as being greater than the value defined in Figure 3.12. In terms of specified minimum time constant it is

$$\left.\frac{dv}{dt}\right|_{t=0+} = \frac{\text{Rated SCR Voltage } (V_{(BR)FX})}{\tau} \tag{3.6}$$

In terms of specified maximum dv/dt capability, the allowable initial dv/dt withstand capability is

$$\left.\frac{dv}{dt}\right|_{t=0+} = \frac{1}{0.632}\ dv/dt = 1.58\ dv/dt \qquad (3.7)$$

The shaded area shown in the insert of Figure 3.12 represents the area of dv/dt values that will not trigger the SCR. These data enable the circuit designer to tailor his circuitry in such a manner that reliable circuit operation is assured.

Since a high circuit-imposed dv/dt effectively reduces $V_{(BR)FX}$ under given temperature conditions, a higher voltage classification unit will allow a higher rate of rise of forward voltage for a given peak circuit voltage. For example, a C38B type ($V_{(BR)FX} = 200$ volts) at $T_J = 130°C$ is operating under a peak circuit voltage of E = 150 volts, or $\frac{150}{200} \times 100 = 75\%$ of rated voltage. Figure 3.12 shows that we may apply a dv/dt = 120 volts/microsecond to the one time constant (τ) point of an exponentially rising voltage. In our example, by Equation 3.5, $\tau_1 = \frac{.632 \times 200}{120}$ = 1.06 microseconds. Accordingly, the time in which the anode of the C38B may reach 150 volts, or 75% of rated voltage, is, from Figure 3.12, $t_1 = 1.5\tau_1 = 1.5 \times 1.06 \approx 1.6$ microseconds.

Had we selected a C38D type ($V_{(BR)FX} = 400$ volts) under the same conditions we find, using the ratio of rated voltages in Equation 3.5, that $\tau_2 = \tau_1 \frac{400}{200} = 2\tau_1 = 2 \times 1.06 = 2.12$ microseconds to reach 63.2% of 400 or 374 volts. Since, in our example, we need to reach only 150 volts, or $\frac{150}{400} = 38.6\%$ of the rated C38D $V_{(BR)FX}$, we see, from the insert of Figure 3.12, that $t_2 \approx 0.5\tau_2 = 0.5\ (2.12) = 1.06$ microseconds.

By selecting a 400 volt device the time to reach the operating circuit voltage can, in this example, be reduced by $\frac{t_2}{t_1} = \frac{1.06}{1.6}\ (100) \approx 67\%$.

Reverse biasing of the gate with respect to the cathode substantially increases dv/dt withstand capability beyond that shown in Figure 3.12. The reader is referred to Section 4.5.2 for further discussion.

The circuit shown in Figure 3.13 can be used to suppress excessive rate of rise of anode voltage. The time constant of the load resistance R_L in ohms and capacitor C in microfarads should be selected so that

$$\tau \leq R_L\ C\ \text{(microseconds), where} \qquad (3.8)$$

τ = minimum time constant of exponential forward voltage rise specified for SCR.

Resistor R_d discharges capacitor C. It should be selected on the basis of limiting the peak capacitor discharge current $\frac{E}{R_d}$ during the SCR turn-on interval to a value within the device's capability (see Section 3.7). For best results, the circuit of Figure 3.13 should be wired and placed in close proximity to the SCR in order to minimize inductive effects. Also, the capacitor should have good high frequency characteristics.

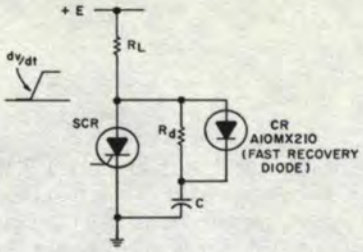

Figure 3.13 Rate of Rise of Anode Voltage (dv/dt) Suppression Circuit

3.10 GATE CIRCUIT RATINGS

Maximum ratings for the gate circuit are discussed in Chapter 4.

3.11 HOLDING CURRENT

Somewhat analogous to the solenoid of an electromechanical relay, an SCR requires a certain minimum anode current to maintain it in the "closed" or conducting state. If the anode current drops below this minimum level, designated as the holding current, the SCR reverts to the forward blocking or "open" state. The holding current for a typical SCR has a negative temperature coefficient; that is, as its junction temperature rises, its holding current requirement decreases.

A somewhat higher value of anode current than the holding current is required for the SCR to initially "pickup." If this higher value of anode latching current is not reached, the SCR will revert to the blocking state as soon as the gate signal is removed. Immediately after this initial pickup action, however, the anode current may be reduced to the holding current level. Where circuit inductance limits the rate of rise of anode current and thereby prevents the SCR from switching solidly into the conducting state, it may be necessary to make alterations in the circuit. This is discussed further in Chapter 4.

3.12 RELIABILITY, STABILITY, AND FAILURE MECHANISMS

General Electric SCR's, like rectifier diodes, are subject to very stringent quality control standards. The concept of quality control is total; that is, it is integrated into all the steps from initial design through evaluation, incoming parts inspection, in-process control, design center testing, environmental testing, acceptance testing, and life testing.

Failure criteria are based on variation out of specification of a given device parameter rather than any type of catastrophic failure. On full load tests, all parameters are operated at their maximum rated values. For this reason, failures under these conditions represent the most pessimistic case, since in an actual application it is rare that all parameters are being operated at their maximum rated values.

The designer in some cases has available to him a choice between different devices in a given current rating range. Figure 3.14 illustrates three such devices in the low current range. Shown are the standard C11 type, the general purpose C20 stud-mounted and C22 "press fit" types, and the high reliability C11DR700 type.

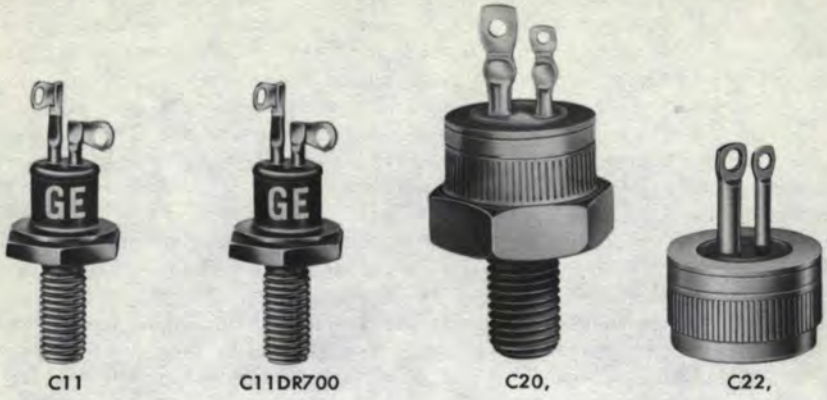

Figure 3.14 Four Types of SCR's in Same Rating Range: Standard C11 Type, General Purpose C20, "Press Fit" C22, and High Reliability C11DR700

Each of these devices is specified to meet the needs of the application for which they are designed.

The standard type has very complete specifications, continuous production and quality assurance testing, and a design to give excellent performance over a wide temperature range and under fluctuating load conditions. The general purpose type is designed for less demanding applications where cost is a primary consideration. Specifications are not as complete for this type of device, and its less complicated design and manufacturing process allow for simpler testing procedures. For applications requiring demonstrated reliability figures at high confidence levels the high reliability type is available. These devices are subjected to very elaborate testing procedures over long periods of time in order to demonstrate the reliability figures quoted. The high cost associated with accumulating meaningful reliability data is justified largely for military high reliability programs. Chapter 17 discusses the general subject of reliability in greater detail.

Stability of device parameters is considered very important in obtaining high levels of reliability. One of the most stringent tests to which a controlled rectifier can be subjected is that of an elevated temperature blocking life test. This is a test performed on all General Electric controlled rectifiers for a duration determined by statistical criteria of confidence level. It has been found that if a device is subject to a possible drift in any of the parameters due to the onset of a degradation mechanism, it will show up by the end of a blocking life test. This test may be considered a type of accelerated "aging" test to screen a production line for possible future failures.

Failure mechanisms of controlled rectifiers generally fall into three categories:

First, there is the possibility of an increase of surface conductivity of the silicon pellet as a result of chemical activation of sealed-in contaminations or by an imperfect hermetic seal allowing moisture penetration from the atmosphere. The electrical consequences are reduction in forward blocking capability and an increase in reverse blocking current. However, reduction of forward blocking capability is also often the first indication that some rating of the device is being overstressed by such causes as current surges or voltage transients.

Fracturing of the silicon pellet is another possible failure mechanism. Usually, high current overloads, extreme temperature cycling, or excessive mechanical abuse lead to this condition.

Finally, thermal fatigue which develops as a result of many temperature cycles may lead to ultimate failure if the thermal impedance of the device structure increases and leads to increased dissipation and finally junction temperatures above rated value. Certain so-called "soft" solders used in attaching the silicon sandwich to the stud in some devices can recrystallize, over certain extreme temperature cycles, causing deterioration of the solder joints. This type of failure mechanism was first noticed among some of the older types of rectifier diodes. It has, however, not been a problem with G-E controlled rectifiers for two reasons. Higher temperature SCR's use improved, so-called "hard," soldering techniques and SCR's using soft solder techniques are limited by their temperature ratings to operation over smaller temperature ranges, and hence are subjected to negligible thermal fatigue stresses.

In certain high reliability applications it is often required to take additional steps to increase the reliability and stability of the device even beyond the high levels already being achieved with standard products. Junction temperature derating by derating current or larger heatsinking is perhaps the single most effective way of going in the direction of increased potential reliability. Other steps that can be taken in this direction are above all to keep the device applied well within ratings and not subjected to either overvoltages or overcurrents in excess of specified ratings. Applied within its ratings, the controlled rectifier has taken its place among the most reliable of all semiconductor devices.

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Gate Trigger Characteristics, Ratings, And Methods

The design of trigger circuits for SCR's involves these important considerations: (1) choice of a suitable circuit which will supply the proper trigger signal under the prevailing circuit and temperature conditions; (2) determination of the maximum voltages and currents which the trigger circuit can supply to the gates of the SCR's without exceeding maximum allowable gate ratings; and (3) determination of the minimum voltages and currents which the trigger circuit will supply to the gates of the SCR's to ensure that the SCR's will be triggered reliably under all conditions. Since the SCR is designed to be triggered by means of the gate, this chapter describes the trigger characteristics of the SCR, the considerations for proper design of trigger circuits, and different types of basic trigger circuits. Beyond the material presented here, further examples of the use of these trigger circuits in practical applications are given in chapters 6, 7, 8, 9, 10, and 12.

4.1 GATE E-I CHARACTERISTICS

The gate trigger characteristics of an SCR are presented in the form of a graph similar to Figure 4.1 which applies to the C35 (2N681) type SCR.

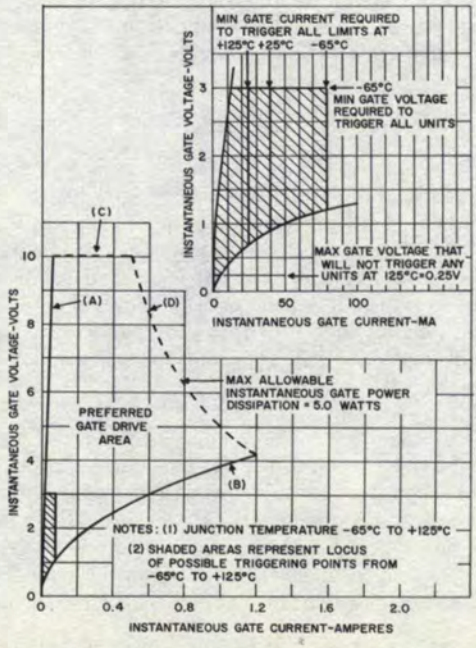


Figure 4.1 Gate Triggering Characteristics (For C35 Type SCR)

The graph shows gate-to-cathode voltage as a function of positive gate current (flow from gate to cathode) between limit lines (A) and (B) for all SCR's of the type indicated. Since the SCR gate-to-cathode circuit consists of a p-n junction, the gate characteristic of an SCR may be considered to be the static forward characteristic of this p-n junction.

A given SCR will trigger at a definite point (I_{GT}, V_{GT}) on its gate characteristic. The basic function of the trigger circuit is to simultaneously supply the gate current to trigger I_{GT} and its associated gate voltage to trigger V_{GT}. The shaded area shown in Figure 4.1 contains all the possible trigger points (I_{GT}, V_{GT}) of all SCR's conforming to this specification. The trigger circuit must, therefore, provide a signal (I_{GT}, V_{GT}) *outside* of the shaded area in order to reliably trigger all SCR's of that specification.

The area of trigger circuit—SCR gate operation is indicated as the "preferred gate drive area." It is bounded by the shaded area in Figure 4.1 which represents the locus of all specified triggering points (I_{GT}, V_{GT}), the limit lines (A) and (B), line (C) representing rated peak allowable forward gate voltage V_{GF}, and line (D) representing rated peak power dissipation P_{GM}. Some SCR's may also have a rated peak gate current I_{GFM} which would appear as a vertical line joining curves (B) and (D).

The insert in the upper right hand portion of Figure 4.1 shows the detail of the locus of all specified trigger points, and the temperature dependence of the minimum gate current to trigger $I_{GT_{min}}$. The lower the junction temperature, the more gate drive is required for triggering. (Some specifications may also show the effect of forward anode voltage on trigger sensitivity. Increased anode voltage, particularly with small SCR's, tends to reduce the gate drive requirement). Also shown is the small positive value of gate voltage below which no SCR of the particular type will trigger. (See Section 4.3.)

The reverse quadrant of the gate characteristic is usually specified in terms of maximum voltage and power ratings. The application of reverse bias voltage and the extraction of reverse gate current for increased SCR off-state stability is discussed in Section 4.5.2.

4.2 LOAD LINES

The trigger circuit load line must intersect the individual SCR gate characteristic in the region indicated as "preferred gate drive area" in Figure 4.1. The intersection, or maximum operating point, should furthermore be located as close to the maximum applicable (peak, average, etc.) gate power dissipation curve as possible. Gate current rise times should be in the order of several amperes per microsecond in the interest of minimizing anode turn-on time particularly when switching into high currents. This in turn results in minimum turn-on anode switching dissipation and minimum jitter.

Construction of a "load line" is a convenient means of placing the maximum operating point of the trigger circuit-SCR gate combination into the preferred triggering area. Figure 4.2(a) illustrates a basic trigger circuit of source voltage e_s and internal resistance R_G driving an SCR gate. Figure 4.2(b) shows the placement of the maximum operating point well into the "preferred trigger" area close to the rated dissipation curve. The load line is constructed by connecting a straight line between the trigger circuit open-circuit voltage E_{oc}, entered on the ordinate, and the trigger circuit short-circuit current $I_{sc} = \frac{E_{oc}}{R_G}$ entered on the absissa.

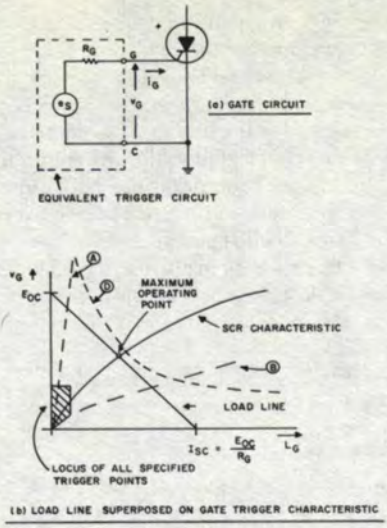


Figure 4.2 Gate Circuit and Construction of Load Line

If the trigger circuit source voltage is a function of time e_s (t), the load line sweeps across the graph, starting as a point at the origin and reaching its maximum position, the load line, at the peak trigger circuit output voltage.

The applicable gate power curve is selected on the basis of whether average or peak allowable gate power dissipation is limiting. For example, if a DC trigger is used, the average maximum allowable gate dissipation (0.5 watt for C35) must not be exceeded. If a trigger pulse is used the peak gate power curve is applicable (for the C35, the 5 watt peak power curve labelled D in Figure 4.1). For intermediate gate trigger waveforms the limiting allowable gate power dissipation curve is determined by the duty cycle of the trigger signal according to average allowable gate power $\leq$ peak gate drive power $\times \frac{\text{ON}}{\text{ON}+\text{OFF}}$.

4.3 POSITIVE GATE VOLTAGE THAT WILL NOT TRIGGER SCR

Figure 4.1 also indicates the maximum gate voltage that will not trigger the SCR. For example, for the C35 (2N681) type, Figure 4.1 shows that at 125°C junction temperature this value is 0.25 volt. This limit is important when designing a trigger circuit which has a standby leakage current when no trigger signal is present. Examples of this are saturable reactors and directly coupled unijunction transistor trigger circuits. To prevent false triggering under these circumstances, a resistor should be connected across the output of the trigger circuit. Its value of resistance in ohms should not exceed the maximum gate voltage that will not trigger divided by the maximum trigger circuit standby current.

4.4 POSITIVE GATE VOLTAGE WHEN ANODE IS NEGATIVE

The presence of positive voltage on the gate when reverse voltage is applied to the anode increases reverse blocking (leakage) current through the device sub-

stantially. As a result, the SCR must dissipate additional power. It is, therefore, necessary either to make provision for this additional loss or to take steps to limit it to a negligible value.

Figure 4.3 gives the temperature derating for different SCR lines at various gate drive duty cycles (per cent of full cycle or 360 electrical degrees) for values of peak positive gate voltage. For proper application, this loss must be included in the total device dissipation. The temperature derating, ΔT, found from Figure 4.3, must be subtracted from the maximum allowable stud temperature (found from a curve such as Figure 3.5) for the proper cell type and conduction angle. For lead mounted devices, subtract from the ambient temperature curve. Derating becomes negligible if the gate voltage is less than 0.25 volt or the temperature derating turns out to be 1°C or less.

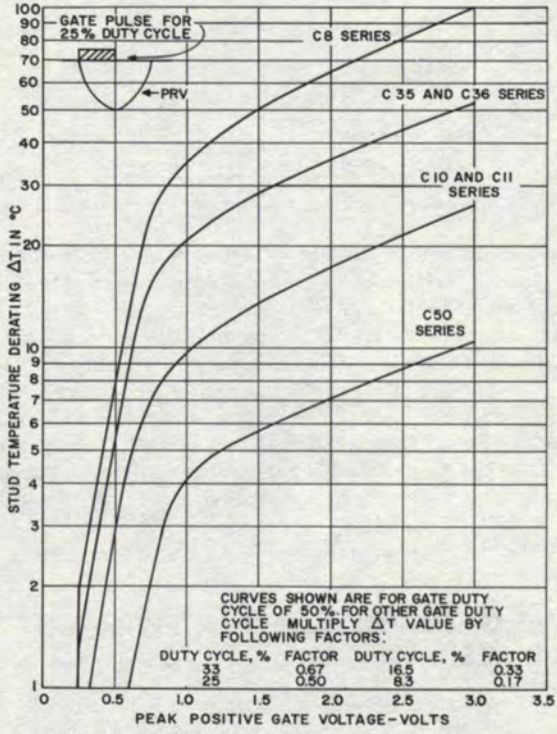


Figure 4.3 Temperature Derating Curve for Simultaneous Application of Positive Gate Pulse when Anode is Negative

A means of limiting the additional reverse dissipation to a negligible value is given by a gate clamping circuit of the type shown in Figure 4.4 for low and medium current SCR's (C10 and C35 series). Resistor R_A and a diode are connected from gate to anode to attenuate positive gate signals whenever the anode is negative. For a given peak value of open circuit gate source voltage, Figure 4.4 gives the maximum ratio of the value of R_A to R_G that will safely clamp the gate for all values of reverse voltage within the reverse voltage rating of the SCR.

An alternate way to limit additional reverse leakage dissipation due to positive gate voltage is to insert in series with the SCR a rectifier diode that has a lower reverse blocking current. In this manner the diode will assume the greater share of

the reverse voltage applied to the series string, significantly reducing reverse dissipation in the SCR.

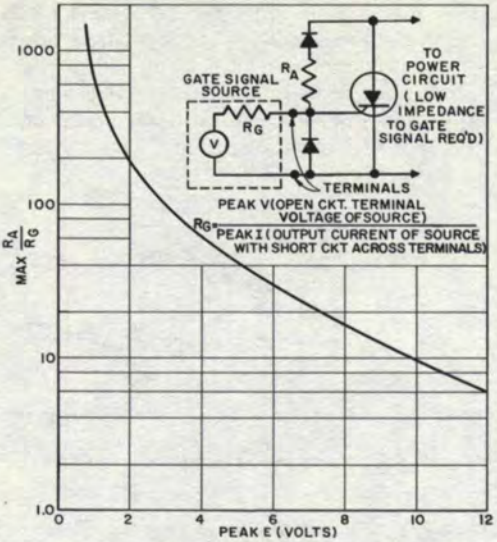


Figure 4.4 Gate Clamp Circuit for Controlled Rectifier

4.5 NEGATIVE GATE VOLTAGE AND CURRENT

The gate should never be allowed to become more negative with respect to the cathode than is indicated on the specification bulletin. For example, the gate of the C35 (2N681) type has a rated peak reverse voltage of 5 volts. If there is a possibility that the gate will swing more negative than the rated value, a diode should be connected either in series with the gate, or from cathode to gate to limit the reverse gate voltage. A considerable negative gate current (conventional current flow out of the gate) can be caused to flow if the cathode circuit between cathode and gate is opened for any reason while the SCR is conducting forward load current (conventional current flow from anode to cathode). This current would initially be limited only by the impedance of the gate circuit and could cause the allowable gate dissipation to be exceeded, thus leading to possible failure of the SCR.

4.5.1 Negative Gate Biasing

Negative gate bias, when the anode is positive, tends to increase the forward breakover voltage $V_{(BR)FX}$ (Section 3.8.3) and the dv/dt withstand capability (Section 3.9) of the SCR for a given junction temperature.

The effect of negative gate bias on $V_{(BR)FX}$ is greatest for the smaller junction area devices. For example, the C5 types (2N1595, etc). have $V_{(BR)FR}$ specified for a certain value of gate-to-cathode resistance (R_{GC} = 1000 ohms) and at a specified junction temperature. For more detail on the effect of negative gate bias on small SCR's the reader is referred to Reference 1. The resistor R_{GC} shown in Figure 4.5(a) provides a diversionary path for negative gate current (out of gate) around the gate-to-cathode emitter junction. The resistor thereby reduces the forward

bias on the emitter (due to effects of temperature, anode voltage, or dv/dt of anode voltage) and increases circuit stability by effectively increasing $V_{(BR)FR}$ and dv/dt withstand capability. The lower the value of the resistor, the greater is its effectiveness. Resistive gate biasing reduces the gate input sensitivity because the trigger circuit must also supply shunt current to the bias resistor. For example, where DC triggering is used with small SCR's, protection against line transients and other dv/dt phenomena can be obtained, without loss of DC input sensitivity, by connecting a small capacitor between gate and cathode. A value of .05μf is often sufficient. In extremely critical applications small amounts of external negative gate bias may be added externally. Figures 4.5(b) and 4.5(c) illustrate two possible arrangements.

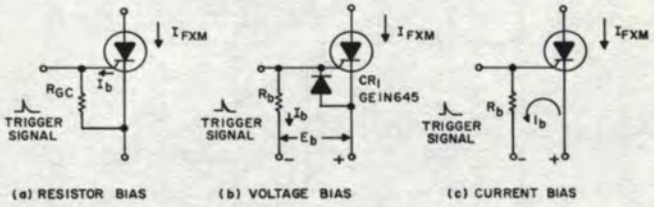


Figure 4.5 Negative Gate Bias Arrangements

Figure 4.5(b) shows a voltage bias arrangement. Resistor R_b is taken to a negative supply instead of being merely returned to the cathode as in Figure 4.5(a). The voltage source E_b establishes a current $I_b \cong \frac{E_b - D}{R}$, where D is the voltage drop across diode CR1 (typical value 0.7 volt). The diode provides a fixed negative bias voltage gate-to-cathode for the SCR. The disadvantage of this approach, however, is the loss of input sensitivity due to resistor R_b.

Figure 4.5(c) shows a current bias scheme useful for smaller junction diameter SCR's. Resistor R and the bias source are selected so that a bias current $I_b \cong I_{FXM}$ is established through resistor R in the direction indicated; I_{FXM} is the maximum forward blocking (leakage) current of the SCR under the prevailing junction temperature and anode voltage. Selection of I_b in this manner yields a "worst case" design on the assumption that most, if not all, of I_{FXM} will be diverted from the SCR emitter (gate-cathode junction). This approach is limited to SCR's which have sufficient reverse gate power ratings to handle reverse current I_b at its associated reverse gate voltage. The scheme of Figure 4.5(c) is suitable, for example, for General Electric C5 type SCR's which allow operation of the gate-to-cathode junction in reverse avalanche.

With increasing area of the semiconductor junctions in the SCR, however, negative gate bias has less effect. Unless $V_{(BR)FR}$ (with bias resistor) is specified, conservative circuit design practice should not depend on increasing $V_{(BR)FX}$ by negative gate biasing.

The improvement in dv/dt withstand capability that can be achieved by negative gate biasing is shown in Figure 4.6 for a typical C35 type SCR. It shows the effect of gate bias on the allowable time constant of application of forward blocking voltage without having the SCR switch on. The zero gate voltage curve corresponds to the time constant values given on the C35 specification sheet for the open gate condition. Figure 4.6 extends the usefulness of this information for different values of gate bias.

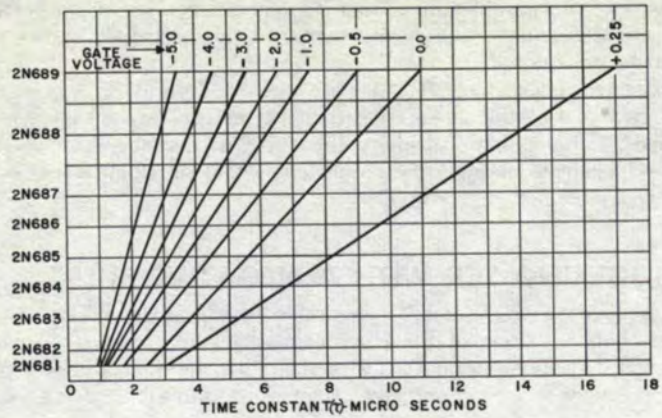


Figure 4.6 Effect of Gate Bias on Allowable Time Constant of Application of Forward Blocking Voltage

4.6 DURATION OF TRIGGER PULSE SIGNAL

The maximum gate signal necessary for triggering any SCR under the most adverse conditions (−65°C junction temperature) is given in the specification sheet in the form shown in Figure 4.1. There, for example, it is seen that for the C35 (2N681) series SCR no more than 80 ma at 3 volts are required to trigger every SCR of that specification at −65°C. This requirement assumes either a static (or DC) level of this magnitude, or a pulse of this magnitude with a certain minimum pulse width.

Figure 4.7 shows the increase in gate drive required for triggering five types of SCR's with trigger signals of short pulse duration. In order for the SCR to trigger, the anode current must be allowed to build up rapidly enough so that the latching current of the SCR is reached before the pulse is terminated. (Latching current may be assumed to be three times the value of the holding current given on the specification sheet). For highly inductive anode circuits it is, therefore, advisable to use a maintained type of trigger signal which assures gate drive until

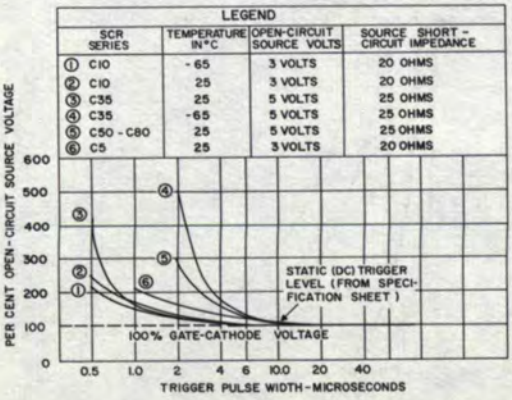


Figure 4.7 Gate Drive Required for Short Trigger Pulse Duration

latching current has been attained. Also, in certain rectifier and inverter circuits that require re-triggering, a square wave type of trigger circuit shown in Section 4.13.6 might be considered.

The DC gate trigger characteristics are measured on a 100% basis in production for all SCR's, but the pulse trigger characteristics are measured only on a sampling basis. For applications where the pulse trigger characteristics are critical, a special specification should be requested so that satisfactory pulse triggering will be assured.

4.7 TRIGGERING SCR WITH A NEGATIVE PULSE

Some applications may make it desirable to trigger an SCR with a negative pulse rather than with one of the conventional positive polarity. In low power level SCR circuits a diode connected in series with the SCR allows negative triggering conveniently and economically. Figure 4.8 shows this arrangement for a C5 type SCR.

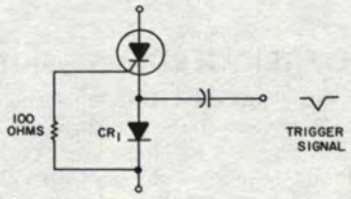


Figure 4.8 Negative Pulse Triggering

4.8 ANODE TURN-ON INTERVAL CHARACTERISTICS

Figure 4.9 shows the turn-on, or switching, characteristics of a typical C10 type SCR. It is representative of other SCR types as well. Per cent anode voltage is shown as a function of time, following application of the trigger signal at zero time, for switching from 500 volts and from 100 volts for two different circuit current levels.

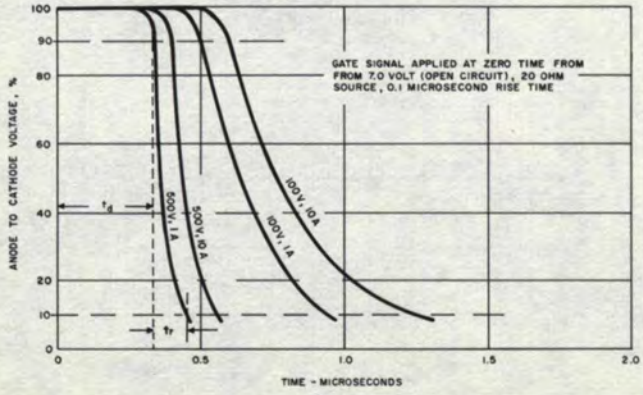


Figure 4.9 Typical Turn-On Characteristics of C10 Type SCR

Delay time t_d is shown for the 500 volt/1 ampere switching characteristic. It is defined as the time between the 10% point of the leading edge of the gate current pulse and the 10% point of the anode voltage waveform. The delay time decreases as the amplitude of the gate current pulse is increased, but approaches a minimum value of 0.2 to 0.5 μsec for gate current pulses of 500 ma or more.

Rise time t_r is defined as the time required for the anode voltage to drop from 90% of its initial value to 10%, as indicated for the 500 volt/1 ampere curve in Figure 4.9. The rise of current as the voltage across the SCR falls is determined largely by the circuit. In a purely resistive circuit the current will rise in the same manner as the voltage falls; hence the term rise time. It is important that the instantaneous voltage-current product during the turn-on interval not exceed the dissipation capability of the SCR. For this reason, the rate of rise of anode current (di/dt) must be limited in accordance with Section 3.7. Rise time, as well as delay time, tends to be reduced by a stiff gate drive within the allowable gate dissipation ratings of the SCR. Therefore, in order to minimize turn-on switching dissipation, the gate should be driven in the area of "preferred triggering" close to the allowable gate power dissipation curve shown in Figure 4.1.

Total turn-on time is defined as $t_{on} = t_d + t_r$. It is important to note that large turn-on switching dissipation can still occur after the termination of the turn-on time as defined above. Particularly, when switching from a high voltage into a large current, applicable switching ratings such as discussed in Section 3.7 should be consulted.

The jitter, or variation of switching time from one cycle to the next, is usually less than 2 mμsec at constant temperature if the gate is driven at two to three times the minimum amplitude required for triggering.

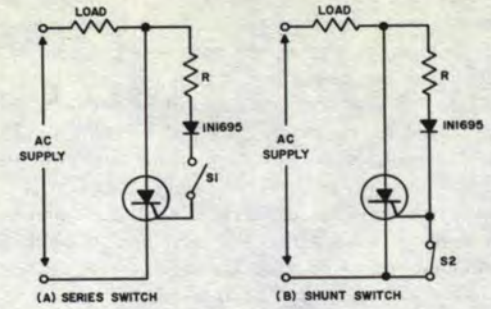
4.9 DC TRIGGERING

For simple on-off switching of SCR's in DC circuits, a continuous DC gate signal is satisfactory, provided that the gate power dissipation rating is not exceeded. With DC circuits separate means must be provided for turning off the SCR as described in Chapter 5. With AC circuits a continuous DC gate signal can also be used, provided that the considerations of Section 4.4 are taken into account.

4.10 SIMPLE RESISTOR AND RC TRIGGER CIRCUITS

It is sometimes required to find the simplest and most economical means for triggering an SCR when some performance compromise can be made, particularly with regard to repeatibility over a temperature range. The reader is referred to Reference 2 for a more detailed treatment of simple and low cost SCR trigger circuits.

Figure 4.10 shows a simple method of obtaining gate current for triggering the SCR from the main AC supply whenever the anode is positive with respect to the cathode. As soon as the SCR has triggered, the anode voltage drops to the conduction value and the gate current decreases to a low value. Resistor R limits the peak gate current. The diode in the gate circuit is provided to prevent reverse voltage from being applied between cathode and gate during the reverse part of the cycle. If desired, the diode can be connected between gate and cathode rather than in series with R. Conduction is initiated by closing contact S_1 in Figure 4.10(a) or by opening contact S_2 in Figure 4.10(b). Interruption of load current occurs within one-half cycle after opening S_1 or closing S_2 due to line voltage reversal.



(A) Series Switch (B) Shunt Switch

Figure 4.10 Half-Wave Static Switch

A very useful device for use as the switches S_1 and S_2 in Figure 4.10 is the reed switch. It consists of a set of contacts in a hermetically-sealed glass enclosure which can be actuated by a small magnetic field. Typical commercially available units have pick-up ampere-turns on the order of 50, with drop-out ampere-turns between 15 and 20. Since the reed switch also responds to small permanent magnets, static limit switch type operation can easily be effected.

Simple resistor-capacitor-diode combinations will trigger and control SCR's over the full 180 electrical degree range, giving very good performance at commercial temperatures. Since in a scheme of this type a resistor will usually have to supply all of the gate drive required to turn on the SCR, these types of circuits operate most satisfactorily with SCR's having fairly good gate sensitivities. The less sensitive the gate, the lower resistance must be the resistor, and the greater will have to be its wattage rating.

A very simple variable resistance half-wave circuit is shown in Figure 4.11. It provides phase retard from essentially zero (full on) to 90 electrical degrees of the anode voltage wave. Diode CR1 blocks reverse gate voltage on the negative half cycle of anode supply voltage. It must be rated to block at least the peak value of the AC supply voltage. The retard angle cannot be extended beyond the 90 degree point because the trigger circuit supply voltage and the trigger voltage producing the gate current to fire, I_{GF}, are in phase. When $e_{ac} = E_m$, at the peak of the AC supply voltage, the SCR can still be triggered with the maximum value of resistance between anode and gate. Since the SCR will trigger and latch into conduction the first time I_{GT} is reached, its conduction cannot be delayed beyond 90 electrical degrees with this circuit. This circuit, therefore, provides continuously variable control from the SCR full "on" (100% half-wave output) to the SCR half "on" (50% half-wave output).

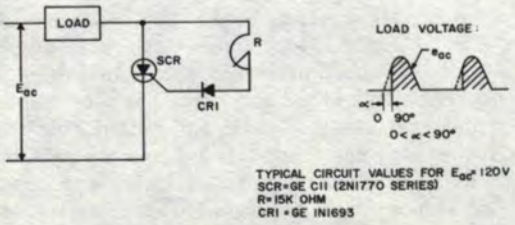


Figure 4.11 Simple Half-Wave Variable Resistor Phase Control (Limited Range of Control)

Figure 4.12 shows an R-C-Diode circuit giving full half-cycle control (180 electrical degrees). On the positive half-cycle of SCR anode voltage the capacitor will charge to the trigger point of the SCR in a time determined by the RC time constant and the rising anode voltage. On the negative half-cycle, the top plate of the capacitor charges to the peak of the negative voltage cycle through diode CR2, thus resetting it for the next charging cycle.

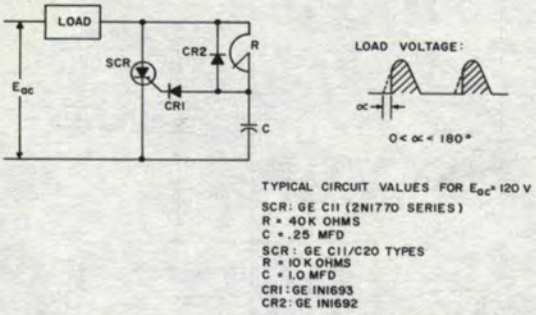


Figure 4.12 Simple Half-Wave RC-Diode Phase Control (Full 180° Control Range)

Figure 4.13 illustrates a slave circuit arrangement in which an independent half-wave circuit (SCR_2) is triggered on one half-cycle at a predetermined phase angle. On the following half-cycle the slave circuit will trigger SCR_1 at the same phase angle relative to that half-cycle. When SCR_2 does not trigger, capacitor C will charge and discharge to the same voltage at the same time constant. The voltage across C will not be sufficient to trigger SCR_1. As SCR_2 is triggered, capacitor C on discharging sees a time integral of line voltage that is different from the one on charging by the time integral of voltage appearing across the load. This action resets the capacitor to a voltage level related to the trigger delay angle of SCR_2. On the next half-cycle, when the anode of SCR_1 swings positive, it will trigger at the end of this delay angle.

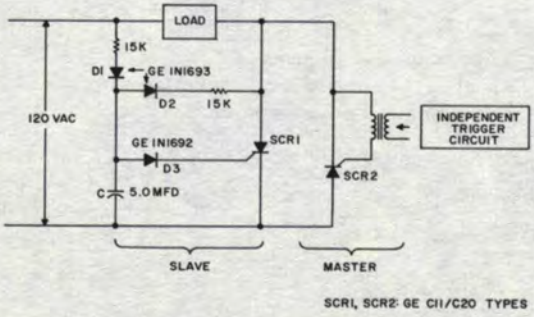


Figure 4.13 Three Terminal, Full Wave, RC-Diode Slaving Circuit For Full-Wave Phase Control

4.11 AC THYRATRON TYPE PHASE SHIFT TRIGGER CIRCUITS

Figure 4.14 illustrates a full-wave phase controlled rectifier employing an R-C or R-L phase shift network to delay the gate signal with respect to the anode voltage on the SCR's. Many variations of this type of phase shift circuit have been worked out for thyratrons.

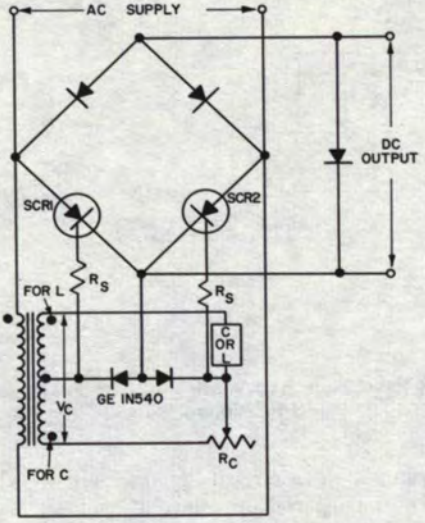


Figure 4.14 R-C or R-L Phase Shift Network Control of Single Phase Bridge Output

When using SCR's (C8, C10, C11, C35, C36, and C50 series), the following criteria should be observed to provide the maximum range of phase shift and positive triggering over the particular SCR's temperature range without exceeding the gate voltage and current limitations:

A. The peak value of V_c should be greater than 25 volts.

B. $\frac{1}{2\pi fC}$ or $2\pi fL \leq \frac{V_c}{2} - 9$

where C = capacitance in farads
L = inductance in henries
V_c = peak end-to-end secondary voltage of control transformer
f = frequency of power system

C. $R_s = \frac{V_c - 20}{0.2}$

where R_s = series resistance in ohms

D. $R_c \geq \frac{10}{2\pi fC}$ or $10\ (2\pi fL)$

Because of the frequency dependence of this type of phase shift circuit, the selection of adequate L or C components becomes easier at higher operating frequencies.

4.12 SATURABLE REACTOR TRIGGER CIRCUITS

Saturable reactors can provide a fairly steep wavefront of gate current together with a convenient means of control from a low level DC or AC signal. This type of control is adaptable to feedback systems and provides the additional advantage of multiple, electrically-isolated inputs and outputs for more complex circuits.

4.12.1 Continuously Variable Control

A typical half-wave magnetic amplifier type trigger circuit is shown in Figure 4.15. The gate signal for triggering the SCR is obtained from winding 3-4 of transformer T_1. When the core of T_2 is unsaturated, the winding 3-4 of T_2 presents a high impedance to the gate signal so that only a small voltage is developed across R_3. When the core of T_2 saturates, the impedance of winding 3-4 of T_2 decreases by several orders of magnitude so that a large voltage appears at the gate of the SCR, causing it to trigger. Resistor R_2 limits the gate current to the rated value and resistor R_3 limits the gate voltage produced by the magnetizing current of winding 3-4 of T_2 so that the SCR will not trigger before the core of T_2 saturates. Diode CR_2 serves the dual purpose of preventing a reverse voltage on the gate of the SCR and preventing any reverse current through winding 3-4 which would produce an undesired reset of the core T_2.

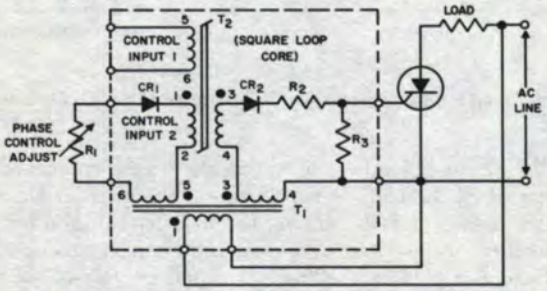


Figure 4.15 Typical Half-Wave Magnetic Trigger Circuit

Control signals can be applied to either input 1 or input 2 or both. Input 2 operates in the reset mode by controlling the reset voltage on winding 1-2 of T_2 during the negative half cycle. The setting of the potentiometer R_1 determines the amount of reset of the core during the negative half cycle, which in turn determines the phase angle of the SCR conduction during the positive half cycle. Other control circuits, such as a transistor amplifier stage, can be used in place of R_1. Since power is furnished by winding 5-6 of T_1, no auxiliary power supply is needed. Input 1 operates in the MMF (magnetomotive force) mode by controlling the current through the winding 5-6 and the core flux level, which in turn determines the trigger angle. The current for input 1 must be obtained from an external power supply or from a current generating type of transducer.

Additional output windings can be added to T_2 for triggering several SCR's in parallel or in series. Also, additional control windings of the reset or MMF type can be added to T_2. Full wave and multiple phase operation can be achieved by combining two or more half wave circuits.

4.12.2 On-Off Magnetic Trigger Circuits

Magnetic trigger circuits designed for phase control applications such as the one shown in Figure 4.15 require the use of saturable cores which are large enough to allow the output winding to sustain the gate voltage signal for a full half cycle without saturating. For simple on-off control applications, the magnetic trigger circuits shown in Figure 4.16 permit the use of smaller and less expensive cores since the output winding is not required to sustain the gate voltage signal for a full half cycle. In addition, these circuits have the advantage of not requiring the use of an auxiliary supply transformer.

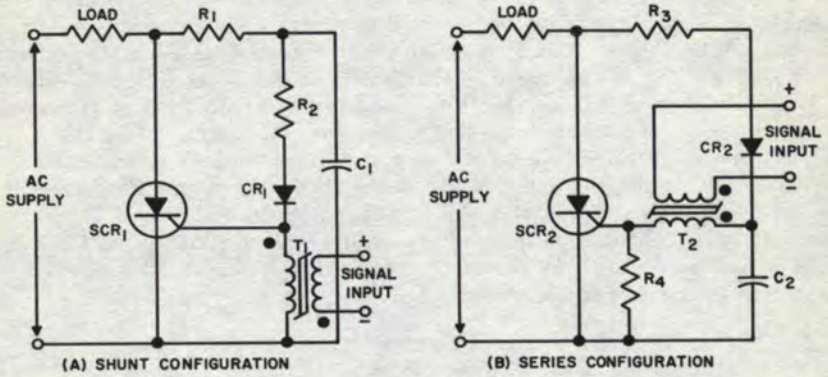


Figure 4.16 Half-Wave On-Off Magnetic Trigger Circuits

In Figure 4.16(a), one winding of saturable transformer T_1 is connected in shunt with the gate of SCR_1. If T_1 is unsaturated, the current through R_1, R_2 and CR_1 will flow into the gate of SCR_1 during the first part of the positive half cycle and cause SCR_1 to turn on. If T_1 is saturated, the current through R_1, R_2 and CR_1 will be diverted from the gate by the low saturated impedance of the winding on T_1. When T_1 is saturated it can be reset, and the SCR can be made to trigger by a positive voltage on the signal input. Capacitor C_1 provides filtering for the gate signal to prevent undesired triggering due to fast transients on the AC supply.

In Figure 4.16(b), one winding of saturable transformer T_2 is connected in series with capacitor C_2 and the gate of SCR_2. If T_2 is unsaturated the current through R_3 and CR_1 will charge C_2 during the initial part of the positive half cycle. T_2 will saturate after a few degrees of the positive half cycle and permit a rapid discharge of C_2 into the gate of SCR_2, thus causing SCR_2 to trigger. If T_2 is initially saturated at the beginning of the positive half cycle, the winding of T_2 will divert the current from C_2 and prevent C_2 from being charged. Resistor R_4 prevents the voltage at the gate of SCR_2 produced by the current through R_3 from exceeding the maximum gate voltage that will not trigger the SCR. When T_2 is saturated, it can be reset and the SCR can be made to trigger by a positive voltage at the signal input.

The circuits of Figure 4.16 permit the SCR to perform the function of an AC contactor with an isolated DC control winding. Modifications of these circuits permit full wave operation with normally open, normally closed or latching operation. The reader is referred to Chapter 7 for further discussion of static switching circuits.

4.13 UNIJUNCTION TRANSISTOR TRIGGER CIRCUITS

The silicon unijunction transistor is an ideal device for use in SCR trigger circuits. It has the advantages of a stable trigger voltage, a very low trigger current, operation over a wide temperature range and a peak emitter current rating of two amperes. SCR trigger circuits using the UJT (unijunction transistor) are simple and compact with low power consumption and a high effective power gain in phase control circuits.

The characteristics of the UJT which are most important in the design of SCR trigger circuits are described here. For further information on the UJT, see condensed specifications in the rear of this manual, or consult applicable specification sheets the UJT application notes 90.10, or Chapter 13 of the G-E Transistor Manual, Seventh Edition.

4.13.1 Unijunction Transistor Characteristics

The UJT has three terminals which are called the emitter (E), base-one (B_1), and base-two (B_2). Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. This resistance is called the interbase resistance (R_{BB}) and at 25°C has values in the range from 4.7K to 9.1K.

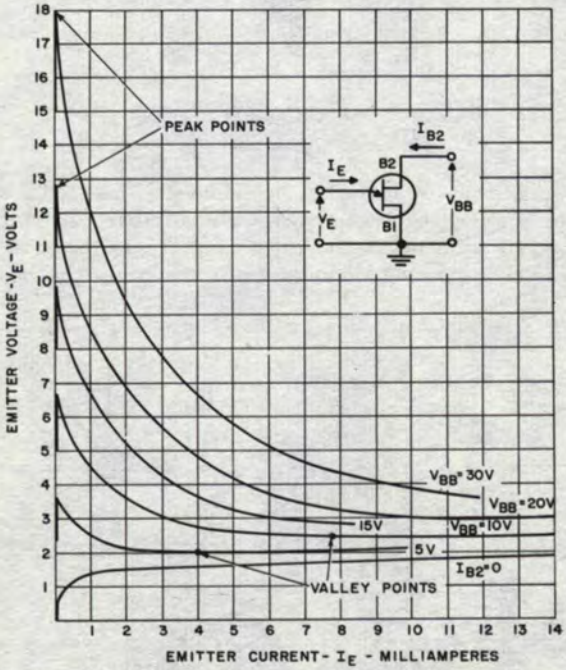


Figure 4.17 Unijunction Transistor Symbol and Emitter Input Characteristics

The normal biasing conditions for a typical UJT are indicated in Figure 4.17. If the emitter voltage, V_E, is less than the emitter peak point voltage, V_P, the emitter will be reverse biased and only a small reverse leakage current, I_{EO}, will

flow. When V_E is equal to V_P and the emitter current, I_E, is greater than the peak point current, I_P, the UJT will turn on. In the on condition, the resistance between the emitter and base-one is very low and the emitter current will be limited only by the series resistance of the emitter to base-one circuit.

The peak point voltage of the UJT varies in proportion to the interbase voltage, V_{BB}, according to the equation:

$$V_P = \eta V_{BB} + V_D \tag{4.1}$$

The parameter η is called the intrinsic standoff ratio. The value of η lies between 0.51 and 0.82, and the voltage V_D, the equivalent emitter diode voltage, is in the order of .5 volt at 25°C, depending on the particular type of UJT. It is found that V_P decreases with temperature, the temperature coefficient being about -3mv/°C for the 2N2646-47 (-2mv/°C for 2N489 series). The variation of the peak point voltage with temperature may be ascribed to the change in V_D (also η for 2N2646-47 series). It is possible to compensate for this temperature change by making use of the positive temperature coefficient of R_{BB}. If a resistor R_{B2} is used in series with base-two as shown in Figure 4.18, the temperature variation of R_{BB} will cause V_{BB} to increase with temperature. If R_{B2} is chosen correctly, this increase in V_{BB} will compensate for the decrease in V_P in Equation 4.1. Over a temperature range of -40°C to 100°C Equation 4.3(a) gives an approximate value of R_{B2} for the majority of 2N2646 and 2N2647 UJT's. Equation 4.3(b) gives R_{B2} for the 2N489 MIL series, 2N1671A and B, and the 2N2160.

$$R_{B2} \approx \frac{10000}{\eta V_1} \tag{4.3a}$$

$$R_{B2} \approx \frac{0.40 R_{BB}}{\eta V_1} + \frac{(1-\eta) R_{B1}}{\eta} \tag{4.3b}$$

For a more detailed discussion of the characteristics of the various types of UJT's the reader is referred to Reference 8. Quantitative data and techniques for temperature compensation on an individual and general basis in very high performance circuits over extreme temperature ranges are discussed in Reference 9.

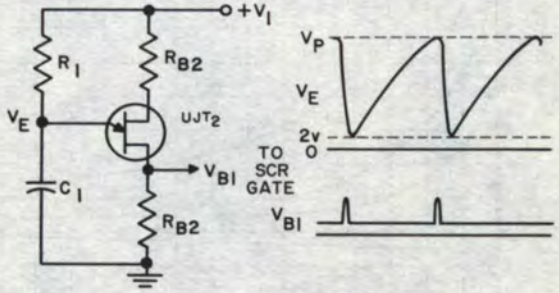


Figure 4.18 Basic Unijunction Transistor Relaxation Oscillator-Trigger Circuit with Typical Waveforms

4.13.2 Basic UJT Pulse Trigger Circuit

The basic UJT trigger circuit used in applications with the SCR is the simple relaxation oscillator shown in Figure 4.18. In this circuit, the capacitor C_1 is

charged through R_1 until the emitter voltage reaches V_P, at which time the UJT turns on and discharges C_1 through R_{B1}. When the emitter voltage reaches a value of about 2 volts, the emitter ceases to conduct, the UJT turns off and the cycle is repeated. The period of oscillation, T, is fairly independent of the supply voltage and temperature, and is given by:

$$T = \frac{1}{f} \approx R_1 C_1 \ln \frac{1}{1-\eta} = 2.3 R_1 C_1 \log_{10} \frac{1}{1-\eta} \qquad (4.4)$$

Figure 4.19 shows a nomogram for solution of Equation 4.4 for an assumed intermediate value of intrinsic standoff ratio of $\eta = 0.62$.

The design conditions of the UJT firing circuit are very broad. In general, R_{B1} is limited to a value below 100 ohms although values up to 2 or 3K are possible in some applications. The resistor R_1 is limited to a value between 3K and 3 Meg. The lower limit on R_1 is set by the requirement that the load line formed by R_1 and V_1 intersect the emitter characteristic curve of Figure 4.17 to the left of the valley point, otherwise the UJT in Figure 4.18 will not turn off. The upper limit on R_1 is set by the requirement that the current flowing into the emitter at the peak point must be greater than I_P for the UJT to turn on. The recommended range of supply voltage V_1 is from 10 volts to 35 volts. This range is determined on the low end by the acceptable values of signal amplitude and at the high end by the allowable power dissipation of the UJT.

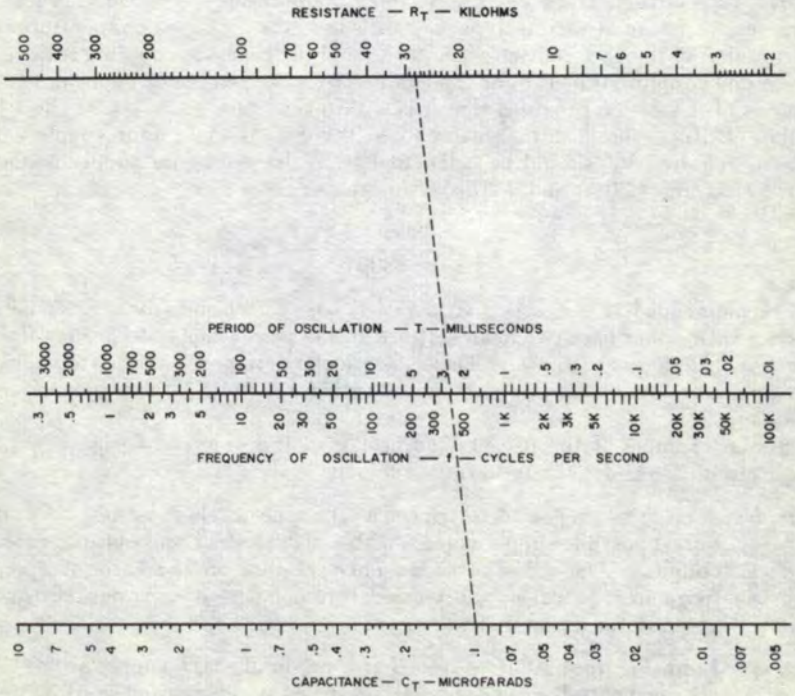


Figure 4.19 Nomogram for Determining Frequency or Period of UJT Relaxation Oscillator

If the pulse output (V_{B1}) of the circuit of Figure 4.18 is coupled directly, or through series resistors, to the gates of the SCR's, the value of R_{B1} should be low enough to prevent the DC voltage at the gate due to interbase current from exceeding the maximum voltage that will not trigger the SCR's (see Figure 4.1) V_{GT} (max) at the maximum junction temperature at which the SCR's are expected to operate. To meet this criterion, R_{B1} should be chosen in accordance with the following inequality:

$$\frac{R_{B1}\ V_1}{R_{BB}\ (\text{min}) + R_{B1} + R_{B2}} < V_{GT\ (\text{max})} \tag{4.5}$$

For the C35 (2N681) types at a maximum junction temperature of 125°C, V_{GT} (max) is 0.25 volt, hence for a supply voltage of 35 volts or less, R_{B1} should be 50 ohms or less. If the pulse output from the UJT firing circuit is coupled to the gates of the SCR's by means of transformers or capacitors, these limitations do not apply.

4.13.2.1 Designing the Unijunction Transistor Trigger Circuit

The type 2N2646 and 2N2647 UJT's are specifically characterized for SCR trigger circuits and are factory tested to ensure reliable operation with all types of G-E SCR's over their respective temperature ranges. Their condensed specifications are given in Chapter 20.

The design of a suitable UJT trigger circuit can be achieved rapidly and easily by using the design curves given in Figures 4.20(a) and 4.20(b) for the 2N2646 and 2N2647, respectively. These curves give the minimum supply voltage V_1 required to guarantee triggering of various types of SCR's over the indicated temperature range as a function of the UJT emitter capacitor C_1 and the base-one coupling resistor R_{B1} or base-one coupling transformer. The value of resistor R_1 is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. If R_{B2} is significantly greater than 100 ohms the minimum supply voltage which is required V_1' should be calculated from the minimum supply voltage V_1 given by Figures 4.20(a) and 4.20(b) using the equation:

$$V_1' = \frac{(2200 + R_{B2})\ V_1}{2300} \tag{4.6}$$

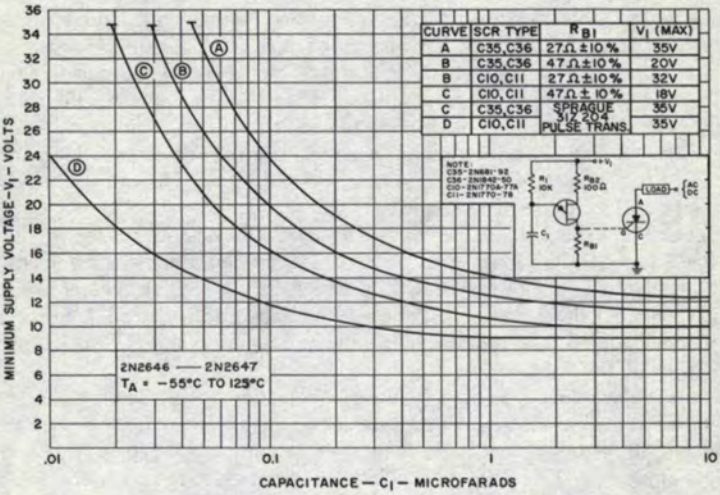
It is recommended in all cases that a resistance of 100 ohms or greater be used in series with either base-two or in series with the power supply to protect the UJT from possible thermal runaway. This is particularly important when operating at high ambient temperatures, at high supply voltages, or with large values of emitter capacitance.

As an example of the use of Figure 4.20 in the practical design of an SCR trigger circuit, consider the following problem:

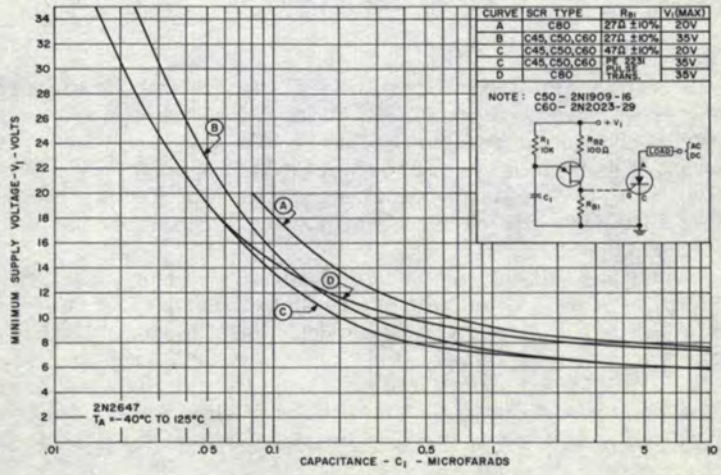
Example: A circuit is required to trigger a C11 type (2N1773 series) SCR at the lowest possible supply voltage with a 2N2646 UJT and pulse transformer coupling. The value of capacitance, chosen on the basis of operating frequency, is 0.1 μf, and temperature compensation is desired. Assume $\eta = 0.66$ for a nominal value.

Solution: From Figure 4.20(a) we see that a minimum UJT supply voltage V_1 is obtained with $R_{B1} = 47$ ohms (i.e., curve C lies below curve B). On curve C the minimum voltage for a value of $C_1 = 0.1$ μf is $V_1 = 16$ volts. This is below the maximum allowable voltage V_1 (max) = 18 volts found in the

chart on Figure 4.20(a). (If we select $V_1 > V_1$ (max) the SCR may trigger by the DC voltage across R_{B1} at elevated temperatures). The value for R_{B2} is determined from Equation 4.3(a) as $R_{B2} \approx \frac{10000}{(.66)(16)} = 950 \approx 1000$ ohms (nearest standard value). With this value of R_{B2} the supply voltage must be increased to a value V_1' in accordance with Equation 4.6 or $V_1' = \frac{(2200+1000)}{2300}(16) \approx 22$ volts. Thus, a suitable design for this example would be $C_1 = .1\ \mu f$, $R_{B2} = 1$ k ohms; $R_{B1} = 47$ ohms $\pm 10\%$ and $V_1' = 22$ volts.



(a) Low and Medium Current SCR's With 2N2646 and 2N2647



(b) High Current SCR's With 2N2647

Figure 4.20 UJT Trigger Circuit Design Curves

If, in the case of the 2N2646 and 2N2647 UJT's, R_{B2}, as determined from Equation 4.3(a) causes V_1' (from Equation 4.6) to be larger than can be attained practically or economically, the use of the 2N489 series, the 2N1671A or the 2N-1671B is suggested. (Equation 4.3(b) yields a lower value of R_{B2}); alternatively, if extreme temperature compensation is not required, or if the temperature range to which the 2N2646/47 UJT's are subjected is not great, a value of $R_{B2} \geq 100$ ohms may be used.

4.13.2.2 Triggering Parallel-Connected SCR Gates

If the load on the UJT trigger circuit consists of two or more SCR gates in parallel, it is desirable to prevent a low resistance gate from loading the output to such an extent that the other SCR's may not trigger. To reduce this possibility it is recommended that the trigger pulse be coupled by means of a separate capacitor to each SCR gate. These capacitors act to equalize the charge coupled to each gate during the trigger pulse and thus tend to reduce the effects of unequal loading. The optimum value of capacitor for this purpose has been found to be 0.1 μf. In addition to this capacitor, a resistor having a value of 220 Ω to 1K should be connected between gate and cathode of each SCR.

Using this approach of equalizing capacitors the design curves of Figure 4.20 can be used for parallel triggering of SCR's provided that the minimum supply voltage is multiplied by a factor of 1.50 if two SCR's are to be triggered in parallel, and by a factor of 1.80 if three SCR's are to be triggered in parallel. Since the gates are not direct coupled, the maximum supply voltage allowed is limited only by the 35 volt rating of the UJT.

Alternatively, a larger value of base-one resistance, R_{B1}, can be used to reduce the otherwise required increase in value of supply voltage for parallel triggering. For example, if $R_{B1} = 100$ Ω, and using equalizing capacitors, the curves for $R_{B1} = 27$ Ω apply for triggering two SCR's in parallel with no increase in supply voltage. For triggering three SCR's in parallel under this condition the supply voltages given by these curves should be increased by a factor of 1.25.

4.13.2.3 Synchronization Methods

In the basic trigger circuit of Figure 4.18, the UJT can be triggered at any intermediate part of the cycle by reducing either the interbase voltage or the supply voltage, V_1. This results in an equivalent decrease in V_P in accordance with Equation 4.1 (or 4.3) and causes the UJT to trigger if V_P drops below the instantaneous value of V_E. Thus, the base-two terminal or the main supply voltage can be used to synchronize the basic trigger circuit. Figure 4.20(A) illustrates the use of a negative synchronizing pulse at base-two.

Another synchronization method is illustrated in Figure 4.21(B). An NPN transistor, Q_2, is used in shunt with the emitter capacitor C_1. A positive current pulse at the base of Q_2 will discharge C_1 and delay the triggering of the UJT Q_1. This circuit can also be used for clamping the voltage at the emitter of the UJT. As long as a positive current is maintained into the base of Q_2, no voltage will be developed across C_1. When the base current is removed, the voltage across C_1 will rise and the UJT will trigger at the end of the time interval determined by the values of R_1 and C_1.

Two methods of achieving synchronization with the AC line are illustrated in Figure 4.22. A full wave rectified signal obtained from a rectifier bridge or a similar

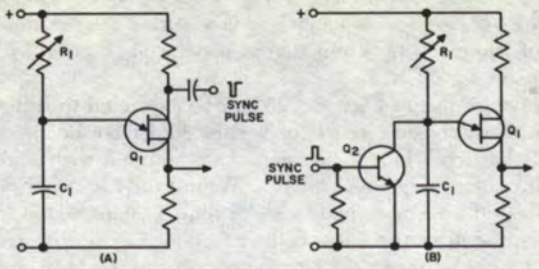


Figure 4.21 Circuits for Pulse Synchronization of UJT Relaxation Oscillator

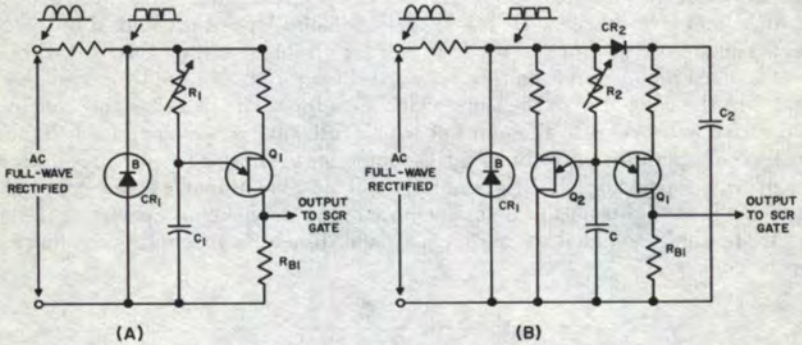


Figure 4.22 Circuits for Synchronization to AC Line

source is used to supply both power and a synchronizing signal to the trigger circuit. Zener diode CR_1 is used to clip and regulate the peaks of the AC as indicated in Figures 4.22(a) and (b).

At the end of each half-cycle the voltage at base-two of Q_1 and Q_2 will drop to zero, causing Q_1 and Q_2 to trigger. The capacitors are thus discharged at the beginning of each half cycle and the trigger circuits are thus synchronized with the line. In Figure 4.22(A) a pulse is produced at the output at the end of each half cycle which can cause the SCR to trigger and produce a small current in the load. If this is undesirable, a second UJT can be used for discharging the capacitor at the end of the half cycle as illustrated in Figure 4.22(b). Diode CR_1 and capacitor C_2 are used to supply a constant DC voltage to Q_1. The voltage across Q_2 will drop to zero each half-cycle causing C_1 to be discharged through Q_2 rather than through the load R_{B1}. The UJT's should be chosen so that Q_2 has a higher standoff ratio than Q_1.

4.13.3 UJT Trigger Circuits For Simple Manual Control

The basic unijunction transistor trigger circuit was discussed in Section 4.13.2. A simplified type of trigger circuit results if base two and the emitter timing circuit of the UJT are supplied directly from the line by way of a dropping resistor R_D which keeps the peak voltage on the UJT within its specifications.

Figure 4.22 shows such a circuit with values given for operation from a 120 VAC supply. The voltage across capacitor C will rise to a value determined by the time constant of the circuit. When it reaches the peak point voltage the UJT will trigger and turn on the SCR.

The half-wave circuit of Figure 4.23 can be extended to full-wave operation. In Figure 4.24 two of the basic circuits of Figure 4.23 have been placed back-to-back. The emitters of the two UJT's have been cross-coupled with a network that exerts full cycle phase control over both SCR's. Where only manual control is required, this circuit trades off a pulse transformer and an avalanche diode for an additional low cost UJT compared to the basic full-wave UJT circuit discussed earlier.

Figure 4.25 gives a lower cost version of a full-wave UJT circuit with only one UJT but requires a center-tapped potentiometer P and a double-pole-double-throw switch DPDT. With DPDT in the "dotted" position, potentiometer P can be turned up to lower resistance values until the SCR triggers for a full half-cycle. Diode CR_1 resets the voltage on capacitor C to essentially zero. Continuing the travel of the potentiometer arm throws DPDT into the "solid" position and simultaneously inserts sufficient resistance in the UJT emitter circuit to cut off the SCR. Diode CR_1 now bypasses all negative half-cycles to the load and also continues to reset the voltage on the capacitor to the same value as before. The SCR has full control over the positive half-cycles to the point at which full wave power is applied to the load. This type of operation introduces a DC component into the supply lines inherent in all half-wave operation. It will generally not be objectionable whenever the total connected load of this nature is small compared to the normal capacity of the supply line. It should be avoided when driving loads subject to magnetic core flux saturation.

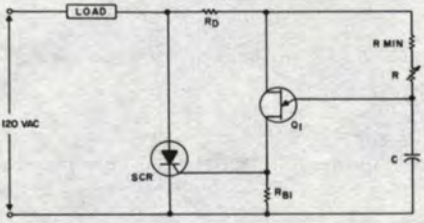


Figure 4.23 Simplified Unijunction Transistor Trigger Circuit

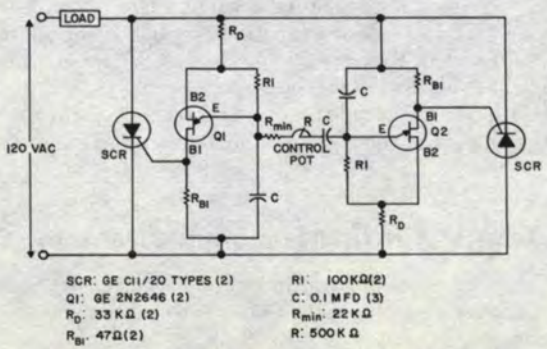


Figure 4.24 Simplified Full-Wave UJT Trigger Circuit

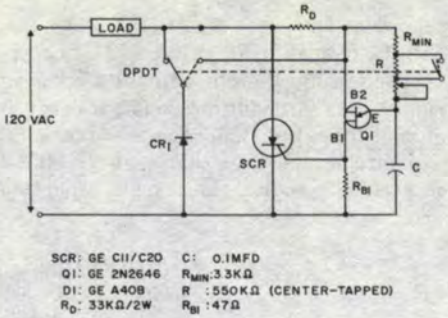


Figure 4.25 Simplified UJT Circuit with Auxiliary Diode and Switch for Full-Wave Operation

4.13.4 UJT Trigger Circuits With Transistor Control

The UJT trigger circuits shown in Section 4.13.3 are simple manual on-off or phase-control control circuits. UJT trigger circuits are also ideally suited for remote and closed loop control by a transistor stage.[3] Phase control circuits can be obtained by using a p-n-p or n-p-n transistor in series or in shunt with the emitter capacitor of the UJT trigger circuit. The amount of current in the base of the transistor will control the effective charging current to the capacitor and hence will control the trigger angle of the UJT and SCR. The subject of phase control and associated UJT trigger circuits is discussed in Chapter 8.

4.13.4.1 Shunt Transistor Control of UJT

Referring to the circuit of Figure 8.12 in Chapter 8, it is seen that n-p-n transistor Q_2 shunts some of the charging current supplied to capacitor C_1 by resistor R_2 in an amount dependent on the base drive of Q_2. The more Q_2 is turned on, the later UJT will trigger, and the lower the output of the SCR's will be.

By fixing the value of R_2 at approximately 2500 Ω, base current i_B will then control the diversion of charging current from C_1 and retard or advance the trigger angle accordingly. The UJT will be prevented from triggering, and essentially zero output will occur across the load, if i_B (in amperes) is increased to approximately the following value:

$$i_B \geq \frac{V_1}{(\beta)(R_2)}(1-\eta) \quad \text{if} \quad \frac{1}{2f(R_2)(C_1)} > 4$$

where V_1 = avalanche voltage of CR_5
β = common emitter current gain of Q_2
η = intrinsic standoff ratio of Q_1
C_1 = UJT capacitor (farads)

For values of i_B less than this value, the SCR output increases rapidly. This type of shunt transistor control of the UJT and SCR trigger angles is characterized by very high gain. Power gain between the base drive of Q_2 and the load on the order of 10^8 is readily attainable.

4.13.4.2 Series Transistor Control of UJT

For a more linear transfer characteristic at the expense of power gain, a transistor in series with C_1 instead of in shunt with it can be used to regulate the charging rate of this capacitor and thereby control the trigger angle. Such a trigger circuit is shown in Figure 4.26. An additional npn transistor Q_3 is required if it is desired to keep one side of the input signal at the potential of the lower line. If the resistors in this circuit are selected so that both Q_3 and Q_4 operate as heavily degenerative common emitter circuits, the transfer characteristic can be approximated as follows:

$$\frac{e_o}{e_{max}} = \frac{1}{2} + \frac{1}{2}\cos\frac{2\pi f \eta (V_1)(C_1)(R_6)(R_4)}{(R_5)(V_2)}$$

where e_o = average value of voltage across load

e_{max} = maximum theoretical average value of voltage across load when no triggering angle delay occurs

f = supply frequency, cps

Zero output voltage across the load will occur when:

$$V_2 = \frac{2f\eta(V_1)(C_1)(R_6)(R_4)}{(R_5)}$$

These types of trigger angle control using the UJT can be used to regulate the output of SCR's in many other phase-controlled circuits, examples of which are shown in Chapter 8.

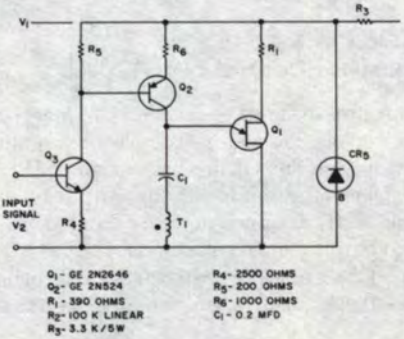


Figure 4.26 Series Transistor Control of UJT Trigger Angle

4.13.4.3 Reversing UJT Control Circuit

A basic circuit for a reversing type control is shown in Figure 4.27. This circuit shows the voltage reference as ground, but a variable reference voltage may also be used. The circuit is designed in such a way that for any value of input voltage only one of the UJT's can trigger during a half cycle. If the SCR's are used in a full-wave bridge, the UJT which triggers will determine the phase angle and the direction of current flow through the load. If the input voltage is reversed in polarity, the opposite UJT will trigger and the current will flow through the load in the opposite direction.

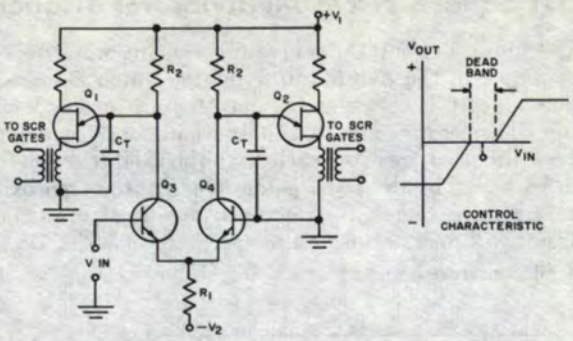


Figure 4.27 Basic Control Circuit for Reversing Type Application

For suitably small values of input voltage, the output from the circuit will be zero since the triggering of both UJT's will be delayed for more than a half cycle. The width of this "dead band" can be chosen as desired by means of properly selecting the component values in Figure 4.27. The dead band can be increased by means of R_1, increasing R_1.

4.13.5 On-Off Type Control Circuits

In some types of applications, an on-off type of control is required rather than a linear control. A circuit which gives this characteristic is shown in Figure 4.28. As the capacitor C_T is charged, either UJT Q_1 or Q_2 will trigger, depending on which one has the lower peak point voltage. The peak point voltage of the two units is varied by controlling the interbase voltages with the differential amplifier as shown. For the circuit shown in Figure 4.28, the UJT which triggered could be controlled by an input voltage change of 4 millivolts. The temperature stability is very good since the circuit is completely symmetrical.

The capacitors C_1 and C_2 are required to prevent one UJT from triggering the other with the pulses developed across the power supply impedance. If these capacitors are eliminated, both UJT's can trigger at the same time and, as the input voltage is varied, the pulse amplitude for one UJT will increase as the pulse amplitude for the other UJT decreases. This would be a serious problem if a reversing type control was used.

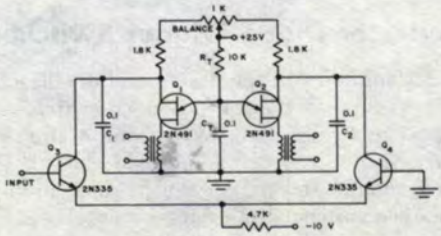


Figure 4.28 On-Off Type Control Circuits

4.13.6 UJT Square Wave Multivibrator Trigger Circuit

Figure 4.29 shows a circuit for generating a square wave for two outputs. This circuit is an example of the hybrid multivibrator which is described fully in the UJT application notes.[4] Transistors Q_2 and Q_3 form a simple flip-flop which is triggered by the UJT operating as a relaxation oscillator. Negative trigger pulses are generated across the 15 Ω resistor each time the UJT triggers. The frequency of oscillation can be varied by the 100K potentiometer from approximately 20 cps to 600 cps. The waveform remains perfectly symmetrical over the full frequency range. The circuit will operate up to a temperature of 75°C. Higher temperatures are possible if silicon transistors are used for Q_2 and Q_3.

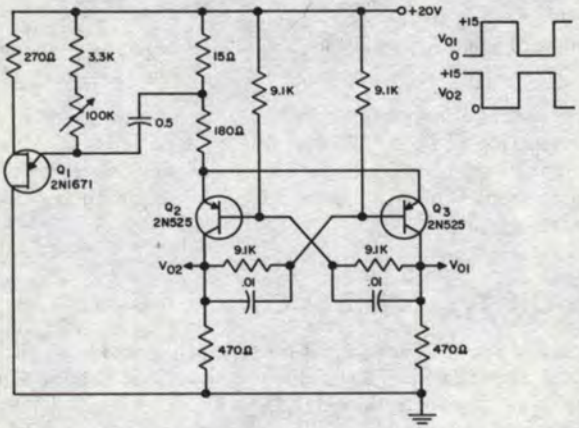


Figure 4.29 UJT-Multivibrator for Generating Square Waves

4.14 TRIGGER DIODE AND NEON LAMP TRIGGER CIRCUITS

Low power level devices exhibiting a negative resistance switching characteristic can be used to trigger SCR's. Of interest in this category are three-, four-, and five-layer semiconductor diode switches and neon lamps. The tunnel diode (negative conductance device) can also find application as an SCR trigger device, although it may be necessary to employ an impedance matcthing transformer. An example using a germanium tunnel diode is shown in Figure 7.12.

4.14.1 Semiconductor Diode Trigger Switches

Due to the flexibility inherent in the design and manufacture of three-, four-, and five-layer p-n devices different types of specified switching characteristics can be obtained as illustrated in Figure 4.30. When one of these types of devices is interposed between a charged capacitor and an SCR gate, its switching action will cause the capacitor to discharge and trigger the SCR. Switching is initiated at the device's specified breakover voltage $V_{(BR)}$ and current $I_{(BR)}$. The circuit may be designed to trigger the SCR on a limited amount of voltage swing after switching (Figures 4.30(a) and (c)); or it may be designed to trigger on an almost complete (to within about 1 volt) switch-down of voltage (Figure 4.30(b)). The greater the volt-

age swing on switching and the faster the switching action, the more of the energy stored in the capacitor will be transferred to the SCR gate.

If the trigger diode has a bilateral characteristic (Figure 4.30(c)) in which $V_{(BR)} \approx V'_{(BR)}$, a single such device can be used to trigger a pair of parallel-inverse connected SCR's in a full-wave phase-control circuit. This arrangement is shown in Figure 4.31 for a trigger diode having $V_{(BR)} \approx V'_{(BR)} = 27$ volts and a voltage swing of about six volts up to 10 ma. Switching currents $I_{(BR)}$ and $I'_{(BR)}$ are in the order of a few hundred microamperes.

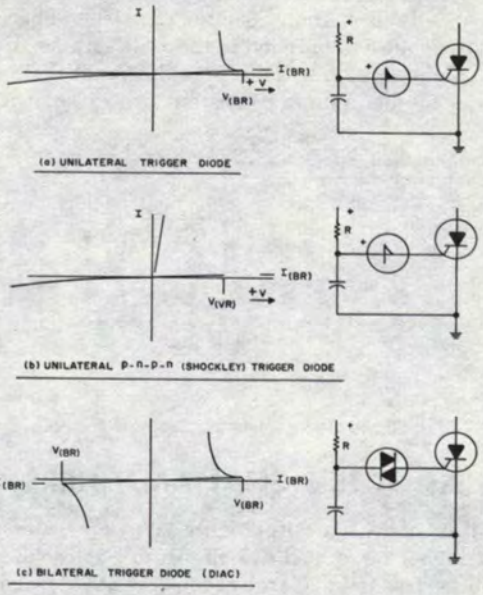


Figure 4.30 Types of Specified Characteristics of Trigger Diodes and Their Connections

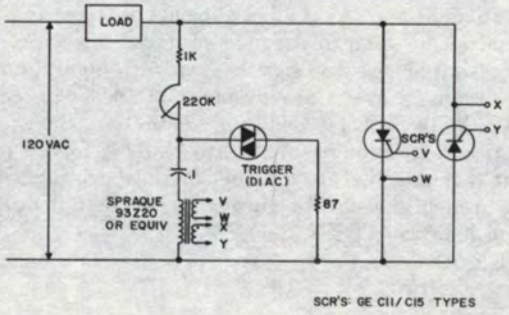


Figure 4.31 Single-Bilateral Trigger Diode in Full-Wave SCR Circuit

4.14.2 Neon Lamp as SCR Trigger

The neon lamp has a bilateral switching characteristic similar to that shown in Figure 4.30(c). Properly specified, it can be used to trigger SCR's in circuitry similar to that shown in Figure 4.31.[5]

Figure 4.32 shows a full-wave phase control circuit in which the transformer shown in Figure 4.31 has been functionally replaced by an RC coupling network. A disadvantage of this approach, however, is its susceptibility to spurious triggering from line transients.

The neon lamp will trigger whenever its ignition voltage is reached (usually between 60-100 volts depending on its specification). Triggering at lower circuit voltage is possible with a series capacitor pre-biasing technique shown in Figures 8.26 and 8.27. On triggering, the neon lamp will switch to its lower sustaining voltage and thereby partially discharge capacitor C1. Depending on the polarity of the line voltage, a positive pulse is supplied to the SCR with positive anode voltage thus triggering it into conduction. A metallic shield around the neon lamp is shown in Figure 4.32 in order to obtain more consistent triggering of the device.

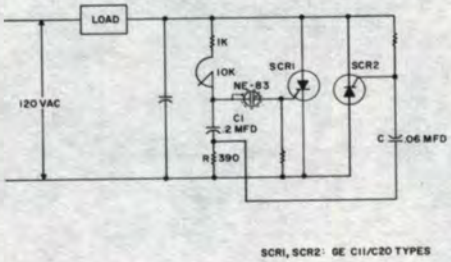


Figure 4.32 Single Neon Lamp RC-Coupled Full-Wave SCR Circuit

4.15 SCR'S AS GATE SIGNAL AMPLIFIERS

The availability of SCR's with highly sensitive gates permits use of these devices to trigger higher rated SCR's as shown in Figure 4.33. Here, for example, a C5B as SCR_1 requires less than 200 microamperes of gate signal to trigger. Current then flows through R_2, SCR_1, and into the gate of SCR_2. When the current reaches the triggering requirements of SCR_2, this device turns on and shunts the main power away from SCR_1. In addition to providing a means of triggering high current SCR's by low level signals from high impedance sources, this type of triggering yields positive triggering from pulsed gate signals even with highly inductive loads due to the much lower latching current requirements of the C5 in comparison with the higher rated SCR's. With SCR_1 latched into conduction, the gate of SCR_2 is driven by a trigger signal which is maintained until SCR_2 is forced into conduction. R_2 limits the current through SCR_1 to a value within its rating. SCR_1 must meet the same voltage requirements as SCR_2. However, its current duty is generally of a pulsed nature, and hence negligible.

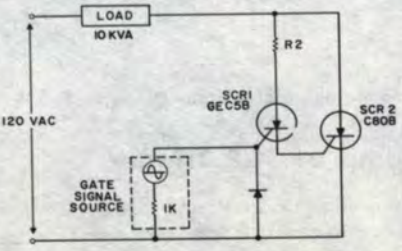


Figure 4.33 Use of C5 as a Gate Signal Amplifier

Depending on the nature of the control input signal other types of SCR's can be considered for triggering larger SCR's. The LASCR (Chapter 11) can be used where direct triggering by light is required. Also, the LASCR in conjunction with a suitable light source provides a simple way in which to obtain electrical isolation in SCR control circuitry.

4.16 TRANSISTOR BLOCKING OSCILLATOR TRIGGER CIRCUIT

The transistor blocking oscillator is a very useful SCR trigger circuit. In its astable (free-running) mode its output is a burst of pulses at a frequency high compared to the frequency at which the SCR is triggered. In this manner the circuit provides the SCR with a gate drive that can be maintained sufficiently long to assure reliable triggering with inductive loads. The circuit also operates from a DC input signal such as available from an amplifier output. Furthermore, the circuit provides electrical isolation between the control and SCR power circuitry.

Figure 4.34 shows a simple astable blocking oscillator. Diode CR1 is shown to indicate a method of obtaining control over the output. If CR1 is reverse biased, the oscillator free-runs at a frequency determined largely by the volt-second capability of the transformer core and R_1 C_1. When CR1 is forward biased (V_{in} slightly negative), the initial base drive necessary to initiate conduction of transistor Q_1 is diverted, and the circuit ceases to oscillate. Initially, when the circuit is energized, or when the circuit is released at CR1, a small forward bias at the base of Q_1 causes an increase in collector current. Core flux in the transformer starts to change, and the winding in the base of Q_1 provides additional forward base drive. Transistor Q_1 switches regeneratively into saturation, resulting in efficient switching action and giving a fast rise time leading edge of the output pulse. During its transformation interval the transformer winding in the collector circuit supports essentially the entire supply voltage, and an output pulse is available at the secondary winding(s) of an approximate duration $t_p = \frac{N}{E}\Delta\Phi$, where N = number of primary turns, E = supply voltage, and $\Delta\Phi$ is the total effective flux swing available in the core. As the transformer core flux begins to enter saturation, the rate of flux change diminishes, and, as a result, the base drive to Q_1 is reduced. Transistor Q_1 rapidly comes out of saturation and collector current starts to fall. Accordingly, core flux starts to change in the opposite direction. This reversal of

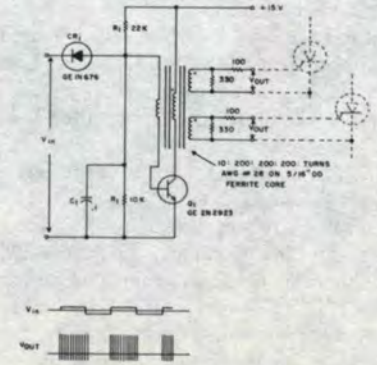


Figure 4.34 Blocking Oscillator Trigger Circuit

the rate of change of core flux induces a voltage in the negative direction: the output pulse is terminated, and Q_1 is restored to its blocking state as the full supply voltage appears across Q_1. While Q_1 is off, a forward bias for the emitter junction of Q_1 builds up across capacitor C_1 due to current provided by resistor R_1, and the cycle is repeated.

The component values shown in Figure 4.34 give an operating frequency of 11 kc/sec, an approximate pulse width of $t_p = 20$ μsec, and make the circuit suitable for triggering, for example, two C20 type SCR's at −25°C or two C35 type SCR's at 25°C. When increased output is desired a larger transformer core with greater volt-second capability may be considered. The circuit can readily be designed for use of p-n-p transistors. For a more complete treatment of blocking oscillator design and various modes of operation the reader is referred to the literature. Although by no means complete, References 7 (page 492–498), 10, and 11 provide design information and further literature references for linear and saturating transformer blocking oscillator designs.

The unijunction transistor relaxation oscillator described in Section 4.13.2 also functions basically as a free-running oscillator giving a burst of output pulses as long as supply voltage V_1 (Figure 4.18) is a pure direct voltage and the design conditions of oscillation are met. The UJT trigger circuit lends itself particularly well to external control (Sections 4.13.3 and 4.13.4) and line synchronization (Section 4.13.2). However, the UJT circuit single output pulse is usually of short effective duration (2 to 5 μseconds), whereas the transistor blocking oscillator single pulse width can be readily varied by circuit design.

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Turn-Off Characteristics And Methods

5.1 TURN-OFF CHARACTERISTICS

If forward voltage is applied to an SCR too soon after anode current ceases to flow, the SCR will go into the conduction state again. It is necessary to wait for a definite interval of time after cessation of current flow before forward voltage can be reapplied. Chapter 1 describes the physical reasons for this required interval.

To measure the required interval, the SCR is operated with current and voltage waveforms shown in Figure 5.1. The interval between t_3 and t_8 is then decreased until the point is found when the SCR will just support reapplied forward voltage.

This interval is not a constant, but is a function of several parameters. Thus, the minimum time t_3 to t_8 will increase with:

1. An increase in junction temperature.
2. An increase in forward current amplitude (t_1 to t_2).
3. An increase in the rate of decay of forward current (t_2 to t_3).
4. A decrease in peak reverse current (t_4).
5. A decrease in reverse voltage (t_5 to t_7).
6. An increase in the rate of reapplication of forward blocking voltage (t_8 to t_9).
7. An increase in forward blocking voltage (t_9 to t_{10}).
8. An increase in external gate impedance.
9. A more positive gate bias voltage.

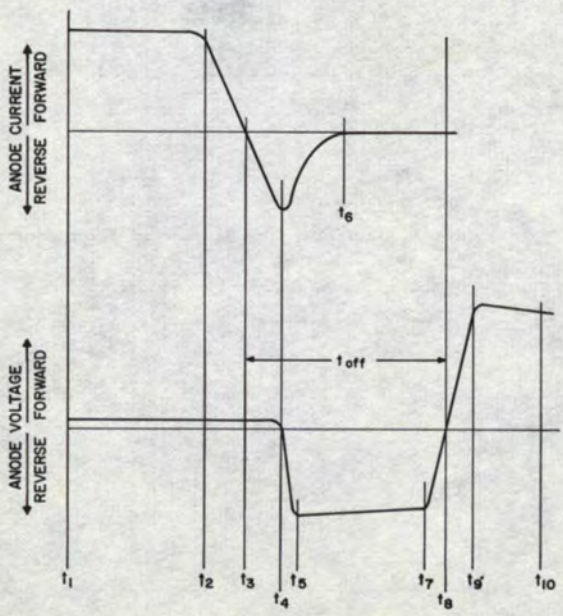


Figure 5.1 SCR Waveform for Turn-Off Time Measurements

5.1.1 SCR Turn-off Time (t_{off})

The turn-off time of an SCR is defined as the shortest interval between the time (t_3) when forward current reaches zero and the time (t_8) when the SCR is able to block reapplied forward voltage without turning on; it is measured under specified conditions of current, voltage and temperature.

Changes in the specified conditions change the SCR turn-off time. Figure 5.2 for example gives a typical curve of the change in SCR turn-off time with gate bias. Figure 5.3 shows the change with junction temperature and 5.4 shows the change with forward current.

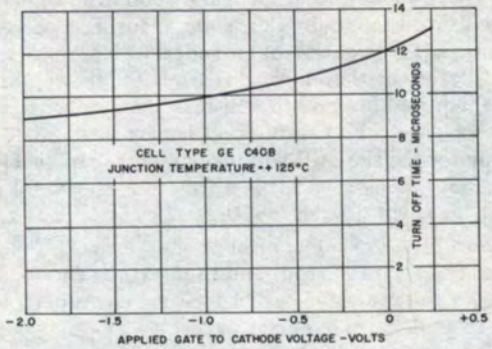


Figure 5.2 Effect of Gate Bias Condition on SCR Turn-Off Time

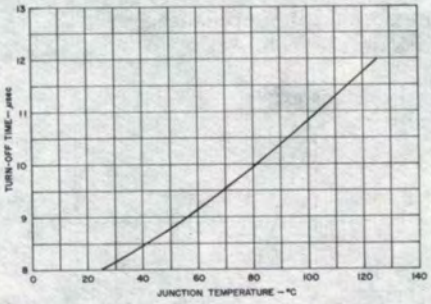


Figure 5.3 Typical SCR Turn-Off Time vs. Junction Temperature (C12 and C40)

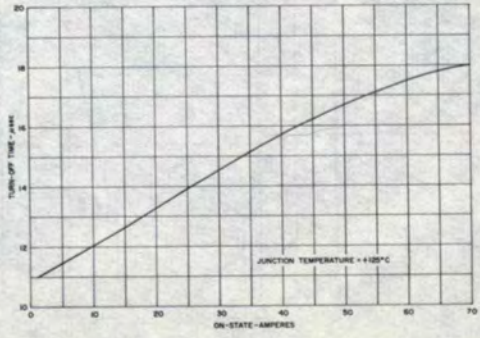


Figure 5.4 Typical SCR Turn-Off Time vs. Forward Current (C40)

5.1.2 Circuit Turn-off Time (t_c)

The circuit turn-off time is the turn-off time that the circuit presents to the SCR.

The circuit turn-off time (t_c) must always be greater than the turn-off time of the SCR (t_{off}); otherwise the SCR will turn on.

5.2 SCR'S WITH GUARANTEED MAXIMUM TURN-OFF TIME

The turn-off times of standard SCR's are usually given as typical values. Wide deviations from the typical values can occur. In those circuits where turn-off time is a critical characteristic, it is necessary for the circuit designer to have control over the maximum value of SCR turn-off time. For this reason General Electric offers a range of SCR's with guaranteed maximum turn-off times under specified standard conditions of waveform and temperature.

5.3 REVERSE RECOVERY CURRENT AND REVERSE RECOVERY TIME

The time during which reverse recovery current flows in the SCR (t_3 to t_6 in Figure 5.1) is known as the reverse recovery time. This is the time required before the SCR can block *reverse* voltage. This should not be confused with turn-off time which is the time that has to elapse before the SCR can block reapplied *forward* voltage. The reverse recovery phenomenon is also common in junction diodes.

Reverse recovery time in typical SCR's is of the order of a few microseconds. Recovery time increases as forward current increases and also increases as the rate of decay of forward current decreases.

The reverse recovery current phenomenon plays a minor but important part in the application of SCR's:

1. In full wave rectifier circuits using SCR's as the rectifying elements the reverse recovery current has to be carried in the forward direction by the complementary SCR's. This can give rise to high values of turn-on current.
2. In certain inverter circuits such as the McMurray-Bedford (Chapter 9) circuit where one SCR is turned off by turning another on, the reverse recovery current of the first gives rise to high values of turn-on current in the second.
3. The cessation of reverse current, which can be very sudden, may produce damaging voltage transients and radio frequency interference.
4. When SCR's are connected in series the reverse voltage distribution may be seriously affected by mismatch of reverse recovery times (Chapter 6).

5.4 TURN-OFF METHODS

The gate has no control over the SCR once anode-to-cathode current is flowing. External measures therefore have to be applied to stop the flow of current. There are two basic methods available for commutation, as the turn-off process is called.

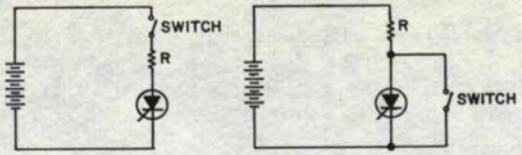


Figure 5.5 Commutation by Current Interruption

5.4.1 Current Interruption

The current through the SCR may be interrupted by means of a switch in either of two positions, Figure 5.5. The switch must be operated for the required turn-off time. Note that the operation of the switch will cause the SCR to see high values of dv/dt.

5.4.2 Forced Commutation

When the above methods of current interruption are not acceptable, then forced commutation must be used. The essence of the forced commutation method is to switch current from some energy source so as to force more current through the SCR in the reverse direction than is trying to flow in the forward direction.

5.5 CLASSIFICATION OF FORCED COMMUTATION METHODS

There are six distinct classes by which the energy is switched across the SCR to be turned off: (Table 5.1).

Class A Self commutated by resonating the load
Class B Self commutated by an LC circuit
Class C C or LC switched by another load-carrying SCR
Class D C or LC switched by an auxiliary SCR
Class E An external pulse source for commutation
Class F AC line commutation

Examples of circuits which correspond to these classes will now be given. These examples show the classes as choppers (Chapter 9). The commutation classes may be used in practice in configurations other than choppers. References to literature covering the different classes will be found in Chapter 9.

5.5.1 Class A—Self commutated by resonating the load

When SCR_1 is triggered, anode current flows and charges up C in the polarity indicated. Current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off.

The condition for commutation is that the LCR circuit must be underdamped.

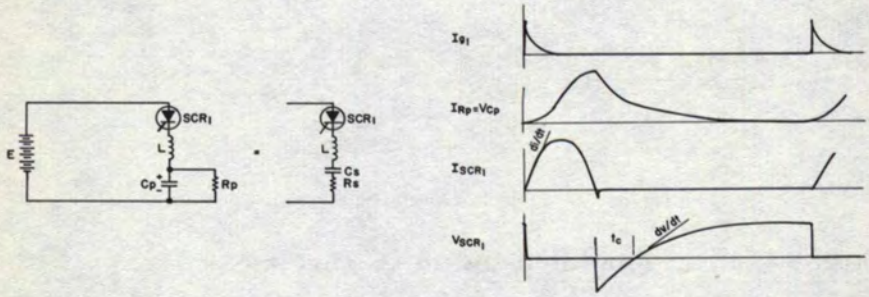


Figure 5.6 Class A Commutation

5.5.2 Class B—Self commutated by an LC circuit

Example 1

Before the gate pulse is applied, C charges up in the polarity indicated. When SCR_1 is triggered, current flows in two directions.

1. The load current I_R flows through R.
2. A pulse of current flows through the resonant LC circuit and charges C up in the reverse polarity. The resonant-circuit current will then reverse and attempt to flow through the SCR in opposition to the load current. The SCR will turn off when the reverse resonant-circuit current is greater than the load current.

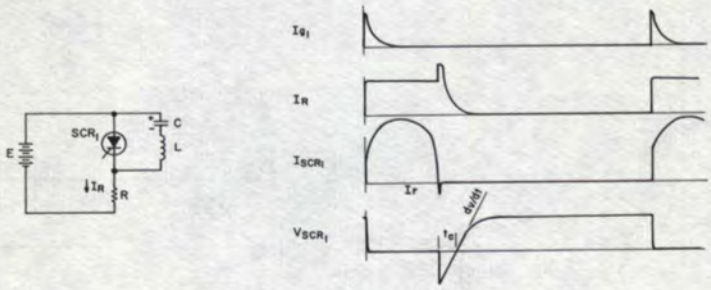


Figure 5.7 Class B Commutation (Example 1)

Class B—Self commutated by an LC circuit

Example 2—The Morgan Circuit

From the previous cycle the capacitor is charged as shown in Figure 5.8 and the reactor core has been saturated "positively."

When SCR_1 is triggered, the capacitor voltage is applied to the reactor winding L_2. The polarity of the applied voltage immediately pulls the core out of saturation. For the time t_1 to t_2 (Figure 5.8) the load current is flowing through R. Simultaneously the capacitor is being discharged.

When the voltage across L_2 has been applied for the prescribed time, the core goes into "negative" saturation. The inductance of L_2 changes from the high unsaturated value to the low saturated value.

The resonant charging of C now proceeds much more rapidly from time t_2 to t_3. As soon as the peak of current is reached and current starts to decrease, the voltage across L_2 reverses.

As soon as the voltage reverses, the core comes out of saturation again, the inductance rises to the high value and the recharging of C proceeds at a more leisurely pace (t_3 to t_4).

The voltage across the inductor is held for the prescribed time and then positive saturation occurs (t_4).

Now the capacitor is switched directly across the SCR via the saturated inductance of L_2. If the reverse current exceeds the load current SCR_1 will be turned off. The remaining charge in C then is dissipated in the load and C is charged up as in Figure 5.8 ready for the next cycle (t_5).

It is quite possible in practice to design L so that negative saturation does not occur. In this case the anode-current pulse from t_2 to t_3 is omitted.

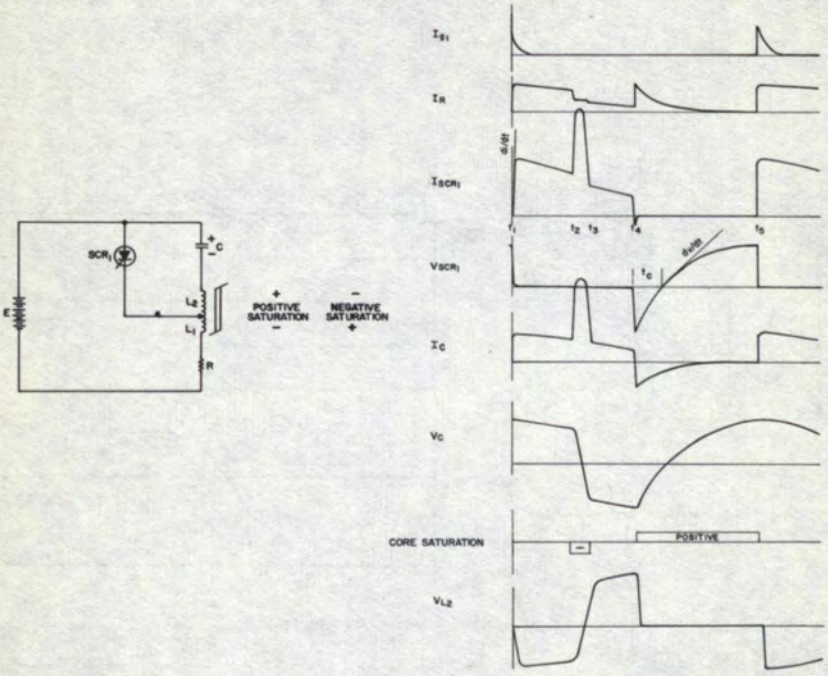


Figure 5.8 Class B Commutation (Example 2)

5.5.3 Class C—C or LC switched by another load-carrying SCR

Assume SCR_2 is conducting. C then charges up in the polarity shown. When SCR_1 is triggered, C is switched across SCR_2 via SCR_1 and the discharge current of C opposes the flow of load current in SCR_2.

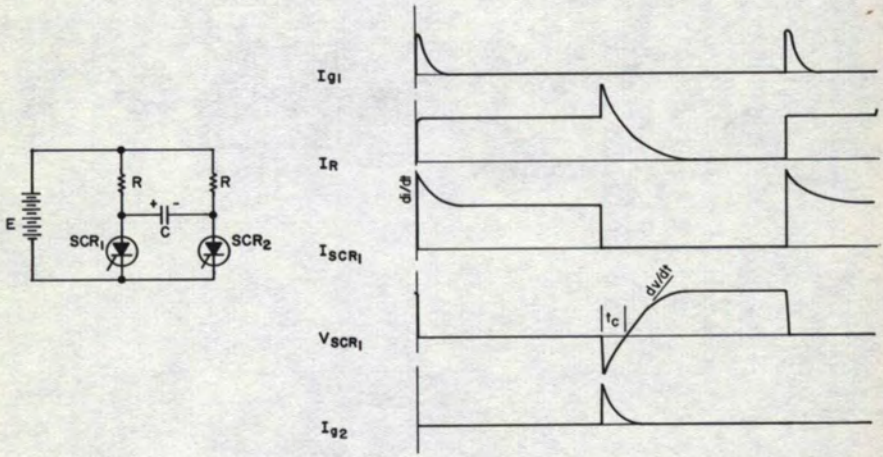


Figure 5.9 Class C Commutation

5.5.4 Class D—LC or C switched by an auxiliary SCR

Example 1.

The circuit shown in Figure 5.9 (Class C), can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR. The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.

Example 2.

SCR_2 must be triggered first in order to charge up the capacitor in the polarity shown. As soon as C is charged, SCR_2 will turn off due to lack of current.

When SCR_1 is triggered the current flows in two paths: Load current flows in R; commutating current flows through C, SCR_1, L, and D, and the charge on C is reversed and held with the hold-off diode D. At any desired time SCR_2 may be triggered which then places C across SCR_1 via SCR_2 and SCR_1 is turned off.

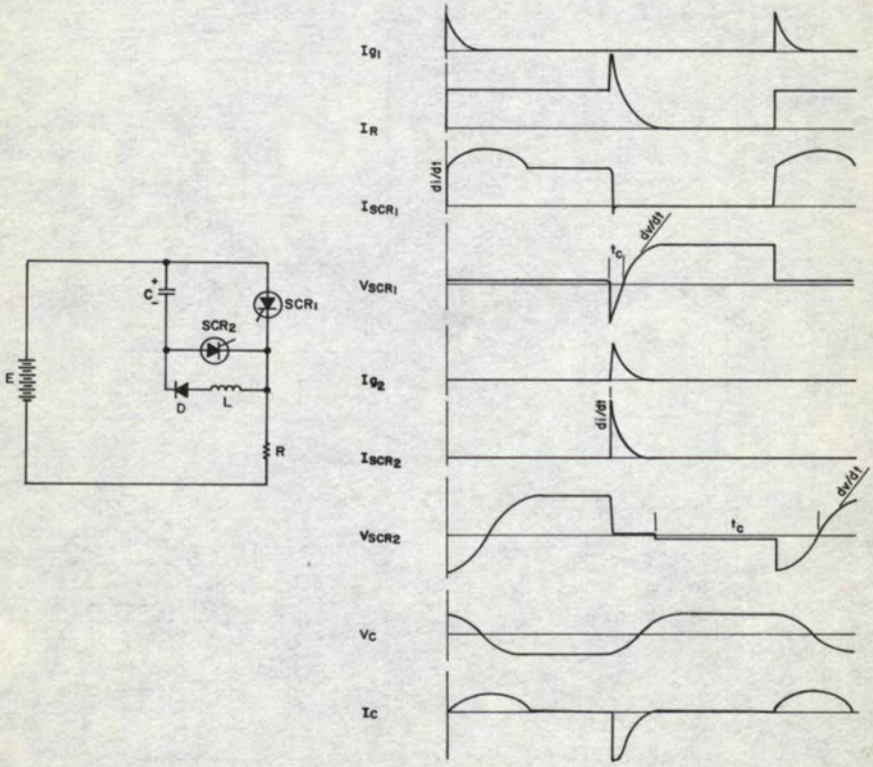


Figure 5.10 Class D Commutation (Example 2)

Class D—LC or C switched by an auxiliary SCR

Example 3.—The Jones Circuit

The outstanding feature of this circuit is its ability to start commutating reliably.

If C were discharged, then, on triggering SCR_1, voltage would be induced into L_2 by closely coupled L_1, and C would become charged in the polarity shown. As soon as SCR_2 is triggered, SCR_1 is turned off. C now becomes charged in the opposite polarity.

The next time SCR_1 is triggered, C discharges via SCR_1, and L_2, and its polarity is reversed ready for the next commutating pulse. The voltage to which C is charged (in the polarity shown in Figure 5.11), depends on which is greater: the voltage induced by load current flowing in L_1 or the reversal of the positive charge built up while SCR_2 was conducting.

With heavy loads, the induced voltage increases, thus tending to offset the decrease of turn-off time. Better turn-off times are obtained with this circuit as compared with Example 2 at the cost of higher voltages appearing across the SCR's. This circuit is discussed in more detail in Chapter 9.

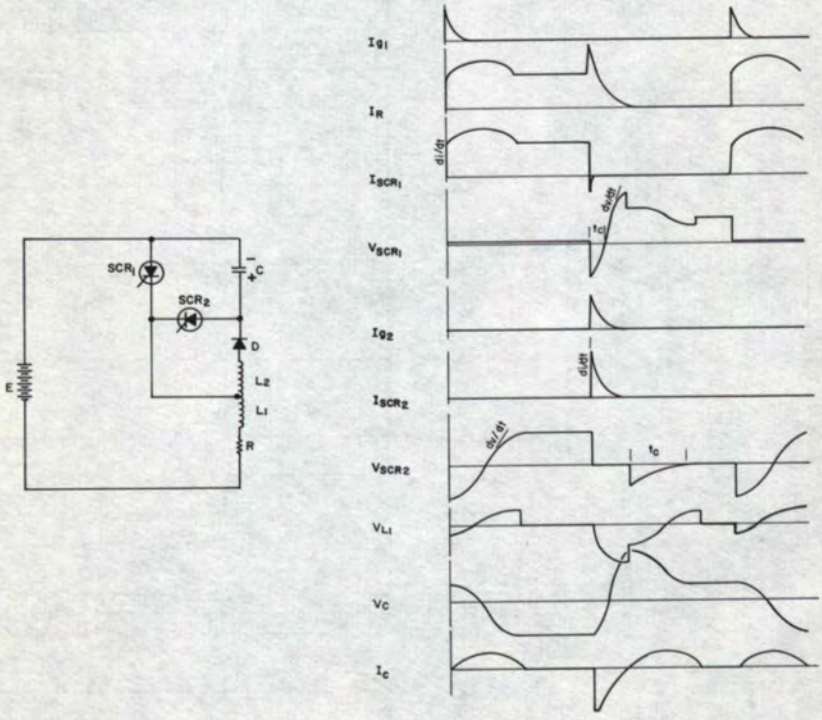


Figure 5.11 Class D Commutation (Example 3)

Class D—LC or C switched by an auxiliary SCR

Example 4.

This circuit is important because no capacitor-charging pulse flows through the load.

Assume C is charged in the polarity shown to some voltage greater than the supply voltage E. When SCR_1 is triggered, load current flows in R and L_2. SCR_2 is in a resonant circuit consisting of C and L_2. When SCR_2 is triggered, a pulse of current flows through L_2. A voltage is developed across L_2 which is greater than the supply voltage E. Reverse voltage is therefore applied to SCR_1 which turns it off. The termination of the discharge pulse through SCR_2 turns it off, and C is now charged in the opposite polarity. L_1 is much larger than L_2, and C is now resonantly charged via L_1 and D to some voltage greater than the supply voltage.

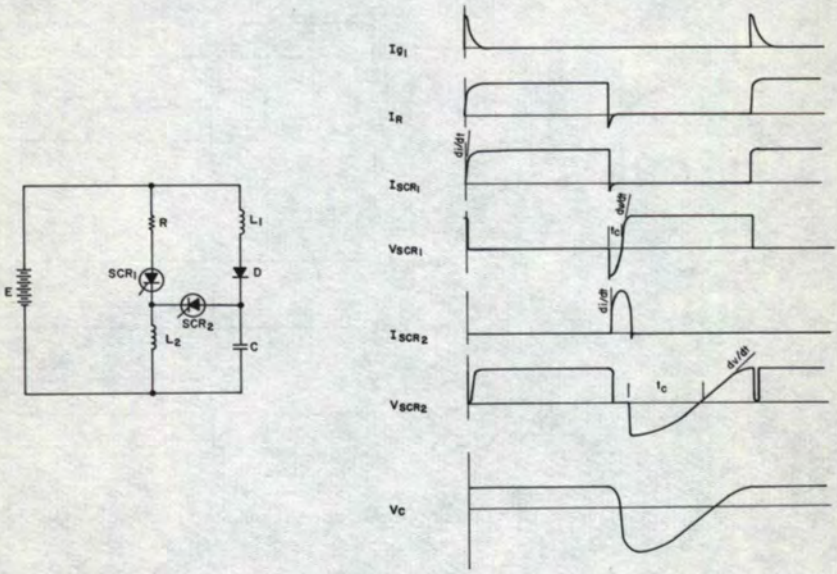


Figure 5.12 Class D Commutation (Example 4)

5.5.5 Class E—External pulse source for commutation

Example 1.

When SCR_1 is triggered, current will flow into the load. To turn SCR_1 off base drive is applied to the transistor Q_1. This will connect auxiliary supply E_2 across SCR_1 turning it off. Q_2 is held on for the duration of the turn-off time.

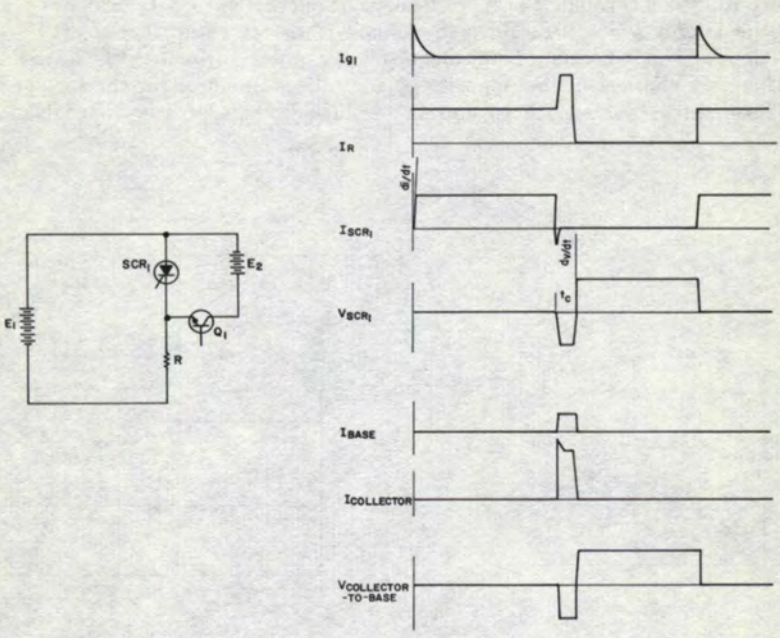


Figure 5.13 Class E Commutation (Example 1)

Class E—External pulse source for commutation

Example 2.

The transformer is designed with sufficient iron and air gap so as not to saturate. It is capable of carrying the load current with a small voltage drop compared with the supply voltage.

When SCR_1 is triggered, current flows through the load and pulse transformer. To turn SCR_1 off a positive pulse is applied to the cathode of the SCR from an external pulse generator via the pulse transformer. The capacitor C is only charged to about 1 volt and for the duration of the turn-off pulse it can be considered to have zero impedance. Thus the pulse from the transformer reverses the voltage across the SCR, and it supplies the reverse recovery current and holds the voltage negative for the required turn-off time.

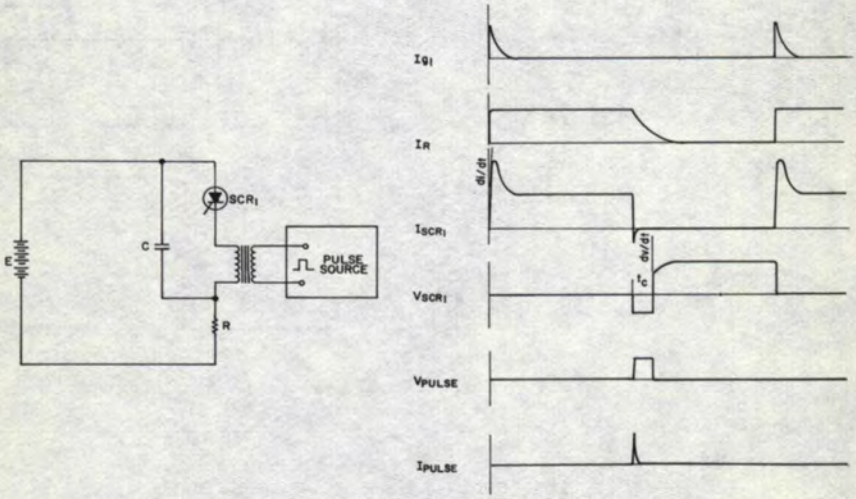


Figure 5.14 Class E Commutation (Example 2)

Class E—External pulse source for commutation

Example 3.

When the SCR is turned on, the pulse transformer saturates and presents a low impedance path for the load current. When the time comes for turning off the SCR, the first step is to de-saturate the pulse transformer. This is done by means of a pulse in the polarity shown. This de-saturating pulse momentarily increases the voltage across the load and also the load current. Once the pulse transformer is de-saturated, a pulse in the reverse polarity is injected, reversing the voltage across the SCR and turning it off. The pulse is held for the required turn-off time.

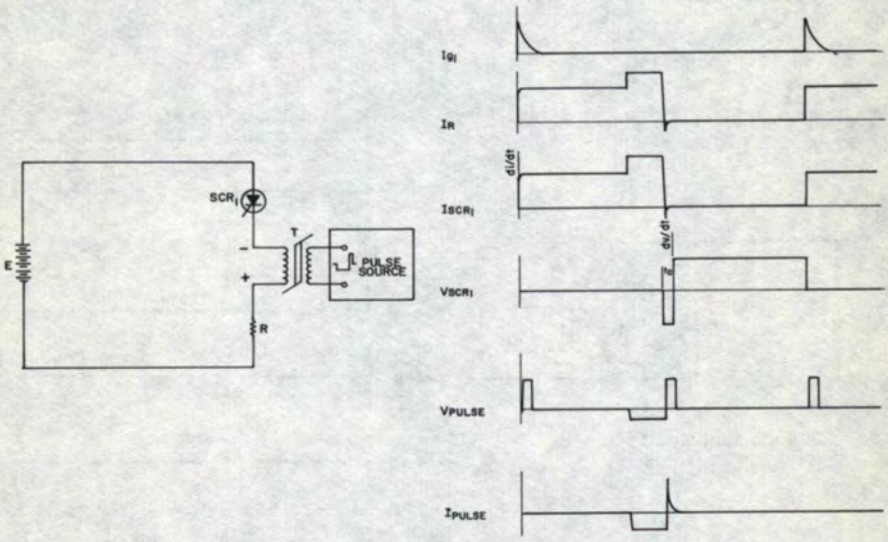


Figure 5.15 Class E Commutation (Example 3)

5.5.6 Class F—AC line commutated

If the supply is an alternating voltage, load current will flow during the positive half cycle. During the negative half cycle the SCR will turn off due to the negative polarity across the SCR. The duration of the half cycle must be longer than the turn-off time of the SCR.

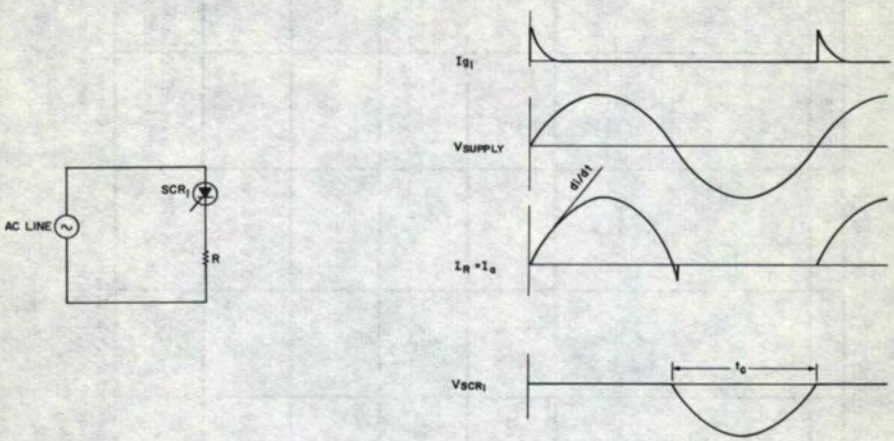
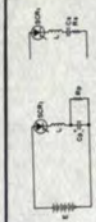
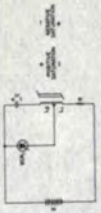
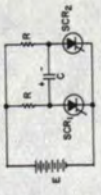
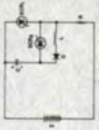
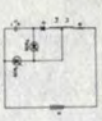
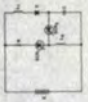
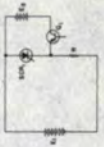
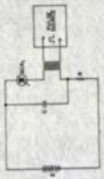
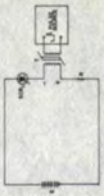


Figure 5.16 Class F Commutation

TABLE 5.1
REQUIRED SCR DYNAMIC CHARACTERISTICS FOR REPRESENTATIVE CIRCUITS

CLASS	A	B	B	C	D	D	D	E	E	E	F
CIRCUIT											
CHARGE PER PULSE IN SCR_1 ($A\mu S$) note 1	$\frac{4E\sqrt{LC_S}}{\pi R_S}$	$E\sqrt{LC}\left(\frac{\pi}{R}+\frac{4}{\pi R_C}\right)$	*	$\frac{Et}{R}+2EC$	$\frac{Et}{R}+2EC$	$\approx\frac{Et}{R}+2EC$	$\frac{Et}{R}-\frac{EL}{R^2}$	$\approx\frac{Et}{R}$	$\frac{Et}{R}+EC$	$\approx\frac{E}{R}$	$\frac{E\times10^6}{R\pi f}$
INITIAL di/dt OF ANODE CURRENT IN SCR_1 ($A/\mu S$)	$\frac{2E}{\pi R_S}\times\frac{1}{\sqrt{LC_S}}$	$\frac{E}{L}+\frac{E}{L_R}$	$\approx\frac{E}{L_1}$	$\frac{E}{\text{Stray L}}$	$\frac{E}{L}+\frac{E}{L_R}$	$\approx\frac{E}{L_1}$	$\frac{E}{L_2}$	$\frac{E}{L_R}$	$\frac{E}{L_{Transformer}}$	$\frac{E}{L_{Transformer}}$	$\frac{2\pi fE\times10^{-6}}{R}$
PEAK VOLTAGE ACROSS SCR_1 (V)	$\frac{4E}{\pi}\sqrt{Q^2+1}$	E	>E	E	E	>E	*	E	E	E+e_1	E
MAXIMUM dv/dt ON SCR_1 ($V/\mu S$)	$\frac{4E}{\pi}\sqrt{\frac{Q^2+1}{LC_S}}$	$\frac{1.2E}{CR}$	$>\frac{1.2E}{CR}$	$\frac{1.2E}{CR}$	$\frac{1.2E}{CR}$	$>\frac{1.2E}{CR}$	*	$\approx$E	$\frac{1.2E}{CR}$	$\approx$E	$2\pi fE\times10^{-6}$
MINIMUM tc for SCR_1 (μS)	$\sqrt{LC_S}\tan^{-1}Q$	0.7CR	>0.7CR	0.7CR	0.7CR	>0.7CR	$\frac{\pi}{2}\sqrt{L_2C}$	pulse width on Q_1	external pulse width	external pulse width	$\frac{10^6}{2f}$

Note 1. Multiply charge per pulse by repetition rate $\times10^{-6}$ to get average current.

Note 2. Equations are for "pure" resistive loads only.

Symbols. t = interval between turn-on and turn-off pulse in SCR_1
L_R = stray inductance of resistive load
R_C = effective resistance of LC circuit
$Q=\frac{1}{R_S}\sqrt{\frac{L}{C_S}}$ Q must be ≥ 2.

Units. C in μf
f in cycles per second
L in μh
R in ohms
t in μs

5.6 CAPACITORS FOR COMMUTATION CIRCUITS

The capacitors used in the various methods of turning off SCR's need care in their selection and specification. The following properties are desirable:

1. The capacitor life should be long, at the operating ambient temperature, and comparable with that of the SCR.
2. The losses should be low for two reasons:
   a. To avoid high internal temperatures which would shorten the capacitor life.
   b. To maintain the advantage of high efficiency which the SCR gives to the over-all circuit.
3. The capacitor's equivalent series inductance should be known. In many circuits inductance in series with the commutating capacitor plays an important part in controlling the initial rate of rise of anode current through the SCR.

The equipment designer is advised to take the following steps:

1. For the breadboard, stock inverter capacitors may be purchased from the General Electric Capacitor Department, Hudson Falls, New York. The following extract from the catalog gives the ratings of off-the-shelf capacitors.

2. After completion of the breadboard tests, the voltage and current waveforms and temperature data should be submitted to the capacitor manufacturer for optimization of life, size, and cost.

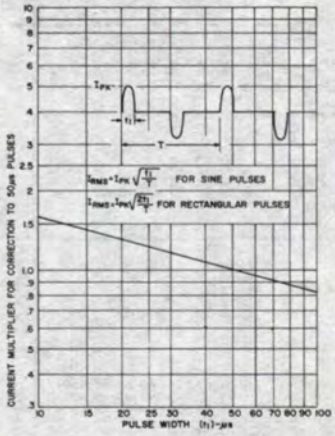


Figure 5.17 Current Multiplier For Capacitors

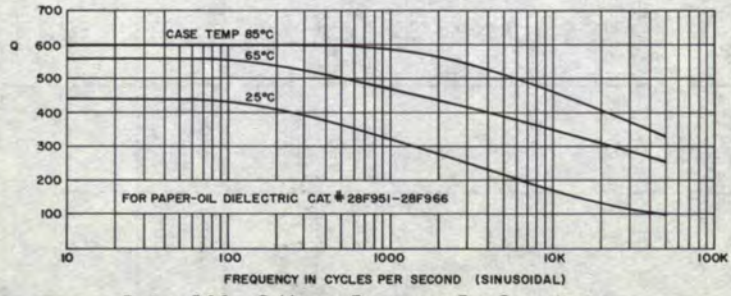


Figure 5.18 Q Versus Frequency For Capacitors

TABLE 5.2 Extracts From G-E Capacitor Catalog

RMS Volts AC Max	DC Volts Max	μf ±10%	Catalog Number	Dielectric	Configuration	Case Base		Case Height	Max RMS Amps at Given Max Temp†			
						Width	Depth		Amb. 80°C	Amb. 70°C	Amb. 60°C	Amb. 50°C
									Case 87°C	Case 83°C	Case 80°C	Case 77°C
500		8/8/8	17F405		Rect.	8	4	6	30	66	90	120
165	200	3	28F951		Oval	2 5/32	1 5/16	2 5/16	7.0	10.0	12.3	14.2
		5	28F952		Oval	2 5/32	1 5/16	3 1/16	9.8	14.2	17.4	19.9
		10	28F953		Rect.	3 3/4	1 1/4	4 1/4	22.0	31.6	39.5	42.9
		20	28F954		Rect.	3 3/4	2 1/4	4 1/2	38.0	43.0	43.1	43.4
200	250	2	28F955		Oval	2 5/32	1 5/16	2 5/16	5.7	7.9	9.8	11.7
330	600	2	28F956	*	Oval	2 5/32	1 5/16	2 13/16	6.3	8.8	11.0	12.6
		3	28F957	Oil	Oval	2 5/32	1 5/16	3 13/16	8.5	12.3	14.8	17.4
		5	28F958	Impreg-	Rect.	3 3/4	1 1/4	4 1/4	15.8	22.1	28.4	31.6
		10	28F959	nated	Rect.	3 3/4	2 1/4	4 1/2	25.3	37.9	42.9	43.0
		20	28F960	Paper	Rect.	3 3/4	3 3/16	5 1/2	43.0	43.0	43.0	43.0
400	800	1	28F961		Oval	2 5/32	1 5/16	2 5/16	4.1	5.7	6.9	8.2
700	2000	1	28F962		Oval	2 5/32	1 5/16	4 3/8	5.3	7.2	9.1	10.7
		2	28F963		Rect.	3 3/4	1 1/4	4 3/4	10.7	15.2	18.3	21.2
		3	28F964		Rect.	3 3/4	2 1/4	4 1/2	14.5	20.5	25.3	28.4
		5	28F965		Rect.	3 3/4	3 3/16	5 1/8	22.1	30.6	36.3	42.6
		10	28F966		Rect.	4 9/16	3 3/4	6	36.3	43.0	43.0	43.0
330	600	20	28F1202	§	Oval	3 21/32	1 31/32	5 1/4	43	43	43	43
				Poly-								
700	2000	10	28F1203	carbonate	Oval	2 11/16	1 9/16	3 7/8	22.6	29	36	43
									Max VA at Given Max Temp			
115		25	28F1101	**	Oval	2 11/16	1 9/16	2 1/8	33	125	230	350
		50	28F1102	Metalized	Oval	2 11/16	1 9/16	2 7/8	42	160	290	430
		100	28F1103	Paper	Oval	3 21/32	1 31/32	3 1/8	65	245	440	670
		125	28F1104		Oval	3 21/32	1 31/32	3 7/8	76	285	520	782

† Based on 50 microseconds current pulse width (t_1). For pulse widths other than 50 microseconds see Fig. 5.17. * See Fig. 5.18 for Q values. Estimated life for 28F type oil impregnated paper units for 95 percent survival is 40,000 hours, provided temperature, voltage and rms current limitations are adhered to.

§ Loss factor for polycarbonate is generally ten times less than for paper. **Peak current must not exceed 10 amps per μf regardless of pulse width.

A check list of the required data follows:

1. Capacitance Required:_____ Tolerance (if less than ±10%)_____
2.* Peak Voltage:_____ RMS Voltage:_____
3.* Peak Current:_____ RMS Current:_____
4.* Repetition Rate:_____ Duty Cycle:_____
(time on—time off)
5. Minimum Q:_____ Series Inductance if other than 0.1 μH ±50%_____
6. Ambient Temperature:_____ Max._____ Min._____
7. Desired Operating Life:_____ (total cycles)
_____ (total hours)
8. Physical Size Limitations:_____
9. Mounting Requirements:_____
10. Unusual atmospheric conditions: (dust, chemicals, humidity, corrosion, etc.)_____
11. Other special requirements: (high altitude, shock, vibration, etc.)_____
12. What kind cooling available: (fins, heatsink, forced air, etc.)_____

* Show sketch of voltage wave shape vs. time.

Series and Parallel Operation of SCR's

When circuit requirements dictate operation at higher voltages and currents than can be realized with a single SCR, series and parallel combinations can be employed if certain design precautions are taken. These precautions are primarily the equalization of the voltages and currents between individual SCR's. Shown in Figure 6.1 are hypothetical voltage/current characteristics for two random SCR's. If the two SCR's are connected in series one might expect them to have a total forward blocking capability of at least 2 (v_2). Yet without forced voltage equalization the total peak forward blocking voltage will be limited to approximately (v_1+v_2) in order to keep SCR2 from turning on. Likewise, if the two SCR's are connected in parallel, without forced current sharing, the total forward conduction current must be limited to (i_1+i_2) in order to prevent damage to SCR2 if its maximum current rating is i_2 amperes.

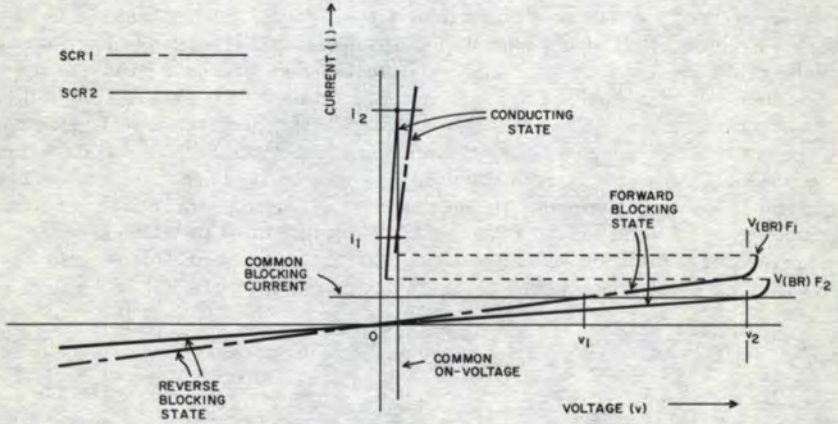


Figure 6.1 SCR Characteristics

6.1 SERIES OPERATION

When designing an SCR series arrangement, it is essential to force approximately equal voltage to the SCR's at all times. Figure 6.2 shows diagramatically the six operating states that can occur in a random sample of SCR's connected in series without forced equalization. It is seen that the equivalent impedances change continuously as the SCR string switches from state to state.

During forward and reverse blocking (states I and VI) the differences in blocking currents result in unequal voltage sharing. This could be harmful to an SCR with low leakage current since it might cause excessive voltage to appear across the SCR. In order to equalize the blocking voltages a shunt resistor is connected across each SCR. The conducting states (III and IV) represent no problem of voltage equalization.

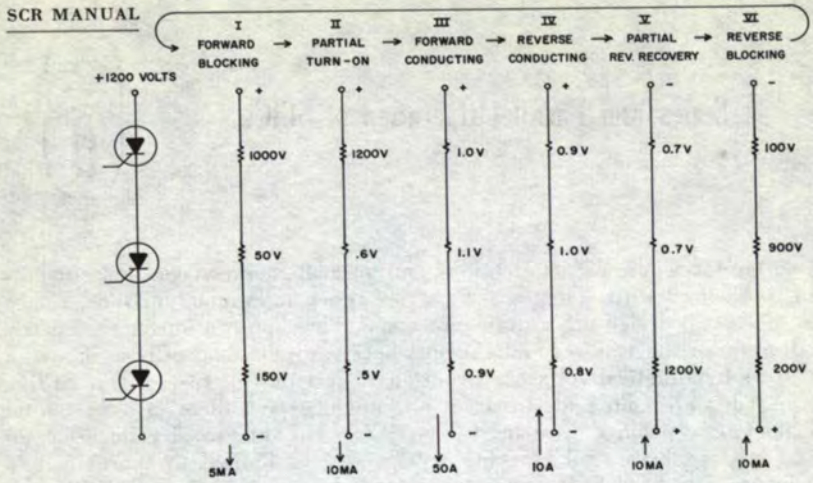


Figure 6.2 Possible Operating States of an Unequalized Series String

States II and V shown in Figure 6.2 represent undesirable conditions since each presents a momentary excessive voltage to at least one SCR. Inasmuch as these states cannot be eliminated, some form of voltage sharing during this time is desirable. Voltage can be equalized to a great degree during State II by simultaneous turn-on of all SCR's (simultaneous triggering). Triggering of series SCR's will be discussed later. State V results from the fact that in a randomly chosen series string of SCR's, all SCR's will not recover their reverse blocking ability at the same instant. As soon as the first SCR recovers, the reverse voltage intended for the entire string appears across that one member. To equalize the voltage during this period, a capacitor is connected across each SCR. If the impedance of the capacitor is low enough during the reverse recovery time (a transient phenomena), the voltage buildup on fast recovery SCR's is limited until the slowest SCR in the string recovers. Addition of shunt capacitors limits forward voltage rise during turn-on also thus alleviating the undesirable condition of State II.

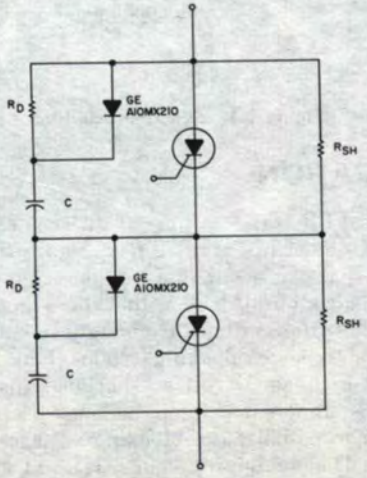


Figure 6.3 Series Equalizing Arrangement

In summary, States III and IV present no equalization problem. Shunt resistors equalize the voltage during States I and VI. Shunt capacitors equalize the voltage during States II and V. Virtual simultaneous triggering reduces, and all but eliminates inequalities during State II.

While capacitors provide excellent transient voltage equalization, they also produce high switching currents through the SCR's during the turn-on interval.[1,2] Switching currents can be limited by means of damping resistors in series with each capacitor. The value of the damping resistors must be kept to a reasonably low value in order not to reduce the effectiveness of the capacitors in equalizing voltage during the reverse recovery time.

Figure 6.3 shows the voltage equalization scheme described above. Diodes are shown across the damping resistors R_D to increase the effectiveness of the capacitors in preventing misfiring due to excessive rate of rise of forward voltage on the SCR's. The damping resistors still limit the switching current duty on the SCR's.

6.1.1 Equalizing Network Design

6.1.1.1 Determining Shunt Resistance Value

The maximum allowable value of R_{SH} can be determined from the following equation:

$$R_{SH} = \frac{nV_{(BR)F} - V_{PK}}{(n-1).\ i_{FM}}$$

where $V_{(BR)F}$ = minimum forward breakover voltage per cell (volts)

V_{PK} = maximum peak forward voltage impressed across the string (volts)

n = number of SCR's in series

i_{FM} = maximum forward blocking current per cell (amps)

Both $V_{(BR)F}$ and i_{FM} can be established from the appropriate SCR specification sheet.

6.1.1.2 Determining Shunt Capacitance Value

The maximum size of capacitor required can be determined from the following equation:

$$C = \frac{10\ (i_F)}{V_{ROM}\ (rep)}$$

where C = maximum capacitance required to distribute reverse recovery transient within cell V_{ROM} (rep) rating (μf)

i_F = current flowing through cell immediately preceding commutation (amps)

V_{ROM} (rep) = maximum repetitive cell PRV rating (volts)

The above expression for C is based on the assumption that one SCR of the string recovers instantaneously while the others recover in a "typical" time. This is a worst-case approximation and it is usually possible to reduce the capacitance by experimental optimiztion.

6.1.1.3 Determining Damping Resistance Value

For operation at 400 cps and below,[1] the following relationship may be used to determine a minimum value for the damping resistors that will limit the switching currents to the ratings of the SCR's.

$$R_{D(min)} = \frac{0.8}{\sqrt{C}} \log_e \left[\frac{\pi V_{(BR)F} \sqrt{C}}{2\,(i_{TO} - i_F)} \right] \Bigg|_{t = t_1}$$

where C = equalization (shunt) capacitance (μfarads)

$i_{TO}\big|_{t_1}$ = turn-on current limit from the appropriate current limit line of the switching dissipation curve evaluated at time = t_1 (see Figure 3.10)

$i_F\big|_{t_1}$ = anode current due to load and commutation circuit evaluated at t_1 where

$t_1 = \sqrt{C}$ μseconds (C in μf)

Note that damping resistors are not required when:

$$\frac{\pi\, V_{(BR)F}\, \sqrt{C}}{2\,(i_{TO} - i_F)} \Bigg|_{t = t_1} \leq 1$$

The diodes used to prevent dv/dt triggering must be fast recovery types in order not to defeat the purpose of the damping resistors.

To illustrate the use of the foregoing relationships, the following example of an equalizing network design is presented. Assume that operation applies a peak forward and reverse blocking voltage of 1000 volts on two C35M SCR's in series. Instantaneous forward current is 20 amperes just before commutation.

$$R_{SH} = \frac{n\, V_{(BR)F} - V_{PK}}{(n-1)\,.\, i_{FM}} = \frac{2\,(600) - 1000}{1 \cdot (5.0 \times 10^{-3})}$$

$$R_{SH} = \frac{200}{5 \times 10^{-3}} = 40 \text{ k ohms}$$

$$C = \frac{10\, I_f}{V_{ROM(rep)}} = \frac{10 \times 20}{600} = .33\ \mu f$$

$$R_D = \frac{0.8}{\sqrt{C}} \log_e \left[\frac{\pi\, V_{(BR)F}\, \sqrt{C}}{2\,(i_{TO} - i_F)} \right] \Bigg|_{t = t_1}$$

$$t_1 = \sqrt{C} = \sqrt{.33}$$

$$= .57 \ \mu\text{seconds}$$

From Figure 3.10, at .57 μseconds, i_{TO} for $V_{(BR)F}$ = 600 volts is 15 amperes. Assume i_F is small compared to i_{TO} so that:

$$R_D = \frac{0.8}{.57} \log_e \left(\frac{\pi \ (600) \ (.57)}{2 \ (15 - 0)} \right)$$

$$R_D = 1.4 \log_e (36)$$

$$R_D = (1.4) \ (3.6) \cong 5 \text{ ohms}$$

The diodes used for dv/dt limit are G.E. A10MX210 fast recovery rectifiers.

The arrangement of Figure 6.3 provides voltage sharing under all conditions of forward and reverse blocking. In applications where the increase in blocking losses due to current through the equalizing resistors must be avoided, as in SCR radar modulator switches, voltage sharing may be successfully accomplished by replacing each shunt equalizing network with a silicon controlled avalanche rectifier as shown in Figure 6.4(a). When maximum avalanche voltage is chosen correctly, total forward blocking current through the circuit will be only slightly higher than the maximum blocking current of the worst SCR. Maximum avalanche voltage of the shunt rectifier should be equal to, or slightly below, the SCR forward breakover

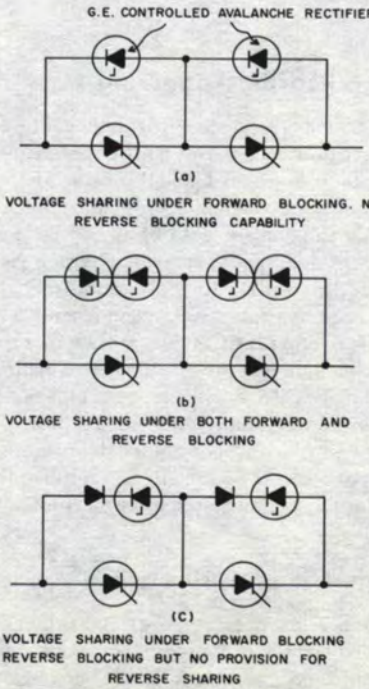


Figure 6.4 Series Equalizing Arrangements Using Controlled Avalanche Rectifiers

voltage specification. Minimum avalanche voltage must be higher than V_{PK}/n when measured at the controlled avalanche rectifier's minimum operating temperature. To provide optimum equalization it is desirable to have as narrow a tolerance as possible on the avalanche voltage of the shunt rectifier. Where a series string has to block appreciable reverse as well as forward voltage, inverse series controlled avalanche rectifiers may be substituted for the single units (see Figure 6.4(b)). In cases where reverse blocking requirements are not severe, some reverse blocking ability can be obtained using controlled avalanche rectifiers and conventional silicon rectifiers arranged as in Figure 6.4(c).

6.1.2 Triggering in Series Operation

There are two methods in common use for triggering series SCR's, namely:

1. Simultaneous triggering with multiple secondary windings on a pulse transformer;
2. Slave triggering whereby one "master" SCR is triggered, and as its forward blocking voltage begins to collapse, a gate signal is thereby applied to the "slave" SCR.

Simultaneous triggering of all SCR gates is a preferred method. Slave triggering, while it is a unique way to provide gate isolation, produces some time delay between master and slave. Fortunately, the equalization capacitors used for voltage equalization during the reverse recovery period also limit the forward voltage rise. As long as the shunt capacitance is sufficient to limit forward voltage within the PFV ratings of the SCR's until all SCR's are "on," slave triggering can be reliably employed.

6.1.2.1 Transformer/Reactor Triggering

When using pulse transformers or saturable reactors with multiple gate windings, particular attention should be given to the insulation between windings. This insulation must be able to support at least the peak of the supply voltage.

Triggering requirements may differ quite widely between individual SCR's. To prevent a cell with a low impedance gate characteristic from shunting the signal away from a cell with a high impedance gate characteristic, resistance should be inserted in each gate lead, or built into the transformer.

Where the total energy available to trigger is limited, as may well be the case in a pulse triggering arrangement, it is preferable to replace these resistors with capacitors in series with each gate lead. Series capacitors tend to equalize the charge coupled to each SCR gate during trigger pulses, thus reducing the effects of unequal loading without additional energy dissipation. When capacitors are used in this manner a resistor should be connected from gate to cathode of each SCR to provide a discharge path for the capacitor. The circuit must be able to pass a fast risetime pulse, preferably less than 1 microsecond.

6.1.2.2 Slave Triggering of Series SCR's

Figure 6.5 illustrates a slave triggering technique. A voltage equalizing network as previously described is connected across the cells. Only SCR_1 is directly triggered by the pulse source. The gate of SCR_2 is triggered by the surge of discharge current from capacitor C_1 when the voltage across SCR_1 decreases abruptly as it switches into conduction. Since the capacitor-resistor shunts, in conjunction

with the SCR's present a balanced bridge to the zener, the triggering circuit to the SCR's is essentially insensitive to ordinary cyclical variations and transients from the supply voltage. In many cases the equalization network, optimized according to the procedure described earlier, will supply the required gate current to trigger. Fast recovery rectifiers CR_2 and CR_3 can be paralleled with the damping resistors to inhibit triggering from dv/dt of the line voltage.

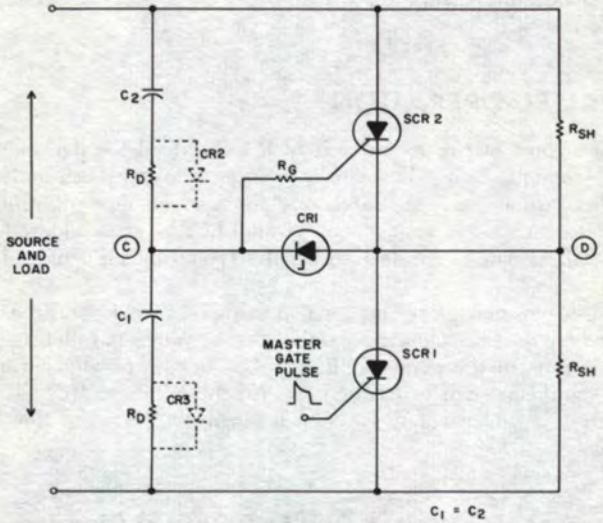


Figure 6.5 Series Operation of SCR's Using Slave Triggering

The minimum capacitance required to supply an abundance of gate current to trigger under all conditions is given by:

$$C_1 \geq \frac{10}{R_G + \frac{V_{GT(max)}}{I_{GT(max)}}} \quad \mu \text{ fds}$$

and

$$R_G = \frac{(V_z/2.7) - V_{GT(max)}}{I_{GT(max)}} \quad \text{ohms}$$

where V_z = nominal zener breakdown voltage of CR_1 (volts)

$I_{GT(max)}$ = maximum gate current to trigger under any of the circuit's operating conditions (milliamps)

$V_{GT(max)}$ = maximum gate voltage to trigger at $I_{GT(max)}$ (volts)

It is necessary that points C and D of Figure 6.5 be as closely balanced as possible. This is to prevent the flow of current in the bridge due to normal cyclical and transient variations of the supply voltage. Depending on the direction of an unbalance, a positive gate current to SCR_2 can result from either a falling or rising supply voltage. The slave triggering technique of Figure 6.5 is expandable to more than two SCR's in series.

6.1.2.3 The Triggering Pulse

For series operation it is imperative to operate the gate well beyond the locus of minimum triggering (see Figure 4.1) in order to obtain turn-on in the minimum possible time. In addition, the pulse should have a very steep rise (ideally about 200 nanoseconds). The width of the pulse should be sufficient to insure that the SCR will latch into conduction under all operating conditions. If anode current swings momentarily to zero during the conducting cycle, the gate pulse must be maintained over the entire conduction period. The amplitude of the gate pulse should be the maximum permissible within the average and peak gate power dissipation ratings of the SCR.

6.2 PARALLEL OPERATION

With the advent of higher current SCR's the need for parallel combinations has steadily decreased. Also it is a rare case when it is more economical to use two smaller devices rather than one large one for a given current requirement. For these reasons it is suggested that use of parallel SCR's be considered only for high current applications where the desired capability cannot be achieved with a single SCR.

The main design consideration for operating SCR's in parallel is the equalization of forward current through the parallel paths. When paralleling low resistance elements, variations in the magnetic flux linked by the parallel circuits can often be the most significant cause of unequal current balance. In SCR circuits, this general situation is aggravated by non-uniformity between the SCR forward characteristics.

6.2.1 Current Unbalance Due to External Circuitry

When forced current sharing is not employed, particular care must be taken to assure that impedance in series with each individual parallel path is maintained as nearly equal as possible. Wiring and connections should be uniform in all respects. The tendency for current to crowd to the outer branches or paths of a parallel network due to reactive effects is of particular significance at higher frequencies, and during the switching interval at the beginning and end of each conduction period. Mutual and self-inductance in series with each parallel path should be equalized where this phenomenon poses a problem.[3]

6.2.2 Current Unbalance Due to Differences in SCR Forward Characteristics

There are two primary methods of minimizing current unbalance due to the differences in SCR characteristics. One is to reduce these differences by using SCR's with matched characteristics in the conduction region and the other is to employ forced current sharing by external means.

6.2.2.1 Use of Parallel Matched SCR's

SCR's with factory matched forward conduction characteristics will share load current if connected directly in parallel. Matched cells of this type are available from General Electric Company on special order. In order to assure satisfactory

current sharing under both normal load and fault conditions, the on-voltage of these special selections are matched at two levels of current. For example, spread in the on-voltage of matched C80 high current SCR's is limited to 50 mv at 3 amperes and 40 mv at 1500 amperes for a specific classification. Based on these figures, a conservative maximum allowable total load current I_{total} through a parallel group of n cells can be expressed as follows:

$$I_{total} = (0.6\ n + 0.4)I_{cell}$$

where I_{cell} is the rated current for a cell operating alone. Thus, two matched C80 cells, each capable of handling 150 amperes average continuously when operated alone, will carry up to

$$(0.6 \times 2 + 0.4) \times 150 = 240 \text{ amperes total (average)}$$

when operated in parallel with each other.

6.2.2.2 Paralleling Unmatched SCR's

When paralleling unmatched SCR's for higher current handling capacity, some external means of forced current sharing is essential. In this case, the components chosen must force current sharing over the entire conduction period of the cell. Resistors are effective but necessarily inefficient. Paralleling reactors as shown in Figures 6.6 and 6.7 are usually the most effective and efficient solution.[4]

In Figure 6.6 when SCR_1 is triggered (from a pulse source), voltage is developed across the reactor as shown. This voltage provides both gate voltage and additional anode voltage to help turn on SCR_2. In practice, as SCR_1 starts to turn on, SCR_2 will follow with but a slight time lag, so that the gate voltage on SCR_2 can never rise excessively. The advantage of this circuit is that if either SCR starts to turn off early in the cycle, as the gate signal is removed, the paralleling reactor develops both gate and anode voltage to keep it turned on.

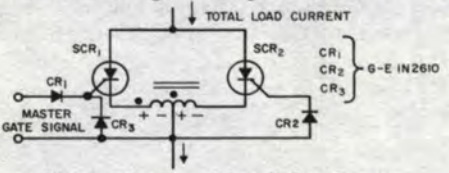


Figure 6.6 Use of Paralleling Reactor

The most important magnetic requirements for such a reactor are high saturation flux density and low residual flux density in order to provide as great a change in total flux ($\Delta\phi$) per cycle as possible. Powdered molybdenum-permalloy cores such as the Arnold type A438281 have been found suitable. CR_1, CR_2, and CR_3 prevent flow of negative gate current in the SCR gate-cathode circuits.

For unmatched SCR's the core must be capable of providing a current-balancing voltage throughout the entire conduction period without saturating. The core may rely on an airgap to return the flux density to a low level at the end of the cycle or on a reset winding to actually reverse the flux before the next cycle starts.

In a single phase circuit, the paralleling core should be capable of supporting $\frac{\Delta V}{2f}$ volt-seconds without saturating where f = supply frequency in cps and ΔV = maximum on-voltage mismatch between SCR's at peak load current. For SCR's with maximum mismatch, ΔV may conservatively be selected as 1 volt.

Figure 6.7 illustrates how equalizing reactors can be used in paralleling three SCR's. Using a three core closed loop arrangement, any one of the three parallel paths could be opened and the two remaining cells would operate satisfactorily,

sharing the total load equally between themselves. This approach has significance in high reliability circuits where continuity of operation is essential, even after removal of a faulty cell from the circuit by a fuse or circuit breaker.

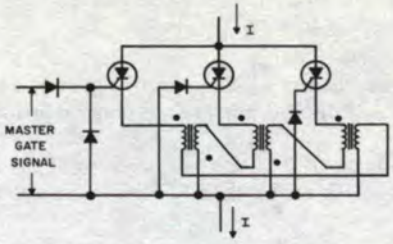


Figure 6.7 Paralleling Reactor Connections for Three Parallel SCR's

Because there is a small but finite delay between triggering of SCR's in these slave-gated parallel arrays, slave gating should not be used in applications where high switching currents are generated, as when paralleled SCR's operate into capacitive or very large resistive loads. *In such cases each SCR must be fired independently and simultaneously to prevent any one cell from instantaneously carrying the full switching current.*

6.2.2.3 Need For a Common Heatsink

At normal load current levels the forward voltage drop of an SCR decreases as junction temperature increases. This phenomenon tends to cause the hotter of two parallel cells to carry more than its share of the total current, thereby causing it to heat up still more and ultimately draw enough current to cause serious damage to the cell. To avoid this possibility, it is suggested that cells operated in parallel be mounted on a common heatsink so that variations in cooling conditions will affect all paralleled cells equally.

6.2.3 Triggering of Parallel Connected SCR's

If parallel SCR's are triggered from a common source, which is an essential requirement when switching high currents to large resistive or capacitive loads, each cell must be supplied with sufficient drive to exceed its own specific triggering needs. As previously pointed out, triggering requirements may differ quite widely between individual SCR's, whether or not units are parallel matched. As such the suggestions of Paragraphs 2 and 3 of Section 6.1.2.1 apply. In addition, it is necessary to drive the gates hard, commensurate with the peak and average gate power dissipation ratings in order to insure fast turn-on. This will cause the SCR's to share the switching duty.

At low values of anode current the forward voltage-current characteristic changes from a positive to a negative resistance as it is reduced towards the minimum holding current. Below this value, the SCR will turn off by reverting to the forward blocking state. This transition point between positive and negative resistance is represented by the valley indicated in Figure 6.8, i.e., the current at which minimum forward voltage drop occurs. It is very difficult to match SCR's satisfactorily for identical characteristics in this region, particularly over wide ranges of temperature. This poses no problem when the gate signal is supplied to the parallel

SCR's throughout the anode conduction period, since any instability in current-sharing or a tendency of one SCR to turn off will not overheat the other device(s) in parallel because of the low current level in the region of the valley. As long as gate current is maintained, an SCR with a tendency to turn off at low anode current levels will switch into conduction again as soon as the total load current moves out of this valley area. It will thus assume its share of the load before overloading on its partner can occur. When a pulse type of gate signal is employed for triggering paralleled SCR's, instability may be encountered at low anode current levels which may have serious consequences if high levels of current follow. Pulsed gate signals are typical of unijunction transistor triggering circuits and some types of saturable reactor triggering schemes. Unless the total load current has reached a sufficiently high level to keep all of the parallel cells above the valley point by the time the gate pulse is removed, a cell such as A in Figure 6.8 will turn off. In the absence of any further gate signal, it will remain in the non-conducting state through the remainder of that cycle, thus failing to carry its share of the load. This phenomenon is likely to occur when operating at very large conduction angles in phase controlled AC circuits and when triggering from reactive lines or into inductive loads where the buildup of load current to normal levels is restrained by the inductive effect.[5]

For the above reasons use of a maintained gate signal is recommended for triggering parallel SCR's whenever possible. (See Section 4.15.)

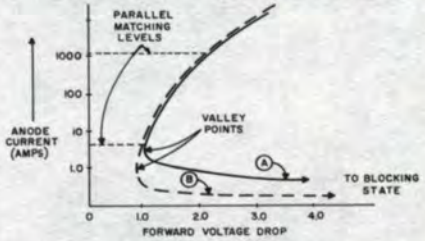


Figure 6.8 Anode Voltage-Current Relationship of SCR's with Matched Forward Characteristics

In cases where pulse triggering must be employed, the pulse must last until all the parallel SCR's have reached their respective latching currents at minimum temperature. A good conservative figure for the minimum total anode current prior to cessation of gate pulse for two parallel type C80 SCR's at 25°C stud temperature is 5.0 amperes. When more than two cells are paralleled, total anode current should be increased proportionately. For example, when three matched C80 SCR's are operating at low stud temperature, the total anode current should reach $(5.0 \times 3/2) = 7.5$ amps before the gate signal is removed.

The above situation is alleviated to a great extent when a paralleling saturable reactor is used because it can be designed to force current sharing until total anode current reaches a value high enough to maintain all cells in conduction. Once the cells are in full conduction, the reactor may saturate and become ineffective for the remainder of that particular cycle.

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3. "Operation of Unmatched Rectifier Diodes in Parallel Without Artificial Balancing Means," A. Ludbrook, IEEE CP 63-1169.
4. "Current Balancing Reactors for Semiconductor Rectifiers," I. K. Dortort, AIEE TP 59-219.
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Static Switching Circuits

7.1 INTRODUCTION

Since the SCR is a bistable device, one of its broad areas of application is in the realm of signal and power switching. This chapter describes circuits in which the SCR is used to perform simple switching functions of a type that might also be performed non-statically by various mechanical and electromechanical switches. In these applications the SCR is used to open or close a circuit completely, as opposed to applications in which the SCR is used to control the magnitude of average voltage or energy being delivered to a load. These latter types of applications are covered in detail in succeeding chapters.

Static switching circuits can be divided up into two main categories, those that operate from an AC supply where reversal of the line voltage turns off the SCR(s), and those that operate from a DC supply where the SCR(s) must be turned off by one of the methods described in Chapter 5. In AC applications, the maximum frequency of operation is limited to approximately 30 kc/s by the turn-off time requirements of the SCR. Above these frequencies standard SCR's, whose turn-off time may be as high as 25–35 microseconds, may not recover their blocking ability between successive cycles of the supply. In DC applications where the circuit turn-off time* is limited, special inverter SCR's such as the C9, C12, C40 or C55 may be required. These types have tested maximum turn-off time specifications.

* Time that circuit keeps the SCR reverse biased.

7.2 STATIC AC SWITCHES

7.2.1 "Back-to-Back" or Inverse Parallel SCR Connection

The circuit of Figure 7.1 provides high speed switching of AC power loads, and is ideal for applications with a high duty cycle. It eliminates completely the contact sticking, bounce, and wear associated with conventional electro-mechanical relays, contactors, etc. As a substitute for control relays, the SCR overcomes the differential problem, that is the spread in current or voltage between pickup and dropout, because the SCR effectively drops out every cycle. Also, providing resistor R is chosen correctly, the circuit is operable over a much wider voltage range than is a comparable relay. Resistor R is provided to limit gate current peaks. Its resistance (which can include any "contact" resistance of the control device and load resistance) should be just greater than the peak supply voltage divided by the peak gate current rating of the SCR. If R is made too high, the SCR's may not trigger at the beginning of each cycle, and "phase control" of the load will result with consequent loss of load voltage and waveform distortion. The control device indicated can be either electrical or mechanical in nature. Light dependent resistors, magnetic cores, and magnetic reed switches are all suitable control elements. In particular, the use of hermetically sealed reed switches as control elements in combination with SCR's offers many advantages. The reed switch can be actuated by passing AC or DC current through a small winding around it, or by the proximity

of a small magnet. In either case complete electrical isolation exists between the control signal input, which may be derived from many sources, and the switched power output. Long life is assured the SCR/reed switch combination by the minimal volt-ampere switching load placed on the reed switch by the SCR triggering requirements. The SCR ratings determine the amount of load power that can be switched.

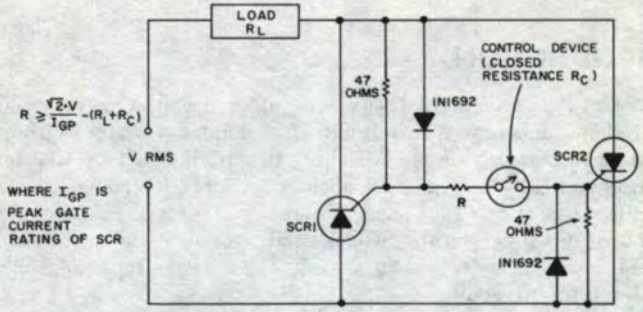


Figure 7.1 Inverse-Parallel, or Back-to-Back, Static AC Switch

7.2.2 Back-to-Back Pair With Separate Trigger Source

Where DC isolation between control signal input and load is desired *without* the use of a mechanical switch, light, or saturable core intermediary, or where a widely varying AC supply precludes satisfactory "anode triggering" of the type shown in Figure 7.1, a back-to-back pair of SCR's may be triggered from a separate source as shown in Figure 7.2. Here, the high frequency output of a transistor blocking oscillator, or a UJT free-running oscillator is transformer coupled to the SCR gates. Suitable oscillator circuits are discussed in Section 4.16. For minimum load waveform distortion and minimum generated RFI, oscillator frequency should be high enough to ensure that the SCR's trigger early in the AC cycle. Other types of UJT trigger circuits suitable for use with AC static switching arrays are described in Section 8.4.1.

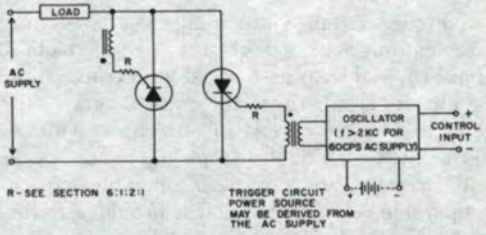


Figure 7.2 Oscillator Driven AC Static Switch

7.2.3 Alternate Connections For Full Wave AC Static Switching

Full wave static AC switching can also be performed by various combinations of SCR's and conventional rectifiers. The most useful of these arrays are shown in Figure 7.3.

The circuit of Figure 7.3(a) uses a single SCR connected across the DC output of a rectifier bridge, to switch an AC load connected in series with the supply line. The bridge rectifies the incoming AC to full wave pulsating DC, so that one SCR can control both half cycles of the AC. In this circuit the SCR turns off at the end of each half cycle when the supply voltage is zero. Unsmoothed DC can be made to flow in the load, if desired, by removing the load from the AC supply line, and placing it in series with the SCR as shown in Figure 7.3(b). In this case, for proper commutation of the SCR, a "free-wheeling" diode must be connected across the load if the load is at all inductive. The circuit of Figure 7.3(c) uses two SCR's and two rectifiers to switch an AC load, SCR1 and CR1 conducting on one half cycle of the supply, SCR2 and CR2 conducting on the other. The "DC load" equivalent to Figure 7.3(c) is shown in Figure 7.3(d), and in this arrangement the free-wheeling diode may be omitted with inductive loads. Unlike the circuit of Figure 7.1, all the static switching configurations of Figure 7.3 may be triggered directly by a single-ended (DC) non-isolated control signal, because the SCR cathodes are tied together. In low voltage switching applications, the multiple voltage drops in series with the load may be a disadvantage.

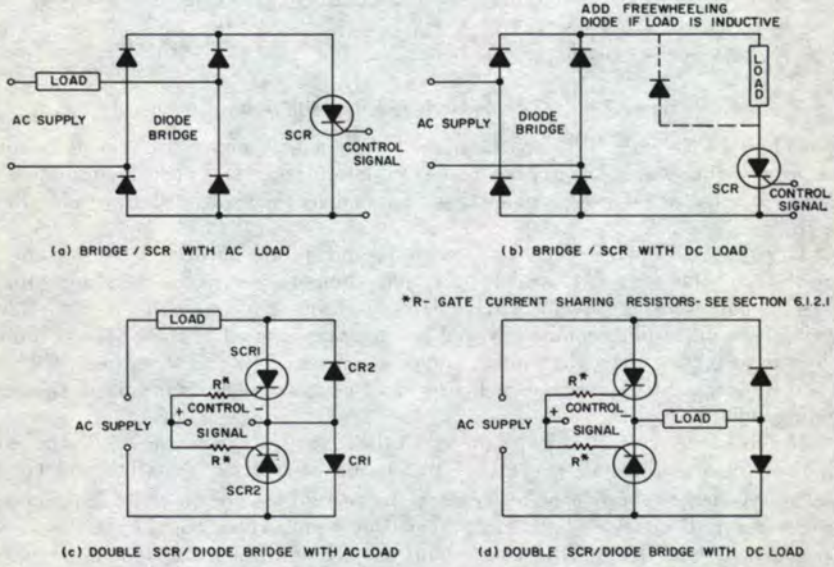
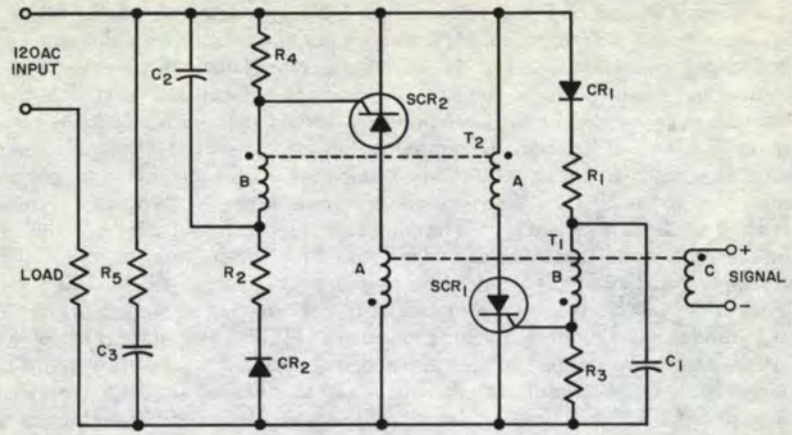


Figure 7.3 SCR/Diode Static Switch Configurations

7.3 AC STATIC CONTACTOR AND LATCHING RELAY

By combining the characteristics of square-loop core materials with the SCR, many useful circuits can be developed. Figure 7.4 uses two small toroidal cores in conjunction with two back-to-back SCR's in a variation of Figure 7.1 to secure a direct analogy to a single pole electromechanical latching relay with an electrically isolated solenoid or, with slight modification, an analogy to a conventional electromechanical non-latching relay.



R_1, R_2	10K, 1 WATT
R_3, R_4	10 OHMS, 1/2 WATT
R_5	15 OHMS, 1 WATT
C_1, C_2	0.25 MFD, 200 VOLTS
C_3	0.5 MFD, 600 VOLTS
SCR_1, SCR_2	G-E C35B OR C11B
CR_1, CR_2	G-E IN1695

T_1	MAGNETICS, INC ORTHONOL CORE #50007-1A A 5 TURNS - #14 AWG B 200 TURNS - #28 AWG C 100 TURNS - #28 AWG
T_2	MAGNETICS, INC ORTHONOL CORE #50007-1A A 5 TURNS - #14 AWG B 200 TURNS - #28 AWG

Figure 7.4 AC Static Latching Relay with Isolated Input

When SCR_1 and SCR_2 are furnished with a gate signal, they will conduct and supply full wave AC to the load, thus simulating the closed contacts of a relay or contactor. If no gate signal is supplied to the SCR's, the switch will be "open."

During the "open" state, both core T_1 and T_2 are saturated by the flow of curent from the main AC supply through their respective B windings during alternate halves of the cycle. This current is limited by resistors R_1 and R_2 respectively. Under these conditions, the gate voltage applied to the SCR's is limited to less than 0.25 volt by the voltage-dividing action of R_1 and R_3 across SCR_1 and R_2 and R_4 across SCR_2. Neither SCR fires, and no current flows in any of the reset windings of the cores.

If a low level voltage is now applied to the "Signal" C winding of T_1, this core will reset during the half cycle that the anode of SCR_1 is negative and CR_1 is blocking. When the anode of SCR_1 starts to swing positive on the following half cycle, winding B on T_1 will sustain part of the supply voltage and capacitor C_1 will charge through CR_1 and R_1. After about 1 or 2 milliseconds, depending on its design, core T_1 will saturate, discharging C_1 through the gate of SCR_1 and firing it. Current will flow from the line through SCR_1 to the load.

The gate triggering circuit on SCR_2 is identical to that on SCR_1 except no separate "Signal" winding is used. Core T_2 depends on current through its winding A to reset the core and thus permit triggering of SCR_2. Thus, if SCR_1 is triggered by the foregoing sequence, anode current in SCR_1 will reset T_2 and SCR_2 will trigger on the following half cycle. Full wave voltage will be delivered to the load.

With winding A on T_1 connected in the anode circuit of SCR_2, T_1 will in turn be reset by the anode current through SCR_2. Thus, once conduction has been initiated in SCR_1 by a positive pulse on the "Signal" winding of T_1, the switch will remain "closed" even though no further signal is applied to the input. The switch

may be turned off by a negative pulse on the "Signal" winding of T_1. This prevents winding A from resetting T_1, and SCR_1 is in turn not triggered on the following half cycle. This interruption of load current stops the reset action on T_2 as well, and the circuit reverts to the "open" state.

In this mode of operation, the circuit behaves like a latching relay. Once it has been turned on, it remains in the conducting state even though the main line voltage is interrupted for long periods of time. In other words, as a latching relay this circuit "remembers" whether it was open or closed even through power interruptions. Positive reset action requires that a minimum load current flow whenever the circuit is closed. For the design in Figure 7.2, this minimum current is approximately one ampere. A lower load current can be sustained by use of a bleeder across the load or by increasing the number of turns in the A windings.

A direct analogy to a conventional single pole contactor can be derived by eliminating the A winding on T_1. With this change, load current will not reset T_1, and a continuous positive DC signal on winding C of T_1 will be necessary to keep the contactor closed. The contactor will open within one cycle after this DC signal has been removed. Sensitivity of the switch to a control signal can be improved by increasing the number of turns on the C winding.

C_3 and R_5 serve as a filter to prevent line voltage transients from triggering the switch. They also assist in completing reset action of the cores in the latching mode if the line voltage is interrupted at a critical part of the cycle. The impedance of the switch in the "open" state is fixed by the impedance of R_5 and C_3 at the line frequency.

7.4 "ONE SHOT" SCR TRIGGER CIRCUIT

A circuit to trigger an SCR for one complete half cycle only of the AC supply is shown in Figure 7.5. Triggering is initiated by closing push button switch S1, and the SCR triggers always *near the beginning* of a positive half cycle, even although the switch may be closed randomly at any time during the two preceding half cycles. The SCR will not trigger again until S1 is opened and then reclosed. This type of logic is required for some test equipment supplies and for the solenoid drives of electrically operated stapling guns, impulse hammers, etc, where load current must flow for one complete half cycle only.

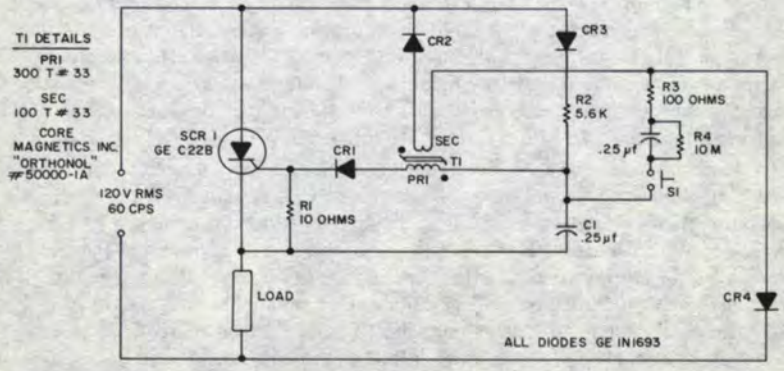


Figure 7.5 "One Shot" Trigger Circuit

During half cycles of the AC supply when the SCR anode is positive, current will flow through CR_3 and R_2. If the core of transformer T_1 *is not* saturated, its primary winding will have a high impedance, and capacitor C_1 will charge. When the time integral of the resultant voltage across T_1's primary is sufficient to produce core saturation, C_1 will discharge through the saturated impedance of T_1, and trigger SCR_1. If on the other hand, the core of T_1 *is in* saturation at the beginning of the positive half cycles, C_1 will be unable to charge, and SCR_1 will not trigger *providing*:

$$\frac{R1}{(R1+R2)} < \frac{V_{GT}(min)}{\sqrt{2}E_{AC}}$$

where $V_{GT}(min)$ is the minimum gate voltage to trigger SCR_1
E_{AC} = RMS line voltage

Normally the core of T_1 *will be* in saturation at the start of each positive half cycle because diodes CR_1 and CR_3 prevent the flow of negative reset current through T_1's primary winding. When switch S_1 is closed however, current is able to flow through CR_2, R_3 and T_1's *secondary* winding to charge capacitor C_2, and this current resets the core. On the next half cycle with T_1 initially unsaturated, C_1 charges, T_1 saturates again and SCR_1 triggers. While the load is energized, diode CR_4 conducts and charges C_2 up to the peak line voltage, in case S_1 had closed late during the previous half cycle and prevented C_2 from charging fully then. With C_2 fully charged, reset current can no longer flow, and the core will remain in saturation even if S_1 is held closed. Reset can only be accomplished when S_1 is opened, C_2 allowed to discharge through R_4, and S_1 reclosed. R_4 must be large enough to prevent C_2 discharging between successive negative half cycles. This condition is satisfied if

$$R4 > \frac{\sqrt{2}E_{AC}}{I_M \cdot R3 \cdot C2 \cdot f}$$

where I_M is the magnetizing current of T_1 sec.
f is the line frequency

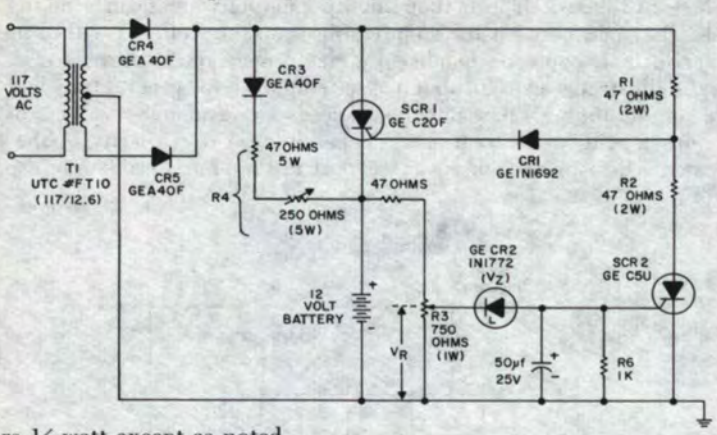
The maximum repetition rate of the circuit is limited by the discharge time constant $C_2 \cdot R_4$. Diode CR_1 prevents ringing between T_1's inductance and C_1 when T_1 saturates. In some cases CR_1 can be eliminated.

7.5 BATTERY CHARGING REGULATOR

Figure 7.6 illustrates an inexpensive means of utilizing the SCR as a battery charging regulator, thus eliminating the problems inherent in electromechanical voltage relays—contact sticking, burning, wide range of pickup and drop out, wear, etc. As shown the circuit is capable of charging a 12 volt battery at up to a six ampere rate. Other voltages and currents, from 6 to 600 volts and up to 300 amperes, can be accommodated by suitable component selection.[1] When the battery voltage reaches its fully charged level, the charging SCR shuts-off, and a trickle charge as determined by the value of R_4 continues to flow.

CR_4 and CR_5 deliver full-wave rectified DC to SCR_1 in series with the battery to be charged. With the battery voltage low, SCR_1 is triggered on each half cycle via resistor R_1 and diode CR_1. Under these conditions, the pick-off voltage V_R at the wiper of potentiometer R_2 is less than the breakdown voltage V_Z of zener diode CR_2, and SCR_2 cannot fire. As the battery approaches full charge, its terminal voltage rises, the magnitude of V_R equals V_Z (plus gate voltage required to fire SCR_2), and SCR_2 starts to trigger each half cycle. At first SCR_2 fires at $\pi/2$ radians after the start of each half cycle, coincident with peak supply voltage, peak charging current and maximum battery voltage. As the battery voltage climbs yet higher as charging continues, the firing angle of SCR_2 advances each half cycle until eventu-

ally SCR_2 is firing *before* the input sine wave has sufficient magnitude to fire SCR_1. With SCR_2 on first in a half-cycle, the voltage divider action of R_1 and R_2 keeps CR_1 back-biased, and SCR_1 is unable to fire. Heavy charging then ceases. Diode CR_3 and resistor R_4 may be added, if desired, to trickle charge the battery during the normal "off" periods. Heavy charging will recommence automatically when V_R drops below V_Z and SCR_2 stops firing each cycle.



All resistors ½ watt except as noted.

Figure 7.6 Battery Charging Regulator

7.6 OVERVOLTAGE PROTECTION ON AC CIRCUITS

The SCR makes possible some interesting protective circuits that capitalize on the fast switching speed and high current-carrying ability of these semi-conductors. Figure 7.7 illustrates a method by which SCR's may be used as a substitute for a dynamic braking contactor to protect a rectifier equipment feeding a regenerative load as typified by a DC shunt motor. An SCR in series with a current limiting resistor R is connected across each of two of the rectifier legs adjacent to one of the AC lines. Under normal operation, neither SCR_1 nor SCR_2 conducts and

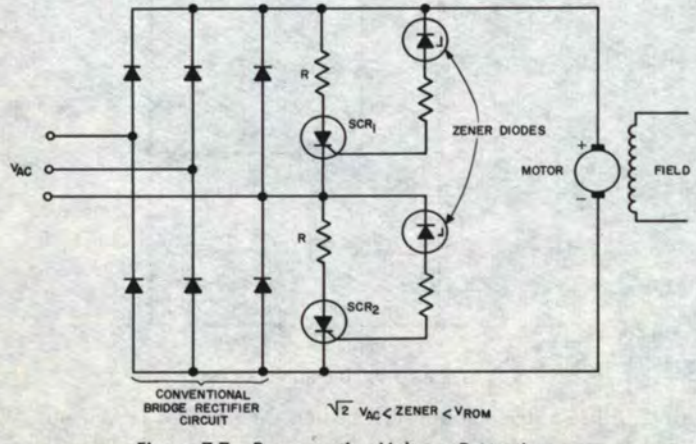


Figure 7.7 Regenerative Voltage Protection

no energy is lost in the resistors. However, when the DC bus voltage rises to a point determined by the avalanche voltage of the regulating diodes, SCR_1 and SCR_2 are fired, connecting the resistors across the bus thus preventing the DC voltage from damaging the rectifier equipment. As soon as the DC bus voltage drops below the AC supply, SCR_1 and SCR_2 are commutated by the AC line and return to their non-conducting state.

Since SCR's switch into their highly conductive state in a matter of microseconds, they can be used for suppressing transient voltages with a much higher rate of rise than could be handled by electromechanical devices such as relays. Figure 7.8 illustrates a circuit that may be employed for general transient protective service on AC lines. When the line exceeds the avalanche voltage of the zener diode, either SCR_1 or SCR_2 triggers, depending on the polarity of the AC line at that instant. Resistor R_1 limits the current to the short term surge capabilities of

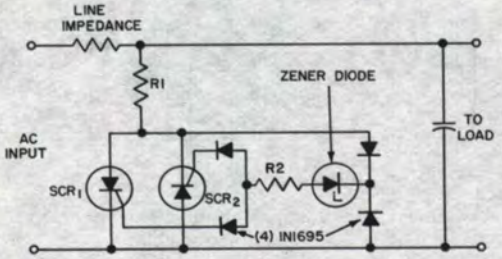


Figure 7.8 Transient Voltage Protection Using Silicon Controlled Rectifiers

the SCR's. For the C35, R_1 must limit the one cycle peak current to less than 150 amperes. This loading effect on the circuit drops the transient voltage across line impedance. Alternation of the AC line voltage turns off the current through the conducting SCR at the end of the cycle.

7.7 DC STATIC SWITCH

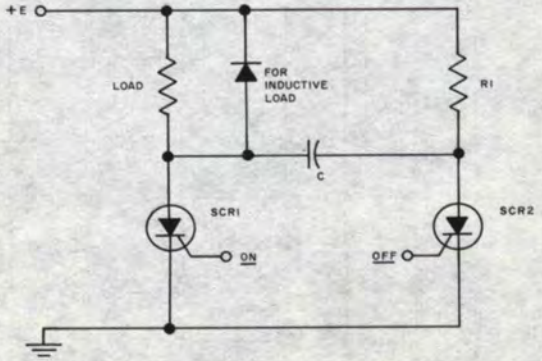


Figure 7.9 DC Static Switch

Figure 7.9 illustrates a static SCR switch for use in a DC circuit. When a low power signal is applied to the gate of SCR_1, this SCR is triggered and voltage is

applied to the load. The right hand plate of C charges positively with respect to the left hand plate through R_1. When SCR_2 is triggered on, capacitor C is connected across SCR_1, so that this SCR is momentarily reverse biased between anode and cathode. This reverse voltage turns SCR_1 off and interrupts the load current, provided the gate signal is not applied simultaneously to both gates.

SCR_1 should be selected so that the maximum load current is within its rating. Since SCR_2 need conduct only momentarily during the turn-off action, it can be smaller in rating than SCR_1. The minimum value of commutating capacitance C can be determined by the following equations:

$$\text{For Resistive Load: } C \geq \frac{1.4\ t_{off} I}{E}\ \mu fd \qquad (7.1)$$

$$\text{For Inductive Load: } C \geq \frac{t_{off} I}{E}\ \mu fd \qquad (7.2)$$

Where t_{off} = Turn-off time of SCR in μ seconds (See specification for inverter-type SCR)

I = Maximum load current (including possible overloads) in amperes at time of commutation

E = Minimum DC supply voltage

The resistance of R_1 should be ten to one hundred times less than the minimum effective value of the forward blocking resistance of SCR_2. This latter value can be derived from the published leakage current curves for the SCR under consideration.

In some cases a mechanical switch may be substituted for SCR_2, to turn off SCR_1 when it (the switch) is momentarily closed. Many other useful variations of this basic DC static switch can be devised, among them the following circuits.

7.8 DC LATCHING RELAY AND POWER FLIP-FLOP

By replacing resistor R_1 with a second driven load, and selecting SCR_2 to suit, the circuit of Figure 7.9 becomes the static analog of a single pole double throw latching relay. In this case commutating capacitor C should be selected on the basis of the heavier of the two loads. By driving the gates with a train of pulses as shown in Figure 7.10, the circuit becomes a high power flip-flop or multivibrator. Sine wave or square wave sources may also be used to drive the gates in this configuration.

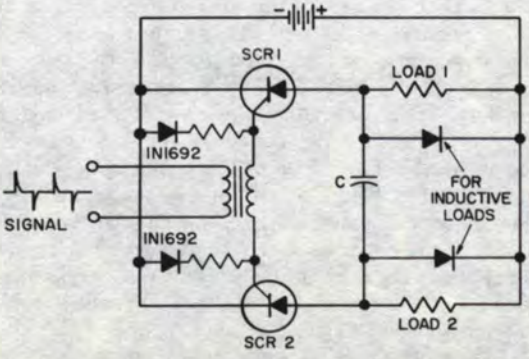
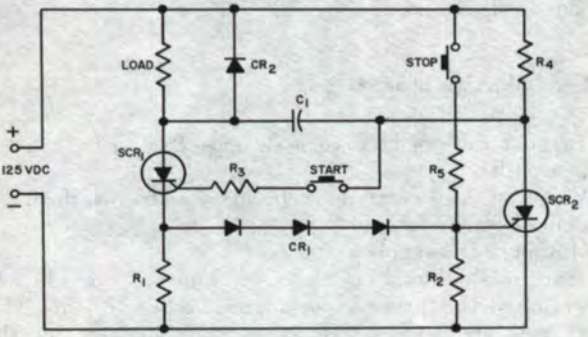


Figure 7.10 Power Flip-Flop and Latching Relay

7.9 SCR CURRENT-LIMITING CIRCUIT BREAKERS

In some phase controlled applications, the fault current due to a short circuit may reach destructive proportions within one-half cycle. This would prohibit use of conventional circuit breakers for protection. Also, in some types of inverters operating on DC it may be desirable to have a fast electronic circuit breaker in the event of loss of commutation in the inverter for any reason.

An SCR current limiting circuit breaker of the type shown in its simplest form in Figure 7.11 will provide these protective fuuctions very nicely. This package



$R_1 \cong 3/I_{trip}$ OHMS NON-INDUCTIVE
R_2—220 OHMS, 1/2 WATT
R_3—100 OHMS, 1/2 WATT
R_4—2200 OHMS, 10 WATTS
R_5—2200 OHMS, 5 WATTS
$C_1 \cong 0.4 I_{trip}$ MFD
SCR_1, SCR_2 – G.E. C40B
CR_1 – (3) G.E. IN1692
CR_2 – G.E. IN2158

Figure 7.11 16 Ampere DC Circuit Breaker

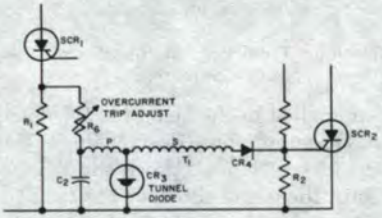
can be inserted in series with the DC output of a phase-controlled rectifier or in series with the DC input to an inverter circuit.

The circuit breaker is basically a parallel capacitor commutated flip-flop. When the "Start" button is momentarily depressed, SCR_1 starts to conduct and delivers power to the load provided the load current is above the minimum holding current of SCR_1. Capacitor C_1 then charges to the load voltage through R_4, the right hand terminal of C_1 being positive with respect to the left hand terminal. When SCR_2 is fired by momentary closing of the "Stop" button, the positive terminal of capacitor C_1 is connected to the cathode of SCR_1, reversing the polarity across this SCR and turning it off. This interrupts the flow of load current and opens the circuit. SCR_2 will also be fired by the voltage developed across R_1 by load current if this exceeds the forward voltage drop of the string of series diodes CR_1 plus the gate firing requirements of SCR_2. By adjustment of the value of R_1 and by selecting the proper number of series diodes CR_1, the circuit can be made to trip out and interrupt overload or fault current at any predetermined level. For a more consistent tripping level under temperature variations, a zener diode can be substituted in place of all but one of the series diodes at CR_1. For still more precise tripping, a UJT overcurrent sensor can be used.

The characteristics of the germanium tunnel diode are also very useful in developing a gate signal when a specific level of current is exceeded. The tunnel

diode has a very stable peak current at which it switches from a low resistance to a relatively high resistance. This, combined with a very low voltage drop makes it almost ideal for this type of application. A tunnel diode overcurrent detecting network for the circuit breaker of Figure 7.11 is shown in Figure 7.12. Main load current flows through SCR_1 and R_1. Part of the load is shunted through R_6, tunnel diode CR_3, and the primary winding of T_1, R_1 and R_6 are selected so that less than ½ amp flows through the tunnel diode at maximum rated load. Under this condition CR_3 remains in its low resistance state. If the main load current rises to the point where more than ½ amp flows through CR_3, it switches instantaneously to its high resistance state. If the current through the tunnel diode is maintained constant through the switching interval, the voltage across it increases about five-fold. This sudden change in voltage across CR_3 induces a pulse of voltage in the primary of T_1 which is stepped up by autotransformer action and applied to the gate of SCR_2, thereby tripping the circuit breaker. The tripping point is stable within a few percent over a wide temperature range and is independent of the firing characteristics of SCR_2.

The component values in Figure 7.11 apply for a 125 volt DC system. When using the C40 SCR, the tripping current level should not exceed 100 amperes in order to stay within the switching rating of SCR_2.



R_1 — $=3/I_{trip}$ -OHMS, NON-INDUCTIVE
R_2 — 47 OHMS, 1/2 WATT
R_6 — 10 OHM, LINEAR POT
C_2 — 2 MFD, 200 VOLT
CR_3 — GERMANIUM TUNNEL DIODE WITH I_{PK} = 0.5A
CR_4 — G.E. IN91
T_1 — AIR CORE TRANSFORMER, 1/4" DIA., P = 50T, S = 500T, #26 AWG

Figure 7.12 Tunnel Diode Sensing Network For Figure 7.10

Because of the fast switching action of SCR's, short circuit current can be interrupted long before it reaches destructive levels. In typical stiff systems with rates of fault current rise on the order of 10 million amperes per second, this type of switch has limited the peak fault current to less than 50 amperes and has interrupted the fault in as little as 20 microseconds after its inception.

In some high reliability applications the flip-flop action of this circuit can be used as a high speed transfer switch in the event of a fault in one load. For instance, both the load in series with SCR_1 and the load represented by R_4 in Figure 7.11 could be DC motors, driving a common load. If the main drive motor in series with SCR_1 should fail short, it would be disconnected from the line and power would be applied to the standby motor R_4 within a matter of microseconds after the fault occurred.

C_1 must have sufficient capacitance to commutate the fault current at the point of tripping. Expressed another way, it must reverse bias SCR_1 for at least 12 microseconds if SCR_1 is to reliably recover its open state and block further flow of fault current. If SCR's other than the C40 are employed in this circuit C_1 must be adjusted to provide the necessary turn-off time for the particular SCR type chosen.

7.10 HIGH SPEED SWITCH OR "ELECTRONIC CROWBAR"

A form of "electronic crowbar," shown in Figure 7.13 has proved very useful for protecting DC circuits against input line voltage transients and short circuit load conditions. If the DC supply exceeds the desired maximum value as determined by the setting of potentiometer R_1, the voltage at the emitter of UJT_1 exceeds the peak point voltage causing UJT_1 to fire which in turn triggers the SCR. The

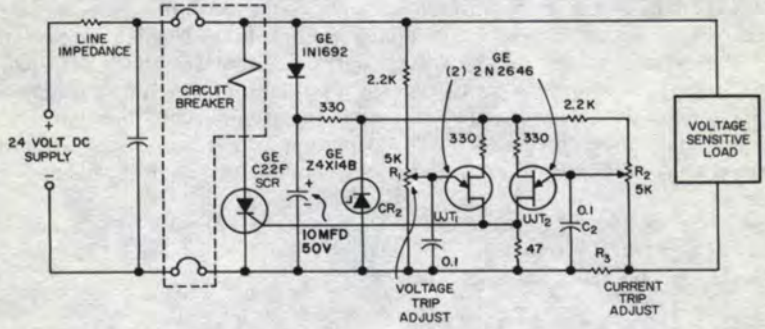


Figure 7.13 Electronic Crowbar Protection of DC Circuits Against Overvoltage and/or Overcurrent

full supply voltage is then applied to the circuit breaker trip coil causing the circuit breaker to open the main DC supply bus. Besides increasing the speed of the circuit breaker action this circuit instantly loads down the DC bus, preventing the voltage on the load from rising until the circuit breaker has time to operate. The circuit also protects the load and the supply against short circuit conditions by monitoring the current through resistor R_3. When the voltage across R_3 exceeds the desired maximum value as determined by the setting of potentiometer R_2 the voltage at the emitter of UJT_2 exceeds the peak point voltage, causing UJT_2 and the SCR to fire as before. Due to the stable firing voltage of the UJT the trip voltage across R_3 can be very low, a value in the range from 100 millivolts to 500 millivolts being suitable for most applications. If only overvoltage protection is desired the circuit of Figure 7.13 can be simplified by eliminating UJT_2 and its associated circuitry. Similarly, if only overcurrent protection is desired UJT_1 and its associated circuitry can be eliminated.

In the circuit of Figure 7.13 rectifier CR_1 and capacitor C_3 are used to provide filtering against negative voltage transients which would otherwise result in false tripping of the circuit. The values of potentiometer R_1 and R_2 are chosen to have appropriate time constants with C_1 and C_2 so as to give the desired voltage-time response in the tripping action.

The SCR is ideal for this type of circuit because of its ability to switch on within a few microseconds after being triggered.

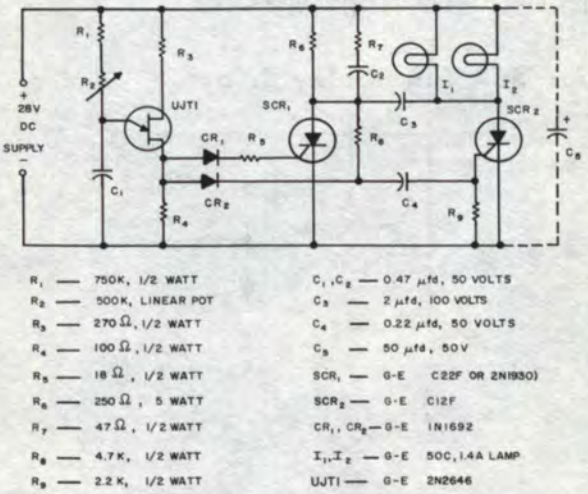
For higher capacity circuits, the C35F or C50F SCR's can be substituted for the C22F shown. With the C50F SCR this circuit is capable of carrying momentary currents as high as 2000 amps for 2 milliseconds without damage to the SCR.

7.11 FLASHER CIRCUIT

Flasher circuits for incandescent lamps are widely used in a variety of applications such as traffic lights, navigational beacons, aircraft beacons and illu-

minated signs. The SCR is ideally suited for this type of application since it can function over a wide range of current and voltage with a much higher degree of reliability than the commonly used electromechanical systems. The SCR also offers an advantage over power transistors in that it does not require an excessive derating of current in order to handle the high inrush currents of incandescent lamps. The UJT makes an ideal partner for the SCR in this type of application since it permits an economical method for obtaining a wide frequency range and a high degree of frequency stability.

The circuit shown in Figure 7.14 has been chosen to illustrate the basic principles of an SCR/UJT flasher which can be easily simplified or modified to meet specific application requirements. The circuit as shown operates a lamp load of up to 3 amperes over a supply voltage range of 17 to 35 volts and a temperature range of $-50°C$ to $100°C$. This circuit is basically a parallel inverter with capacitor commutation. The SCR's conduct alternately and are triggered by the free running UJT relaxation oscillator. The frequency of the relaxation is determined by the time constant, $(R_1 + R_2)\ C_1$, and may be adjusted to the value desired by means of potentiometer R_2.



R_1	750K, 1/2 WATT	C_1, C_2	0.47 μfd, 50 VOLTS
R_2	500K, LINEAR POT	C_3	2 μfd, 100 VOLTS
R_3	270 Ω, 1/2 WATT	C_4	0.22 μfd, 50 VOLTS
R_4	100 Ω, 1/2 WATT	C_5	50 μfd, 50V
R_5	18 Ω, 1/2 WATT	SCR_1	G-E C22F OR 2N1930)
R_6	250 Ω, 5 WATT	SCR_2	G-E C12F
R_7	47 Ω, 1/2 WATT	CR_1, CR_2	G-E 1N1692
R_8	4.7K, 1/2 WATT	I_1, I_2	G-E 50C, 14A LAMP
R_9	2.2K, 1/2 WATT	UJT1	G-E 2N2646

Figure 7.14 High Power Electronic Flasher

Special consideration must be given to the proper starting of the circuit. When the supply voltage is first applied both SCR's are off, and if a pulse is applied to the gates of both SCR's simultaneously they will both turn on and the circuit will fail to function. This problem is overcome by means of the gating action of CR_2, R_8, and C_4. If SCR_1 is off it will be turned on by the first trigger pulse, but SCR_2 will not be turned on since CR_2 is reverse biased by approximately 28 volts and hence blocks the trigger pulse from the gate of SCR_2. If SCR_1 is on, however, then CR_2 will be reverse biased by less than 1 volt so that the trigger pulse will be able to trigger SCR_2 which then turns off SCR_1 through the action of commutating capacitor C_3. In this case triggering SCR_1 and SCR_2 at the same time is permissible since the time constant R_6C_3 is much longer than the trigger pulse width so that SCR_1 remains reverse biased after the end of the trigger pulse long enough to assure reliable commutation of SCR_1.

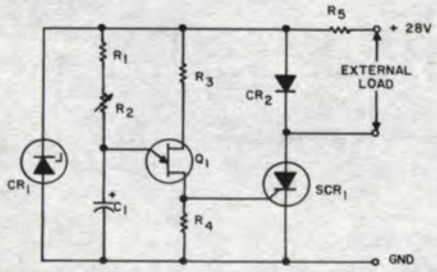
Resistor R_7 and capacitor C_2 are used in the anode of SCR_1 to furnish a higher current to SCR_1 during the commutating interval so as to prevent SCR_1 from improperly turning off due to the effect of inductance in the power supply. In some cases it may also be necessary to place a capacitor C_5 directly across the circuit as shown or to reduce the value of R_6.

For higher values of supply voltage or for greater frequency stability a Zener diode with a dropping resistor can be used to provide the bias voltage for the UJT. The circuit as shown operates the lamps at a 50% duty cycle. For operation at other values of duty cycle an appropriate value of resistance can be connected between the emitter of the UJT and the anode of one of the two SCR's. If independent adjustment of the on and off time of the load is required, a version of the hybrid timing circuit can be used (GE Transistor Manual, 6th Edition, page 199–201).

7.12 TIME DELAY CIRCUITS

Time delay circuits are used frequently in industrial controls and aircraft and missile systems to apply or remove power from a load a predetermined time after an initiating signal is applied. Cascaded time delay circuits can be used to sequentially perform a series of timed operations.

7.12.1 UJT/SCR Time Delay Relay



R_1 - 2.2K, 1/2 WATT
R_2 - 1K TO 500K LINEAR POT
R_3 - 150 Ω, 1/2 WATT
R_4 - 27, Ω, 1/2 WATT
R_5 - 560 Ω, 2 WATT
C_1 - 0.2 TO 100 mfd, 15 V
SCR_1 - G-E C22F OR C11F
CR_1 - 18 V, 10%, 1 WATT ZENER
CR_2 - G-E 1N1692
Q_1 - G-E 2N1671B

Figure 7.15 Precision Solid State DC Time Delay Circuit

Figure 7.15 illustrates an extremely simple yet accurate and versatile solid state time delay circuit. The operating current and voltage of the circuit depend only on the proper choice of the SCR. Resistor R_5 and Zener diode CR_1 provide a stable voltage supply for the UJT. Initially SCR_1 is off and there is no voltage applied to the load. Timing is initiated either by applying supply voltage to the circuit or by opening a shorting contact across C_1. The timing capacitor C_1 is charged through R_1 and R_2 until the voltage across C_1 reaches the peak point voltage of the UJT at which time the UJT fires, generating a pulse across R_4 which triggers SCR_1. The full supply voltage minus the SCR drop then appears across the external load terminals. Holding current for SCR_1 is provided by the current through R_5 and CR_2. Thus the external load may be removed or connected at any time without affecting the performance of the circuit. When SCR_1 triggers, the voltage across the UJT drops to less than 2 volts due to the clamping action of CR_2.

This acts to rapidly set and maintain a low voltage on C_1 so that the time interval is maintained with reasonable accuracy if the circuit is rapidly recycled. For the highest accuracy, however, additional means must be used to rapidly and accurately set the initial voltage on C_1 to zero at the beginning of the timing cycle. A pair of mechanical contacts connected across C_1 is ideal for this purpose.

The time delay of the circuit depends on the time constant $(R_1 + R_2)\ C_1$ and can be set to any desired value by appropriate choice of R_1, R_2, and C_1. The upper limit of time delay which can be achieved depends on the required accuracy, the peak point current of the UJT, the maximum ambient temperature, and the leakage current of the capacitor and UJT (I_{EO}) at the maximum ambient temperature. The absolute upper limit for the resistance $R_1 + R_2$ is determined by the requirement that the current to the emitter of the UJT be large enough to permit it to fire (i.e. be greater than the peak point current) or

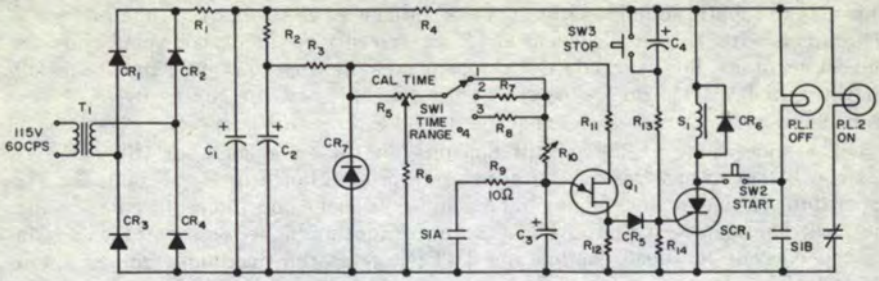
$$R_1 + R_2 < \frac{(1 - \eta)\ V_1}{\frac{25I_p}{V_1} + I_e} \qquad (7.3)$$

where η is the maximum value of intrinsic standoff ratio, V_1 is the minimum supply voltage on the UJT, I_p is the maximum peak point current measured at an interbase voltage of 25 volts, and I_e is the maximum leakage current of the capacitor at a voltage of ηV_1. If high values of capacitance are required it is desirable to use stable, low leakage types of tantalytic capacitors. If tantalytic or electrolytic capacitors are used it is necessary to consider forming effects which will cause the effective capacitance and hence the period to change as a function of the voltage history of the capacitor. These effects can be reduced by applying a low bias voltage to the capacitor in the standby condition.

The resistor R_3 can serve as a temperature compensation for the circuit, increasing the value of R_3 causes the time delay interval to have a more positive temperature coefficient. The over-all temperature coefficient can be set exactly zero at any given temperature by careful adjustment of R_3. However, ideal compensation is not possible over a wide range because of the nonlinear effects involved. To reset the circuit in preparation for another timing cycle SCR_1 must be turned off either by momentarily shorting it with a switch contact or by opening the DC supply.

7.12.2 AC Powered Time Delay Relay

Figure 7.16 illustrates a time delay circuit using a relay output with a push button initiation of the timing sequence. In the quiescent state SCR_1 is on and relay S_1 is energized. Contact S_1A is closed, shorting out the timing capacitor C_3. To initiate the timing cycle push button switch SW_2 is momentarily closed which shorts SCR_1 through contact S_1B causing SCR_1 to turn off. When SW_2 is released S_1 is deenergized and the timing sequence begins. The particular configuration of SW_2 and S_1B is used to prevent improper operation in case SW_2 is closed again during the timing cycle. Capacitor C_3 is charged through R_8 and R_{10} until the voltage across C_3 reaches the peak point voltage of Q_1 causing Q_1 to fire. The positive pulse generated across R_{12} triggers SCR_1 which pulls in the relay and ends the timing cycle. The timing cycle can be terminated at any time by push button switch SW_3 which causes current to flow in R_{13} thus triggering SCR_1. Capacitor C_4 supplies current through R_{13} during the instant after the supply is turned on thus triggering SCR_1 and setting the circuit in the proper initial state.



R_1 — 2Ω, 1 WATT
R_2, R_3 — 330Ω, 1/2 WATT
R_4 — 35Ω, 5 WATT
R_5 — 2.5K, LINEAR POT
R_6 — 25K, 1/2WATT
R_7 — 100K, 1/2%, 1/2 WATT
R_8 — 200K, 1/2%, 1/2WATT
R_9 — 10Ω, 1/2WATT
R_{10} — 100K, 10 TURN HELIPOT
R_{11} — 150Ω, 1/2 WATT
R_{12} — 18Ω, 1/2 WATT
R_{13} — 1.2K, 2 WATT
R_{14} — 100Ω, 1/2 WATT
C_1 — 500μFD, 50V
C_2 — 100μFD, 50V
C_3 — 100μFD, 20V TANTALUM
C_4 — 10μFD, 50V
SCR_1 — G-E C22F
CR_1—CR_6 — G-E IN1692
CR_7 — 18V, 10%, IWATT ZENER
Q_1 — G-E 2N1671B
S_1 — G-E CR2791GI22A4 4PDT RELAY
PL_1, PL_2 — G-E 1477, 24V LAMP
T_1 — 115V/25V 1A TRANSFORMER

Figure 7.16 Variable Time Control Circuit

The timing interval is determined by the setting of a precision ten turn Helipot R_{10} which may be set from 0.25 to 10.25 seconds in increments of 0.01 second. The initial setting of 0.25 seconds takes into account the added series resistance of the time calibration potentiometer R_5. Additional series resistance of 100K and 200K may be added by SW_1 to extend the time range by 10 seconds and 20 seconds. A fourth position of SW_1 open circuits the timing resistors and thus permits unrestricted on-off control of the circuit.

Tests of the circuit have shown an absolute accuracy of 0.5% after initial calibration and a repeatability of 0.05% or better.

7.12.3 Ultra-Precise Time Delay Relay

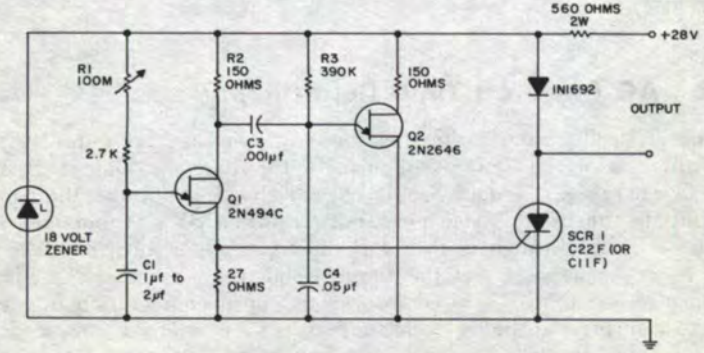


Figure 7.17 Ultra-Precise Long Period Time Delay

Predictable time delays from as low as 0.3 milliseconds to over 3 minutes are obtainable from the circuit of Figure 7.17, without resorting to a large value electrolytic-type timing capacitor. Instead, a stable low leakage paper or mylar

capacitor is used and the peak point current of the timing UJT (Q_1) is effectively reduced, so that a large value emitter resistor (R_1) may be substituted. The peak point requirement of Q_1 is lowered up to 1000 times, by pulsing its upper base with a ¾ volt negative pulse derived from free-running oscillator Q_2. This pulse momentarily drops the peak point voltage of Q_1, allowing peak point current to be supplied from C_1 rather than via R_1. Pulse rate of Q_2 is not critical, but it should have a period τ that is less than .02 ($R_1 \cdot C_1$). With $R_1 = 2000$ megohms and $C_1 = 2\ \mu f$ (mylar), the circuit has given stable time delays of over one hour. R_2 is selected for best stabilization of the firing point over the required temperature range. Because the input impedance of the 2N494C UJT is greater than 1500 megohms before it is fired, the maximum time delay that can be achieved is limited mainly by the leakage characteristics of C_1.

7.13 NANOAMPERE SENSING CIRCUIT WITH 100 MEGOHM INPUT IMPEDANCE

The circuit of Figure 7.18 may be used as a sensitive current detector, or as a voltage detector having high input impedance. A sampling technique similar to that described in the previous section is used to give an input current sensitivity (I_{IN}) of less than 35 nanoamperes. Input impedance is better than 100 megohms.

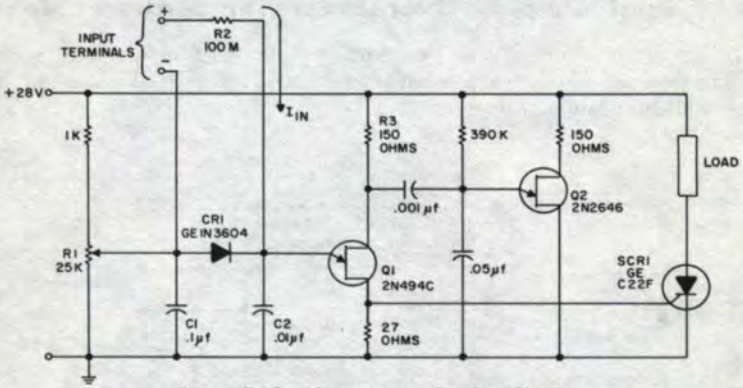


Figure 7.18 Nanoampere Sensing Circuit

Current gain between output and input of the circuit as shown is greater than (200×10^6).

Resistor R_1 is adjusted so that the circuit will not fire in the absence of the current input signal I_{IN}. I_{IN} then charges C_2 through the 100 megohm input resistor R_2 towards the emitter firing voltage of Q_1. R_2 however, cannot supply the peak point current (2 μA) necessary to fire Q_1, and this current is obtained from C_2 itself by dropping Q_1's firing voltage momentarily below V_{C2}. Relaxation oscillator Q_2 supplies a series of .75 volt negative pulses to base two of Q_1 for this purpose. The period of oscillation of Q_2 is not critical but should be less than .02 times the period of Q_1. Capacitor C_2 can be kept small for fast response time because C_1 stores the energy required to fire SCR_1. Rapid recovery is possible because both capacitors are charged initially from R_1. Some temperature compensation is provided by the leakage current of CR_1 subtracting from the leakage current of Q_1. Further compensation is obtainable by adjusting the value of R_3. A floating power supply for the UJT trigger circuit with pulse transformer coupling from Q_1 to SCR_1, enables one of the two input terminals to be grounded, where this may be desirable.

7.14 SIMPLIFIED STATIC SWITCHING CIRCUITS USING THE C5 AND C7 LOW CURRENT CONTROLLED RECTIFIERS

The C5 low current silicon controlled rectifier is a three-terminal four-layer all-diffused p-n-p-n switch, capable of carrying currents up to 1.6 amperes rms, and blocking voltages up to 400 volts. Although similar to earlier SCR's and controlled switches, this all-welded JEDEC TO-5 packaged device requires less than 800 microwatts (maximum) of input signal to switch up to ½ kw of load power. The C7 series is also available, offering increased sensitivity (< 32 microwatts) at lower anode voltage levels (200 volts maximum). Because of the high gain available between its input and output terminals, a single C5 *in free air* can control well over two hundred watts of load, taking inputs directly from such low level elements as thermistors and light-sensitive resistors; a single C7 has sufficient gain to be triggered by unamplified pulses of transmitted RF energy, or by the few microamps output current from a capacitive proximity sensor. When utilized as a gate amplifier for the higher rated SCR's, either of these TO-5 types make possible a multitude of solid-state thyratron tube analogues. The C5 SCR is also suitable for use as a very high voltage remote-base transistor. For more detailed application information on the C5 and C7 devices than presented here, see Reference 2.

7.14.1 Dual Output, Over-Under Temperature Monitor

The circuit of Figure 7.19 is ideal for use as an over-under temperature monitor, where its dual output feature can be used to drive "HIGH" and "LOW" temperature indicator lamps, relays, etc.

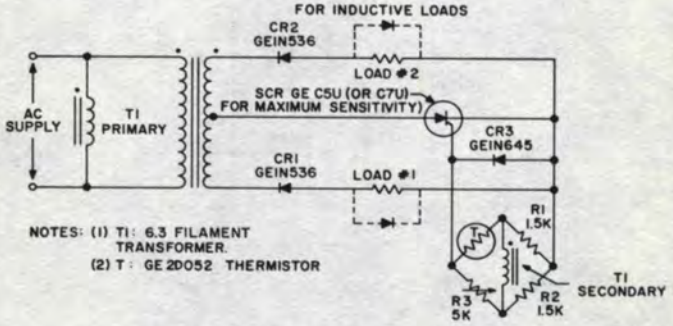


Figure 7.19 Temperature Monitor

T_1 is a 6.3 volt filament transformer whose secondary winding is connected inside a four arm bridge. When the bridge is balanced, its AC output is zero, and the C5 (or C7) receives no gate signal. The bridge's DC resistance is sufficiently low to stabilize the SCR during forward blocking periods.* If now the bridge is unbalanced by raising or lowering the thermistor's ambient temperature, an AC voltage will appear across the SCR's gate cathode terminals. Depending in which sense the bridge is unbalanced, positive gate voltage will be in phase with, or 180° out of phase with the AC supply. If positive gate voltage is in phase, SCR will deliver load current through diode CR_1 to load (1), diode CR_2 blocking current to load (2). Conversely, if positive gate voltage is 180° out of phase, diode CR_2 will

* See Section 4.5.2 "Negative Gate Biasing."

conduct and deliver power to load (2), CR_1 being reverse biased under these conditions. CR_3 prevents excessive negative voltage from appearing across the SCR's gate/cathode terminals. With component values shown, the circuit will respond to changes in temperature of approximately 1–2°C. Substitution of other variable-resistance sensors, such as cadmium sulphide light dependent resistors (LDR) or strain gauge elements, for the thermistor shown is of course permissible. The balanced bridge concept of Figure 7.19 may also be used to trigger conventional SCR-series load combinations. As a low power temperature controller for instance, a C5 could be used to switch a heater element, with a thermistor providing temperature feedback information to the trigger bridge.

7.14.2 Mercury Thermostat/SCR Heater Control

The mercury-in-glass thermostat is an extremely sensitive measuring instrument, capable of sensing changes in temperature as small as 0.1°C. Its major limitation lies in its very low current handling capability—for reliability and long life, contact current should be held below 1 mA. In the circuit of Figure 7.20 the General Electric C5B SCR serves as both current amplifier for the Hg thermostat and as the main load switching element.

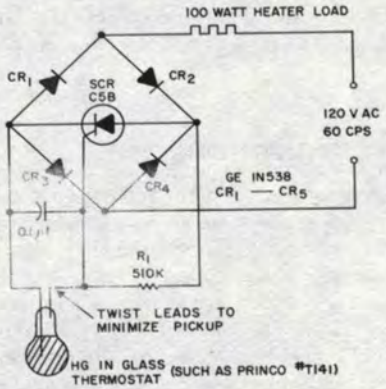
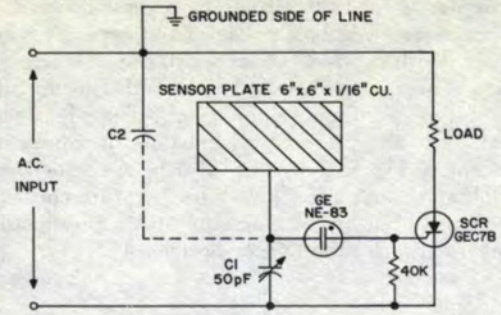


Figure 7.20 Temperature Controller

With the thermostat open, the SCR will trigger each half cycle and deliver power to the heater load. When the thermostat closes, the SCR can no longer trigger, and the heater shuts off. Maximum current through the thermostat in the closed position is less than 250 μA rms.

7.14.3 Proximity Switch

Figure 7.21 is a solid state version of the vacuum-tube proximity switch. Capacitor C_1 and the sensor plate ("capacitor" C_2) form a capacitive voltage divider connected directly across the AC supply. The AC voltage across C_1 will depend on the ratio (C_1/C_2) and the line voltage. The capacitance of C_2 in turn depends on the proximity to the sensor plate of any reasonably conductive and grounded object (metals, human body, etc.). As soon as the voltage across C_1 exceeds the breakover potential of the NE-83 neon, capacitors C_1 and C_2 discharge through the SCR gate, causing the SCR to trigger and energize the load.



NOTES: (1) C2 IS EQUIVALENT CAPACITY OF SENSOR PLATE W.R.T. GROUND.
(2) SENSOR PLATE AREA MAY BE ADJUSTED FOR REQUIRED SENSITIVITY.

Figure 7.21 Proximity Switch

Latching action can be achieved if desired by driving the SCR *anode circuit only* with DC. Since the sensitivity of the arrangement is a function both of sensing distance and sensor plate size, the plate can be made progressively smaller in area if the sensing distance is small, e.g. for a "touch–control," the sensing plate need be no bigger than a penny piece. This circuit is ideally suited for use in elevators (both for door safety controls and floor selector button arrays), supermarket door control, bank-safe monitors, flow switch actuation, and conveyor belt counting systems.

7.14.4 Thyratron Replacement

The C5 makes an ideal trigger element for the larger size SCR's. (See also section 4.15.) Such a combination possesses many of the characteristics of a thyratron gas tube. A thyratron tube is characterized by a very high signal input impedance, low pick-up and drop-out currents, and good power handling capabilities. On the other hand, it is fragile, requires filament power, is frequency limited by a long deionization time, and has a fairly high forward drop. While the solid-state equivalents to this device, using the C5, can match the thyratron in input impedance, current handling ability and low pick-up current, they possess none of the gas tube's limitations. At the present time however, the maximum forward blocking voltage attainable using a single C5 is 400 volts. This can be increased by series connecting additional SCR's (see section 6.1).

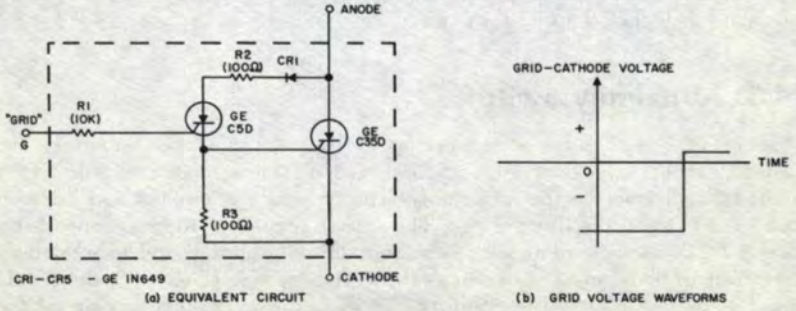


Figure 7.22 Sample Thyratron Replacement

Referring to Figure 7.22; with a negative potential on grid terminal "G", CR_1, CR_2 and the 10 k resistor provide stabilizing gate bias for the C5. When the "Grid" is driven positive however, a maximum current of 200 microamps will trigger the smaller SCR into conduction. The C35D is triggered in turn by the C5, and can conduct up to 25 amps rms load current. With the voltage grades shown, the "device" is capable of blocking voltages up to 400 volts. Over-all pick-up current is determined by the C5 rather than by the C35, a useful feature when the "thyratron" is operating into a highly inductive load. Diode CR_1 prevents transistor action in the C5 if positive grid voltage should coincide with negative anode potential.

7.15 SWITCHING CIRCUITS USING THE C5 SCR AS A REMOTE-BASE TRANSISTOR

7.15.1 "Nixie"® and Neon Tube Driver

The C5 SCR, when biased as a remote-base transistor, makes an excellent high voltage transistor suitable for driving Nixie, neon and other type of high voltage digital readout displays. Collector voltage rating of the equivalent transistor equals or exceeds the $V_{BR(FX)}$ rating of the parent SCR (400 volts) while the common emitter current gain is approximately two (2). The circuit of Figure 7.23 is self explanatory; note however the connections to the C5 terminals. Where a memory feature is desirable (pulse initiation with load remaining energized until reset externally), the same basic circuit may be used, but with the C5 connected conventionally as an SCR. See Section 11.5.3 for appropriate reset circuitry.

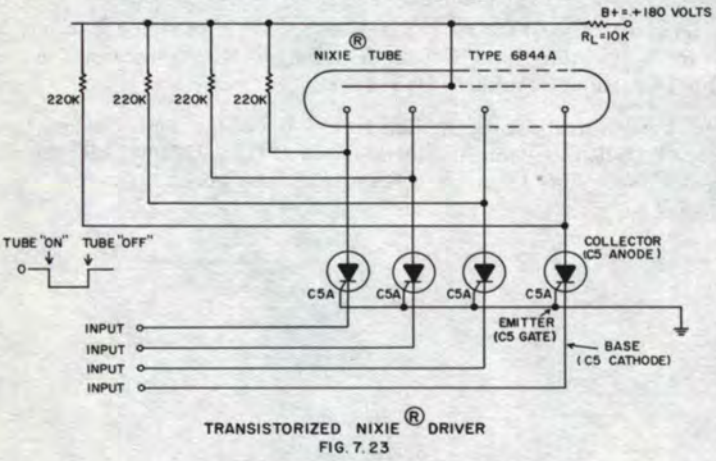
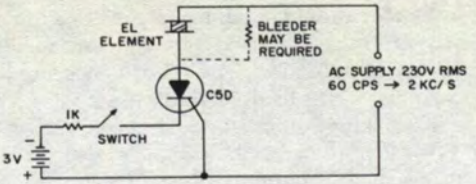


Figure 7.23 Transistorized Nixie® Driver

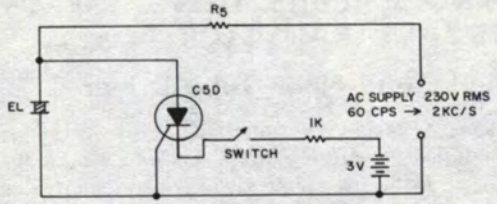
®-Trademark Burroughs Corporation.

7.15.2 Electroluminescent Panel Driver

Either of the circuits of Figure 7.24 may be used to drive the elements of an electroluminescent display panel, depending on the input logic required. Here, the high voltage capabilities of the C5 SCR are again combined with its usefulness as a transistor, in this case a *symmetrical* transistor.



(a) SERIES DRIVE - NO SIGNAL, DISPLAY "OFF"



(b) SHUNT DRIVE - NO SIGNAL, DISPLAY "ON"

Figure 7.24 Electroluminescent Panel Driver

REFERENCES:

1. "Regulated Battery Chargers Using The Silicon Controlled Rectifier", D. R. Grafham, Application Note 200.33, General Electric Company, Rectifier Components Department, Auburn, New York.

2. "Using Low Current Silicon Controlled Rectifiers and Silicon Controlled Switches," D. R. Grafham, Application Note 200.19, General Electric Company Rectifier Components Department, Auburn, New York.

8.1 PRINCIPLE OF PHASE CONTROL

"Phase Control" is the process of rapid ON-OFF switching which connects an AC supply to a load for a controlled fraction of each cycle. This is a highly efficient means of controlling the average power to loads such as lamps, heaters, motors, DC supplies, etc. Control is accomplished by governing the phase angle of the AC wave at which the SCR is triggered. The SCR will then conduct for the remainder of that half-cycle.

There are many forms of phase control possible with the SCR, as shown in Figure 8.1. The simplest form is the half-wave control of Figure 8.1(a) which uses one SCR for control of current flow in one direction only. This circuit is

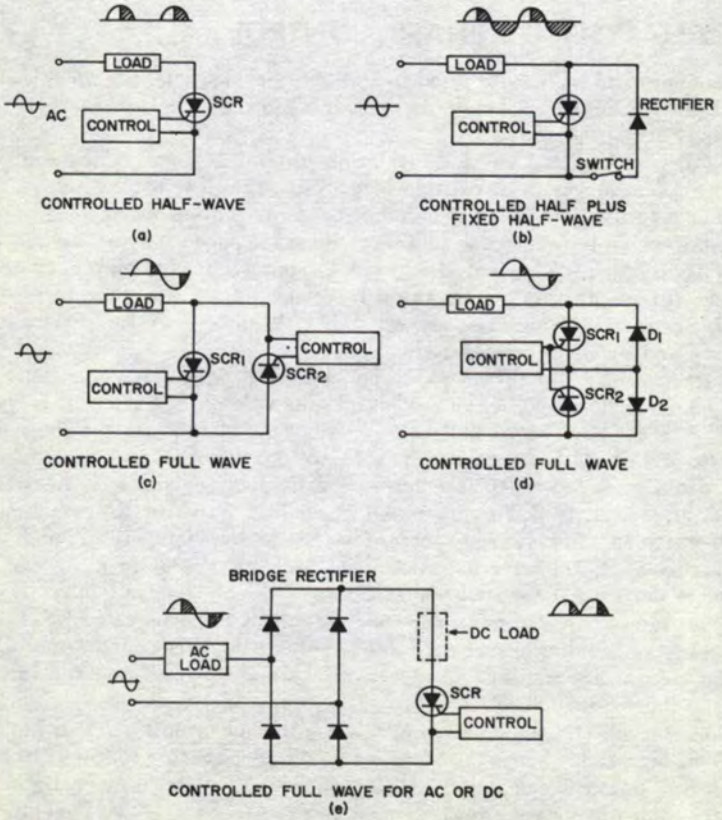


Figure 8.1 Five Basic Forms of AC Phase Control

used for loads which require power control from zero to one-half of full-wave maximum and which also permit (or require) direct current. The addition of one rectifier, Figure 8.1(b), provides a fixed half-cycle of power which shifts the power control range to half-power minimum and full-power maximum but with a strong DC component. The use of two SCR's, Figure 8.1(c), controls from zero to full-power and requires isolated gate signals, either as two control circuits or pulse-transformer coupling from a single control. Equal triggering angles of the two SCR's produce a symmetrical output wave with no DC component. Reversible half-wave DC output is obtained by controlling symmetry of triggering angle.

An alternate form of full-wave control is shown in Figure 8.1(d). This circuit has the advantage of a common cathode and gate connection for the two SCR's. While the two rectifiers prevent reverse voltage from appearing across the SCR's, they reduce circuit efficiency by their added power loss during conduction.

The most flexible circuit, Figure 8.1(e), uses one SCR inside a bridge rectifier and may be used for control of either AC or full-wave rectified DC. Losses in the rectifiers, however, make this the least efficient circuit form, and commutation is sometimes a problem (see Section 8.3). On the other hand, using one SCR on both halves of the AC wave is a more efficient utilization of SCR capacity, hence the choice of circuit form is based on economic factors as well as performance requirements.

8.2 ANALYSIS OF PHASE CONTROL

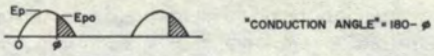
Rectifiers and SCR's are rated in terms of *average* current since this is easily found by a DC ammeter. Most AC loads are more concerned, however, with the *RMS*, or effective, current.

Figures 8.2 and 8.3 show the relationships of average, RMS, and peak voltages, as well as power in a resistive load. Since the SCR is a switch, it will apply this voltage to the load, but the value of current will depend on load impedance.

As an example of the use of these charts, suppose it is desired to operate a 1200 watt resistive load, rated at 120 volts, from a 240 volt supply. Connection of this load directly to the supply would result in 4800 watts, therefore the desired operation is at ¼ maximum power capability. We may use, for this case, either a half-wave or full-wave form of control circuit.

Starting with the half-wave case and Figure 8.2, the ¼ power point is a triggering phase angle of 90 degrees. Peak output voltage E_{PO} is equal to peak input voltage, 1.41×240 volts or 340 volts. Oddly enough, the RMS voltage is $.353 \times 340$ volts or 120 volts. Average voltage is $.159 \times 340$ volts or 54 volts, which would be indicated by a DC voltmeter across the load. Since the load resistance is 12 ohms ($120^2/1200$), peak current is $340/12 = 28.3$ amperes; RMS current is $120/12 = 10$ amperes; and average current is $54/12 = 4.5$ amperes, which would be indicated by a DC ammeter in series with the load. Power is $E_{RMS} \times I_{RMS}$ (since the load is pure resistance) which is 1200 watts. Note carefully that $E_{AVG} \times I_{AVG}$ is 243 but is *not* true power in the load. The SCR must be rated for 4.5 amperes (average) at a conduction angle ($180-\phi$) of 90 degrees. Furthermore, the load must be able to accept the high peak voltage and current, and the line "power-factor" is 0.5 (if defined as $P_{LOAD} \div E_{LINE} \times I_{LINE\text{-}RMS}$).

The other alternative is a symmetrical full-wave circuit, such as Figure 8.1(c), for which Figure 8.3 is used. The phase-angle of triggering is found to be 113 degrees for ¼ power. Peak voltage is $.92 \times 340 = 312$ volts, only a slight reduction from the half-wave case. RMS voltage is again $.353 \times 340 = 120$ volts. Average voltage is zero, presuming symmetrical wave form. RMS current is 10 amperes



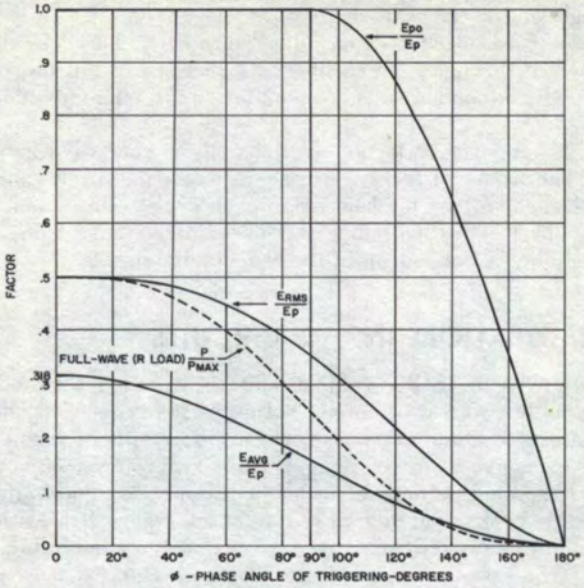
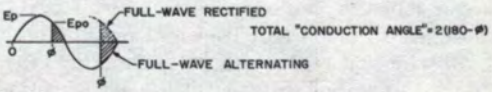


Figure 8.2 Half-Wave Phase Control Analysis Chart



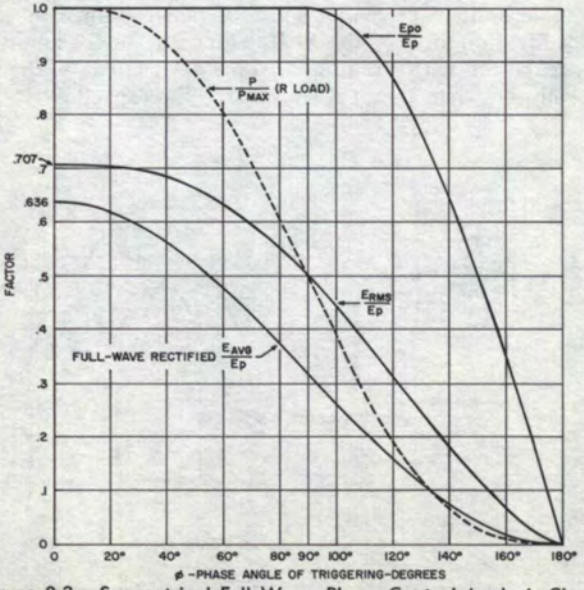


Figure 8.3 Symmetrical Full-Wave Phase Control Analysis Chart

and power is 1200 watts, but peak current has been reduced to 26 amperes. To determine rating required of the two SCR's, each can be considered as a single half-wave circuit. From Figure 8.2, the average voltage, at 113 degrees, is .097 × 340 = 33 volts. Average current in each SCR is then 33/12 = 2.75 amperes at a conduction angle of 180–113 = 67 degrees.

In the case of a bridged SCR circuit, Figure 8.1(e), used for this same load, the average current through each rectifier is 2.75 amperes but the average current through the SCR is 5.5 amperes, corresponding to a total conduction angle of 134 degrees.

Of particular importance to note in the analysis charts is the non-linearity of these curves. The first and last 30 degrees of each half-cycle contribute only 6 per cent (1.5% each) of the total power in each cycle. Consequently, a triggering range from 30° to 150° will produce a power-control range from 3% to 97% of full power, excluding voltage drop in the semiconductors.

8.3 COMMUTATION IN AC CIRCUITS

Commutation of the SCR in AC circuits is usually no problem because of the normal periodic reversal of supply voltage. There are cases, however, which can lead to failure to commutate properly as the result of insufficient time for turn-off, or of excessive dv/dt of reapplied forward voltage, or both. Supply frequency and voltage, and inductance in load or supply, are determining factors.

Consider the inverse-parallel SCR circuit of Figure 8.4, with an inductive load. At the time that current reaches zero so that the conducting SCR can commutate (point A), a certain supply voltage exists which must then appear as a forward bias across the other SCR. The rate-of-change of this voltage is dependent on inductance and capacitance in the load circuit, as well as reverse recovery time of the SCR. In certain cases, an L di/dt transient may be observed as the result of the SCR turning off when current drops below holding current, I_H. The addition of a series RC circuit in parallel with the SCR's, or with the load, can reduce the dv/dt to acceptable limits. The magnitude of C is determined by the load impedance and the dv/dt limitation of the SCR. The value of R should be such as to damp any LC oscillation, with a minimum value determined by the repetitive peak SCR current produced when the SCR's discharge the capacitor.

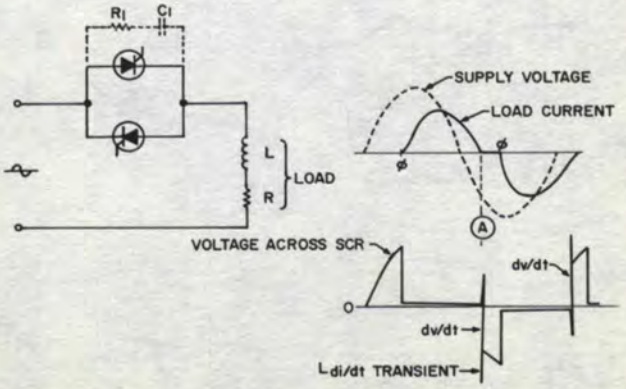


Figure 8.4 Suppression of dv/dt and Transients for Inductive Load

Inductive AC loads in the bridged SCR circuit of Figure 8.5 have a slightly different effect. The rapid reversal of voltage at the input terminals of the bridge rectifier not only represents a high dv/dt, but it also reduces the time available for commutation. If the rectifiers used in the bridge have slow reverse-recovery time, compared with turn-off time of the SCR, the reverse-recovery current is usually enough to provide adequate time for commutation. Where this is not practical, a series R_1C_1 circuit at the input terminals of the bridge may be used. An alternate form of suppression is to use R_2C_2 across the SCR, which will limit dv/dt, but a resistor R_3 is then required to provide a circulating current path (for current on the order of I_H) to allow sufficient commutating time. If capacitor C_2 is large, it can provide holding current to the SCR during the normal commutation period, and thus prevent turn-off until the capacitor is discharged.

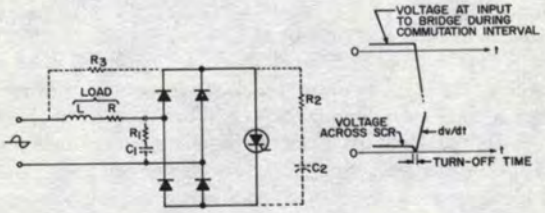


Figure 8.5 Suppression of dv/dt and Increasing Turn-Off Time

Inductive DC loads often require the addition of a free-wheeling diode, D_1 in Figure 8.6, to maintain current flow when the SCR is OFF. When an inductive DC load is used in the bridge circuit, Figure 8.6(c), the inductance causes a holding current to flow through the SCR and the bridge rectifier during the time line voltage goes through zero, preventing commutation. The addition of a free-wheeling diode, D_1, is required to by-pass this current around the SCR. The average current rating required for the diode D_1 is ¼ maximum average load current.

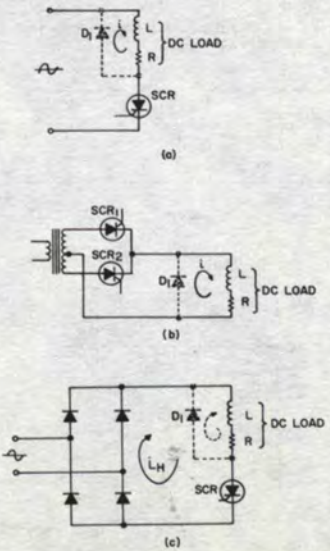


Figure 8.6 Free-Wheeling Diode By-Passes Holding Current

8.4 TRIGGER CIRCUITS FOR PHASE CONTROL

The trigger circuit for SCR phase control must convert information from the form of resistance, current, or voltage, into the time of occurrence of a signal capable of triggering the SCR. Since the trigger signal must be synchronized with the SCR supply, the power for the trigger generator may be obtained from either the supply voltage or from the voltage appearing across the SCR.

8.4.1 Manual Control

Figure 8.7 shows a conventional, manually-controlled SCR circuit with a DC load. A zener diode clamps the control circuit voltage to a fixed level, as shown in Figure 8.8. Since the peak-point (or triggering) voltage, e_p, of the unijunction transistor emitter is a fixed fraction of the interbase voltage, V_{BB}, as indicated by the dashed curve, the capacitor will charge on an exponential curve toward V_{BB} until its voltage reaches e_p. Assuming, for convenience, that e_p is 0.63 V_{BB}, triggering will occur at one time-constant. Therefore, to cover the range from 0.3 to 8.0 milliseconds, the product R_2C must change by the same amount. Since C is fixed, R_2 must then be varied over a 27:1 range. Not only is this a very large range, but the transfer characteristic from R_2 to average load voltage, V_L, is quite nonlinear, as shown in Figure 8.9. These characteristics are usually satisfactory, however, for manual control.

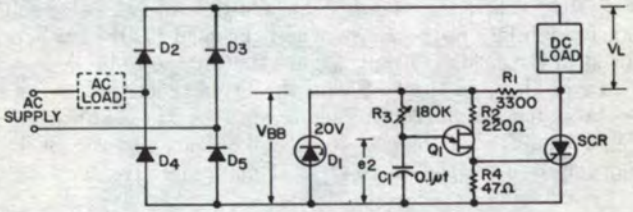


Figure 8.7 Conventional Phase-Control Circuit

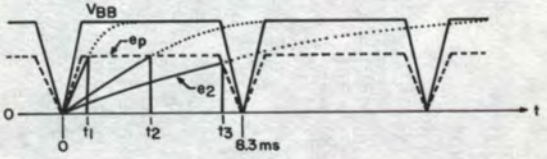


Figure 8.8 Unijunction Transistor Waveforms

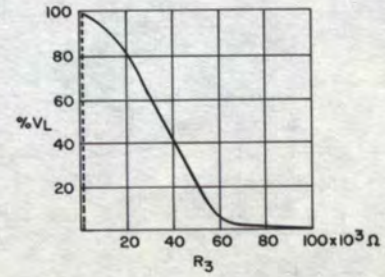


Figure 8.9 Transfer Characteristic of Conventional Circuit

Replacing the manually controlled resistor with a p-n-p transistor, shown in Figure 8.10(a), and applying a DC signal between emitter and base results in a higher current-gain but the range of base current must again be 27:1. The transfer characteristic, Figure 8.10(b), also remains non-linear.

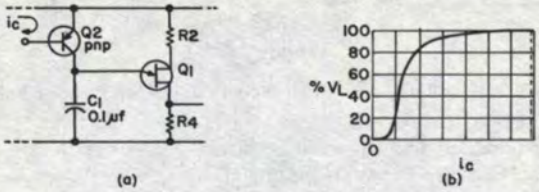


Figure 8.10 Series Transistor Controlled Ramp

Control gain can be made very high by the use of a low resistance potentiometer, connected as shown in Figure 8.11(a). Since the exponential charging of C is very fast, and limited by the voltage-division of the pot, the transfer characteristic is again non-linear, as shown in Figure 8.11(b). If the zener clamp has any significant zener impedance, the clamped voltage will not be flat, but will have a slight peak at 90 degrees. This curvature can produce an abrupt discontinuity, or "snap," in the transfer characteristic as indicated by the dashed curve of Figure 8.11(b).

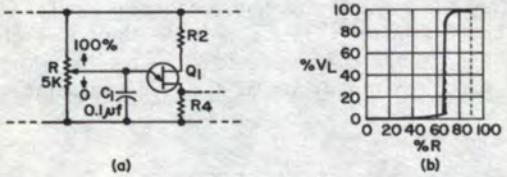


Figure 8.11 Resistance Controlled Pedestal

The use of an n-p-n transistor, Figure 8.12(a), will provide a high current-gain, but non-linearity and possible snap are still present, as indicated in Figure 8.12(b).

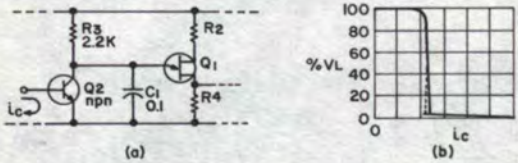


Figure 8.12 Shunt Transistor Controlled Pedestal

8.4.2 Ramp-and-Pedestal Control

If the circuits of Figures 8.7 and 8.11(a) are combined with diode coupling, as in Figure 8.13(a), the exponential ramp function can be caused to start from a higher voltage pedestal, as determined by the potentiometer. Transfer characteristic Curve 1 of Figure 8.13(b) is obtained when R_2 is set for a time-constant of 8 milliseconds. Higher control gain is obtained (Curve 2) by making the R_2C_1 time-constant about 25 milliseconds. The voltage wave-shape observed across C_1 is a nearly-linear ramp sitting on a variable-height pedestal, as in Figure 8.13(c).

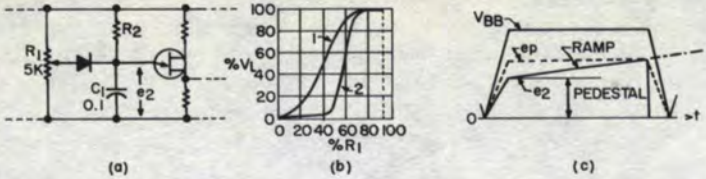


Figure 8.13 Resistance Controlled Pedestal with Linear Ramp

Small changes in pedestal height produce large changes in phase-angle of triggering. The linear relationship between height and phase-angle results, however, in a non-linear transfer function because of the shape of the sine-wave supply.

Both high gain and linearity are obtained by charging C_1 from the un-clamped sinusoidal waveform, as in Figure 8.14(a). This adds a cosine wave to the linear ramp to compensate for the sinusoidal supply waveform, resulting in the linear transfer characteristics shown in Figure 8.14(b). System gain can be adjusted over a wide range by changing the magnitude of charging resistor, R_2, as indicated in Figure 8.14(c). By selecting a ramp amplitude of one volt, for example, and assuming a zener diode of 20 volts, then a change in potentiometer setting of only 5 per cent results in the linear, full-range change in output.

The values shown in Figure 8.14(a) are typical for a 60 cps circuit. The potentiometer resistance must be low enough to charge capacitor C_1 rapidly, in order to be able to trigger early in the cycle. This is the limiting factor on control impedance level. The logarithmic characteristic of diodes limits the control gain that can be achieved with a reasonably linear transfer characteristic. At a one-volt

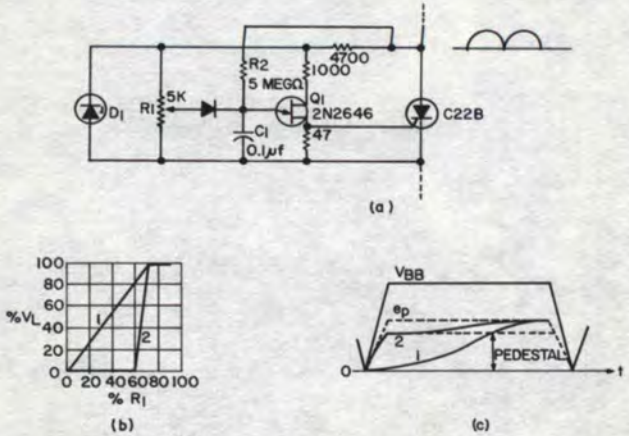


Figure 8.14 Resistance Controlled Pedestal with Cosine-Modified Ramp

ramp amplitude, diode non-linearity is not pronounced, but at 0.1 volt ramp voltage, the capacitor is charged primarily by diode current, thus obliterating the cosine-modified ramp. The sharper knee of a zener diode may be used to obtain higher gains, at the expense of requiring a higher voltage across the potentiometer. The third limiting factor is the peak-point current of the unijunction transistor. This current must be supplied entirely by R_2 and should be no higher than one-tenth the charging current on C_1, at the end of the half-cycle, in order to avoid

distortion of the waveform. The 2N2647 unijunction transistor used in the example has a maximum peak-point current of two microamperes, hence is particularly well suited for high-gain systems. The fourth limitation is the zener impedance of diode D_1. This impedance must be very low in order to keep the peak-point voltage (triggering level) constant during the half-cycle. If this voltage changes 0.1 volt, then the ramp voltage should be on the order of 1 volt. Temperature effects on the unijunction transistor, and other components, must also be taken into consideration when attempting to work at very low ramp voltages.

In Figure 8.15(a), manual control is replaced by a bridge circuit for feedback control. Zener diode D_2 has a slightly lower zener-voltage than D_1 in order to hold the top of the clamped waveform more nearly flat. Resistors R_1 and R_2 form the voltage divider which determines pedestal height. Variation in either of these resistors can therefore provide the control function, although R_2 is generally used as the variable. Figures 8.15(b) and (c) show the use of a thermistor for temperature regulation and a photoconductor for light control, in either open-loop or closed-loop systems.

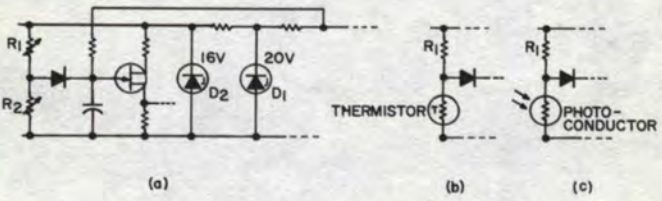


Figure 8.15 Ohmic-Transducer Pedestal Control

To obtain a higher input impedance, an n-p-n transistor may be used as an emitter-follower, as shown in Figure 8.16(a). If the transistor has a current gain of 100, the values of R_1 and R_2 can be increased from 3000 ohms to 300 K ohms, thus greatly reducing power dissipation in the sensing element. This is particularly important when R_1 or R_2 is a thermistor. Resistor R_3 is required in the collector circuit of the transistor in order to limit charging current available to the UJT capacitor and thus prevent premature triggering of the UJT.

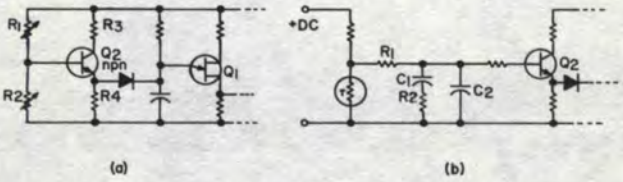


Figure 8.16 Transistor Emitter-Follower Control for AC or DC Input

In many feedback-control systems, high gain and phase-shifts often produce instability, ranging from excessive overshoot to large oscillations, or hunting. The transistor permits use of a DC sensing circuit followed by an appropriate RC "notch-network" (R_1 C_1, R_2 C_2) to produce the required degree of damping. Since the cosine-modified ramp results in a uniform, linear response, system gain is constant and proper damping is much easier to obtain than in the case of the linear ramp where gain changes with phase-angle. System gain is controlled by the ramp charging resistor (R_2 of Figure 8.14), which can be made a secondary

variable through the use of a thermistor or a photoconductor. To avoid excessive loading on the DC sensing circuit, a resistor is required in series with the base of the transistor. Upper and lower control limits may be obtained by the use of diode clamps.

The capability of working from a DC control signal permits a soft-start and soft-stop circuit, shown in Figure 8.17(a). This circuit features individually adjustable rates of start and stop, good linearity, upper and lower limit clamps, and manual or resistive master phase control by means of the top clamping level. For a typical UJT peak-point of 2/3 the interbase voltage, the ramp amplitude may be set at 1/3 interbase voltage and the pedestal clamped at 1/3 and 2/3 this voltage. The resulting performance characteristic is shown in Figure 8.17(b) and (c) for this condition, with the switch turned ON at t_1 and OFF at t_3.

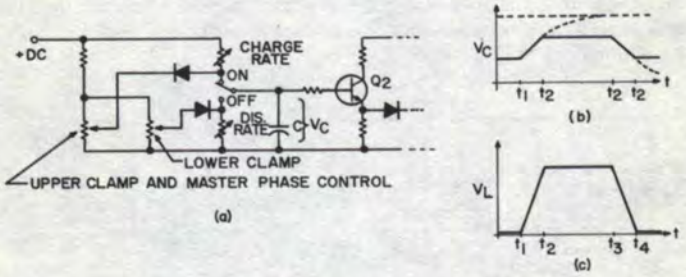


Figure 8.17 Soft Start and Stop Control

Remote control from an AC signal, such as an audio-frequency from a tape recorder or from a tachometer, or an RF carrier alone or with audio modulation, is shown in Figure 8.18. The offset voltage characteristic of a high-gain system provides immunity to noise and effectively decreases the band-width of the input resonant circuit. If offset is not desired, but high-gain is required, the input circuit may be biased, by the dotted resistors R_4 and R_5, to a voltage just below offset. The use of a standard ratio-detector will permit control by an FM signal directly.

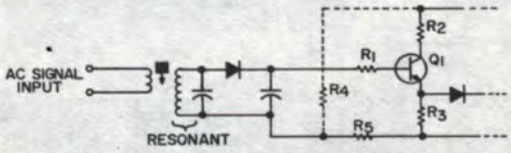


Figure 8.18 Frequency-Selective AC Amplitude Control Circuit

Alternate transistor connections are shown in Figure 8.19, providing a wide variety of performance characteristics. The emitter-follower circuit is simplified in Figure 8.19(a) for low-gain use. At high control gain (low ramp voltage) the emitter current requirement is very low, and the decrease in beta at such low currents causes excessive non-linearity. Standard common-emitter connections for n-p-n and p-n-p transistors, Figures 8.19(b) and (c), provide lower input impedance and higher voltage gain, but require temperature compensation in high-gain applications. In addition, the n-p-n circuit of Figure 8.19(b) results in a sense inversion which may or may not be desirable. Sense inversion is also obtained in the p-n-p emitter-follower of Figure 8.19(d). The excellent performance characteristics and

low cost of the 2N2923 silicon n-p-n transistor, however, make the choice of the n-p-n emitter-follower circuit attractive, particularly since temperature changes have very little effect on operation of this circuit.

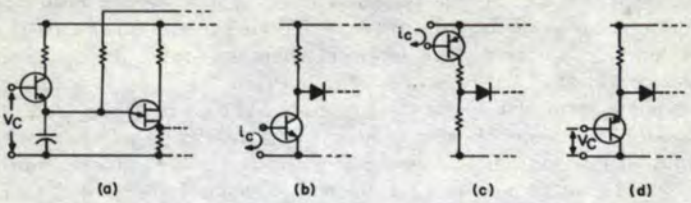


Figure 8.19 Alternate Transistor Pedestal Control Circuits

Snap-action switching of the load in response to change in a DC signal, AC signal, or variable resistance element is readily obtained by removing the ramp completely, with a slight ramp inversion. The circuit of Figure 8.20 produces such a snap action by a small differentiating network, $R_1R_2C_1$, that peaks the leading edge of the pedestal. Triggering can only occur near the beginning of each half-cycle. If the source of power for this control circuit is derived from the voltage across the SCR, the capacitor C_1 will discharge during the conduction period of the SCR, and on the next succeeding half-cycle it will produce a higher peaking voltage on C_3. This results in a differential in the controlling DC voltage required to snap ON and to snap OFF. Snap action is also obtained by taking control power from a fixed source, but there is little differential. For certain heater-type loads, this latter type of snap action is preferable.

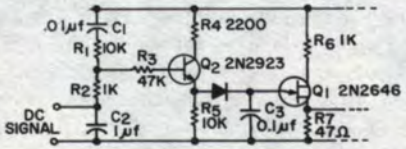


Figure 8.20 Snap-Action Control Circuit

Figure 8.21 illustrates one of the many possible variations of the snap-action circuit. In this circuit, C_4, C_2 and R_8, and R_7 provide the inverted ramp waveform at a high impedance level. Capacitor C_3 has been added to prevent transients from triggering the UJT, Q_1, by coupling the transient from base 2 to the emitter. The value of C_3 should be roughly equal to C_4. Since C_4 will generally be too small to provide positive triggering of an SCR, a second discharge capacitor, C_1 is provided to supply the additional energy. C_1 is charged by the divider R_5, R_6 to a voltage less than the emitter peak-point such as not to interfere with the normal ramp function. It may be desirable to add another capacitor, equal to C_1, in parallel to R_5 for transient voltage immunity.

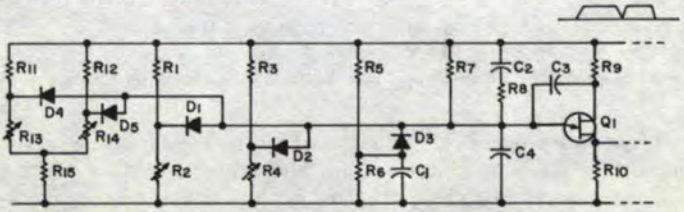


Figure 8.21 Multiple-Input, High Impedance Snap Action Circuit

Multiple input control of this circuit is obtained by using diodes to clamp the voltage on C_4 to whichever voltage divider has the lowest voltage. Thus, reducing either R_2, R_4, R_{13} or R_{14} will prevent triggering of Q_1. Coupling R_{13} and R_{14} together through R_{15} provides the unique function that, with R_{13} fixed, either raising or lowering the resistance of R_{14} will prevent triggering of the UJT. This is useful in thermistor temperature protective circuits where sensing both open-circuit and short-circuit conditions of the thermistor is desired.

An alternate form of the soft-start circuit is shown in Figure 8.22, using the clamping diode, D_1, to control pedestal height on a linear ramp. Capacitor C_1 may be several hundred microfarads and is charged slowly through R_2. R_1 continues the charging beyond emitter peak-point voltage to completely remove the effect of C_1 and to provide a discharge path when power is removed. The supply for this circuit must be obtained from the line, rather than from voltage across the controlled rectifier, in order to completely charge C_1.

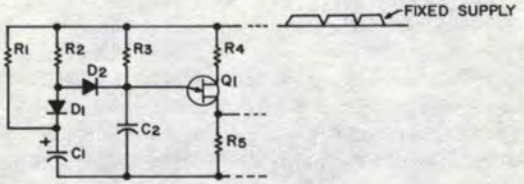
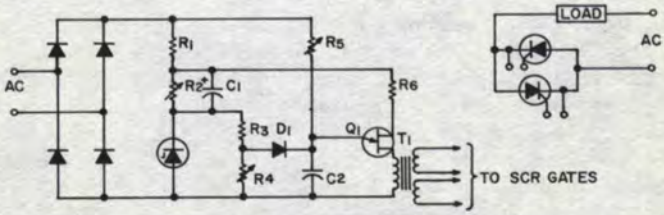


Figure 8.22 Alternate Soft-Start Circuit

In Figure 8.23, compensation for changes in supply voltage is obtained by R_2 and C_1 which add to the zener diode voltage a DC voltage proportional to supply voltage. This is used to supply interbase voltage for the UJT. Since pedestal height is fixed by the zener diode, reducing supply voltage reduces interbase and peak-point voltages of the UJT, thus causing triggering to occur earlier on the ramp. The size of R_2 is dependent on ramp amplitude, hence upon R_5. The voltage compensation feature does not interfere with use of the pedestal height in any other control form, such as a feedback control system. This system has been found capable of holding RMS output voltage constant within 5% for a 50% change in supply voltage. The bottom end of control is reached when supply voltage drops to desired output voltage.



R_1 : 5000Ω R_3: 3300 R_5 : 5M C_1 : 200μf, 10v Q_1 : 2N2647
R_2: 500Ω R_4: 10K R_6 : 1K C_2 : 0.1μf

Figure 8.23 Wide Range Line-Voltage Compensation Control

Current feedback control can be obtained by the use of voltage across a shunt resistor, but this requires rectification and filtering when AC is to be controlled since no current flows prior to SCR triggering. In addition, a lamp may be used as the shunt, with a photoconductor sensing lamp output. Response time of the lamp

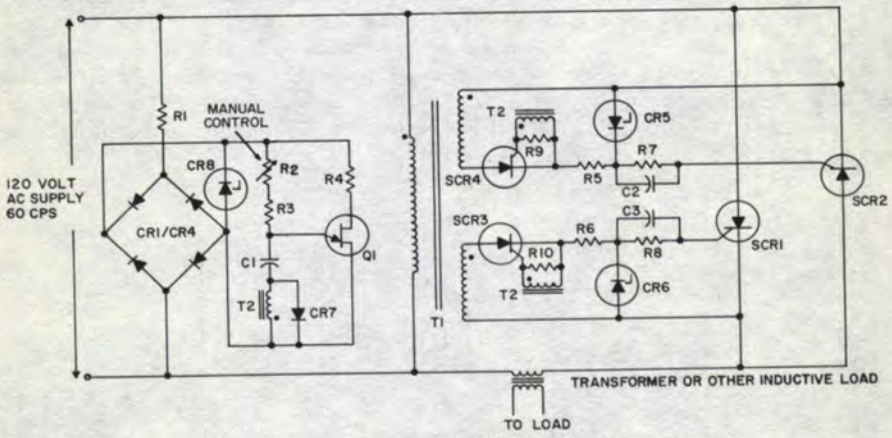
and photoconductor is generally long enough to provide filtering, and the control is on the *square* of current, hence will hold constant RMS value rather than average value. A resistor-thermistor combination will also provide RMS control. A current-transformer may be used to produce a higher output voltage signal on AC with less power loss. If power loss in the shunt is detrimental, a magnetic-flux sensitive element such as the Mistor* resistance transducer or a Hall-effect element may be used in a suitable coil and core. In these magnetic-flux sensors, the output will be a function of average current.

These circuits are typical of a wide variety, based on the ramp-and-pedestal concept for transfer from voltage, current, or impedance level to phase-angle of triggering for SCR's. Adjustable gain, linearity, selection of high or low input impedance, and operation from a DC input signal are attractive features for use in feedback or open-loop control systems, or in special function systems.

8.5 TRIGGER CIRCUIT FOR INDUCTIVE AC LOADS

Inductive AC loads present two basic requirements of the trigger circuits in order to provide symmetry and proper control: a) synchronization must be obtained from the supply voltage rather than SCR voltage; b) the trigger signal must be continuous during most of the desired conduction period. Figure 8.24 shows a trigger circuit specifically designed to meet these requirements.

Unijunction transistor Q_1 is connected across the AC supply line by means of the bridge rectifier, CR_1 through CR_4, thus permitting Q_1 to trigger on both halves of the AC cycle.



R1 - 3.3K, 5 WATT
R2 - 250K, 2 WATT
R3 - 3.3K, 1 WATT
R4 - 330, 1/2 WATT
R5, R6 - 22Ω, 2 WATT
R7, R8 - 33Ω, 2 WATT
R9, R10 - 47Ω, 1/2 WATT
C1, C2, C3 - 0.1 MFD
Q1 - GE 2N2646
SCR1, SCR2 — CONTROLLED RECTIFIERS, AS REQUIRED
SCR3, SCR4 - GE 2N1595

CR1 TO CR4 - GE IN1693
CR5, CR6 - GE IN1765
CR7 - GE IN1692
CR8 - GE IN1776
T1 - ISOLATION TRANSFORMER 120/12.6/12.6 VAC; PRIMARY VOLTAGE DEPENDS ON LINE VOLTAGE (UTC FT-10 FOR 120V.)
T2 - PULSE TRANSFORMER PE 2229, UTC H51 OR SPRAGUE 93Z20 EQUIVALENT

Figure 8.24 Trigger Circuit for Phase Controlled SCR's Feeding Inductive Load

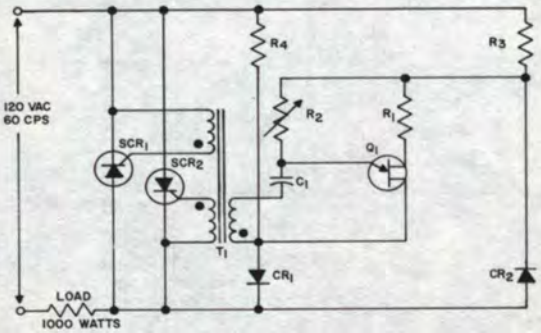
* TM American Aerospace Controls, Inc.

The time constant of potentiometer R_2 in conjunction with capacitor C_1 determines the delay angle α at which the unijunction transistor delivers its first pulse to the primary of pulse transformer T_2 during each half-cycle. These pulses are coupled directly to the gates of SCR_3 and SCR_4. Whichever of these SCR's has positive anode voltage during that specific half-cycle triggers and delivers voltage to its respective main SCR, firing it in turn. The low voltage AC supply for the "pilot" SCR's (SCR_3 and SCR_4) is derived from a "filament" type transformer T_1. Zener diodes CR_5 and CR_6, in conjunction with resistors R_5 and R_6, clip the AC gate voltage to prevent excessive power dissipation in the gates of the main SCR's. The RC networks (R_7—C_2 and R_8—C_3) also limit gate dissipation in the main SCR's while delivering a momentarily higher gate pulse at the beginning of the conduction period to accelerate the switching action in the main SCR's.

If electrical isolation of a DC control signal from the AC voltage is required, the entire unijunction trigger circuit with its bridge rectifier and associated components can be connected to an additional secondary winding (approximately 110 volts) on transformer T_1. Total loading of this particular part of the circuit is less than 30 milliamperes. Of course, low level phase control signals for SCR_3 and SCR_4 can be secured from other circuits than the specific one shown, but this is incidental to the main objectives: driving SCR_1 and SCR_2 from a square wave source synchronized to the AC line.

8.6 1 KW GENERAL PURPOSE AC PHASE CONTROL

The inverse-parallel circuit of Figure 8.25 is an economical unit designed for general use, such as manual control of lights, heaters, ovens, fans or blowers. The use of two dropping resistors, R_3 and R_4, permits use of the low-voltage selenium diodes with a significant reduction in cost. Further reduction in cost may be obtained by fabricating the pulse transformer from three windings of 60 turns, AWG 30 wire, placed side-by-side on a 1" by ¼" diameter ferrite "antenna" core, well insulated of course. The UJT drives the center winding and the outer two windings are connected to the SCR's.



R_1	1000 OHMS
R_2	250,000 OHM LINEAR POT, 3300 OHM MIN
R_3, R_4	33,000 OHM, 1 WATT
C_1	0.1 MFD
SCR_1, SCR_2	G-E C22B
CR_1, CR_2	G-E 6RS5GDIBADI
CR_5	1N1776 ZENER DIODE, ONE WATT, 22 VOLTS
Q_1	G-E 2N2646
T_1	PE 223I, UTC H5I, SPRAGUE 93Z20 OR EQUIVALENT

Figure 8.25 One Kilowatt General Purpose AC Phase Control

This circuit may be modified for a ramp-and-pedestal control system by reducing R_3 and R_4 to 4700 ohms each and either adding one zener diode across R_1 and Q_1, or replacing CR_1 and CR_2 by zener diodes.

8.7 NEON LAMP TRIGGER CIRCUITS

Neon lamp SCR phase-controlled trigger circuits have the promise of combining the low cost of the RC diode circuit with improved performance. In addition, the possibility exists in such a relatively simple yet high impedance circuit to exercise control over the charging rate of the trigger capacitor with suitable devices responsive to light, heat, pressure, etc.

Figure 8.26 shows a half wave AC phase-controlled circuit using an NE-83 as the trigger for a two terminal system. The NE-83 will trigger when the voltage across the two 0.1 MFD capacitors reaches the breakdown voltage of the lamp. Control can be obtained full off to 95% of the half wave RMS output voltage. Full power can be obtained with the addition of the switch across the SCR.

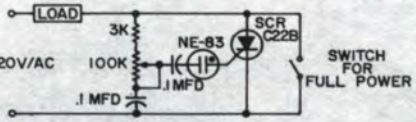


Figure 8.26 Half Wave/Two Terminal

Figure 8.27 is a transformer coupled full-wave AC phase-controlled circuit using an NE-83 as the trigger for a two terminal system. The NE-83 will perform the same as in the half-wave circuit but the pulse transformer will allow the SCR's to alternate in firing. The resistor R and the pulse transformer should be chosen to give proper shape of the pulse to the gate of the SCR. Some loss of load voltage will occur but will amount to only about 5% in terms of total RMS output voltage.

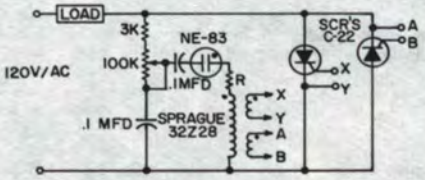


Figure 8.27 Full Wave Transformer Coupled/Two Terminal

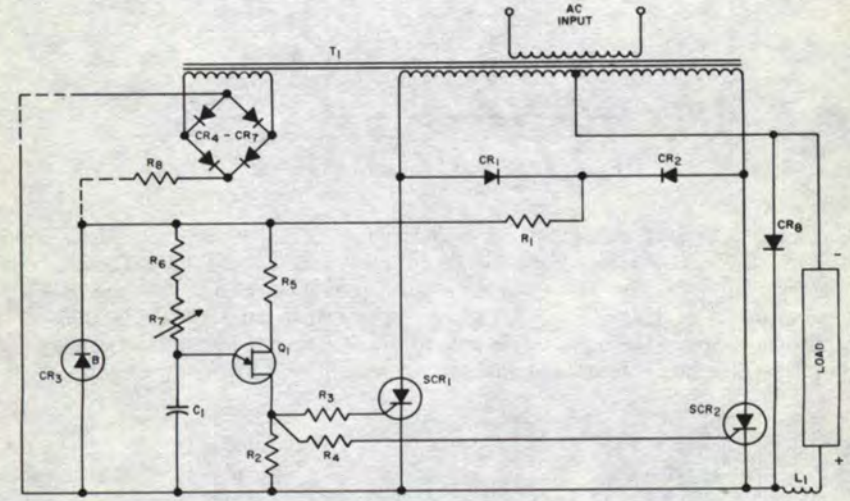
8.8 TYPICAL PHASE-CONTROLLED CIRCUITS FOR DC LOADS

As mentioned earlier, diode rectifiers can be replaced by SCR's in conventional rectifier circuits giving continuous control over a DC load from an AC source. The following examples in the power supply and motor drive area illustrate this.

8.8.1 Phase-Controlled DC Supplies

Figure 8.28 illustrates the use of SCR's in a typical single phase centertap phase-controlled rectifier. By varying R_7, the DC voltage across the load can be steplessly adjusted from its maximum value down to zero. As in the AC phase-controlled switch, a single UJT (Q_1) is used to develop a gate signal to fire both SCR's on alternate half-cycles. Whichever of the two SCR's has positive anode voltage at the time the gate pulse occurs will fire, thus applying voltage to the load for the remainder of that half-cycle. The firing angle can be adjusted by means of R_7. At 60 cps, the firing angle of this circuit can be varied from approximately 10° to 180° (fully off).

If the secondary voltage applied to the SCR anodes is less than approximately 100 volts RMS, a separate voltage supply should be used for the UJT control. In Figure 8.28 an additional 117 VAC winding on T_1 in conjunction with a diode bridge CR_4—CR_7 can be substituted for CR_1, CR_2, and R_1 if the main secondary voltage is low. A more steeply rising square wave of voltage with sufficient amplitude is thereby provided for control purposes. If the load requires filtering, inductance L_1 and free-wheeling diode CR_8 may be added, as shown.



R_1 —— 3.3K, 5 WATT IF SEC. VOLTAGE OF T_1 IS 117 VOLTS EACH SIDE OF CENTERTAP
R_2 —— 47 Ω, ½ WATT
R_3, R_4 — 22 Ω, ½ WATT
R_5 —— 390 Ω, ½ WATT
R_6 —— 2.7K, ½ WATT
R_7 —— 50K LINEAR POT
R_8 —— 3.3K, 5 WATT
C_1 —— 0.2 MFD
SCR_1, SCR_2 — AS REQUIRED BY LOAD
CR_1, CR_2, CR_4, CR_7 — G-E IN1695
CR_3 —— IN1776 REGULATING DIODE
Q_1 —— G-E 2N2646
OPTIONAL CR_8 — AS REQUIRED BY LOAD CURRENT
L_1 — AS REQUIRED FOR FILTERING

Figure 8.28 Phase-Controlled DC Power Supply

8.8.2 Full Wave DC Motor Drives

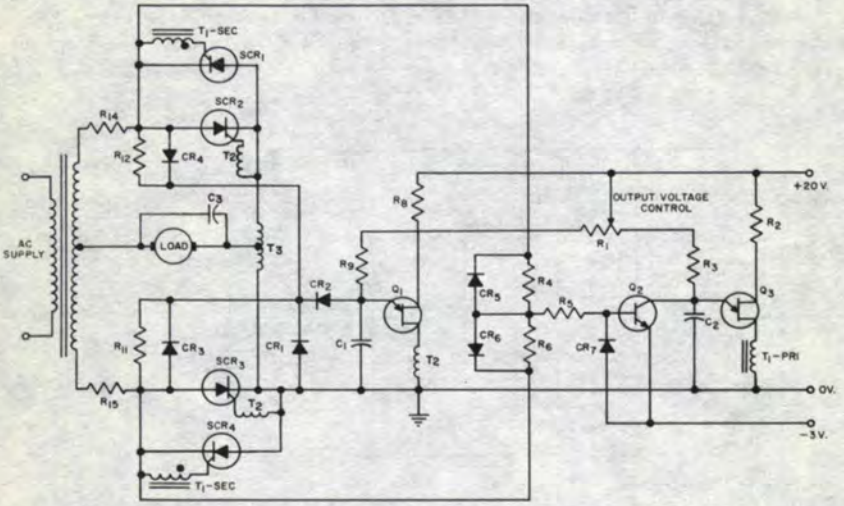
SCR's are well suited for supplying both armature power and field excitation to DC machines.

A full wave reversing control or servo as shown in Figure 8.29 can be designed around two SCR's with common cathode (SCR_2, SCR_3) and two SCR's with common anodes (SCR_1, SCR_4). In this circuit SCR_2 and SCR_3 are controlled by UJT Q_1 and

the other pair, SCR_1 and SCR_4, are controlled by UJT Q_3. Transistor clamp Q_2 synchronizes the firing of Q_3 to the anode voltages across SCR_1 and SCR_4.

Potentiometer R_1 can be used to regulate the polarity and the magnitude of output voltage across the load. With R_1 at its center position, neither UJT fires and no output voltage appears across the load. As the arm of R_1 is moved to the left, Q_1 and its associated SCR's begin to fire. At the extreme left-hand position of R_1, full output voltage appears across the load. As the arm of R_1 is moved to the right of center, similar action occurs except the polarity across the load is reversed.

If the load is a DC motor, plugging action occurs if R_1 is reversed abruptly. R_{14} and R_{15} are used in series with each end of the transformer to limit fault current in the event a voltage transient should fire an odd- or even-numbered SCR pair simultaneously. Commutating reactor T_3 and capacitor C_3 limit the dv/dt which one pair of SCR's can impress upon the opposite pair.



R_1 — 100K LINEAR POT
R_2, R_8 — 470 OHMS, 1/2 WATT
R_3, R_9 — 2700 OHMS, 1/2 WATT
R_4, R_6 — 10K, 2 WATTS
R_5 — 4700 OHMS, 1/2 WATT

R_{11}, R_{12} — 2200 OHMS, 2 WATTS
R_{14}, R_{15} — 2 OHMS, 500 WATTS OR LESS, DEPENDING ON RATING OF LOAD
C_1, C_2 — 0.2 MFD
$SCR_1, SCR_2, SCR_3, SCR_4$ — G-E SCR (VOLTAGE RATING DEPENDENT ON SECONDARY TRANSFORMER VOLTAGE)

$CR_1, CR_2, CR_3, CR_4, CR_5, CR_6$ — G-E IN1695
CR_7 — G-E IN1692
Q_1, Q_3 — G-E 2N1671A
Q_2 — G-E 2N335
T_1, T_2 — PE2231, UTC H51, OR EQUIVALENT
T_3, C_3 } AS REQUIRED BY LOAD

Figure 8.29 Full Wave Reversing Drive

8.8.3 Half Wave DC Motor Drives

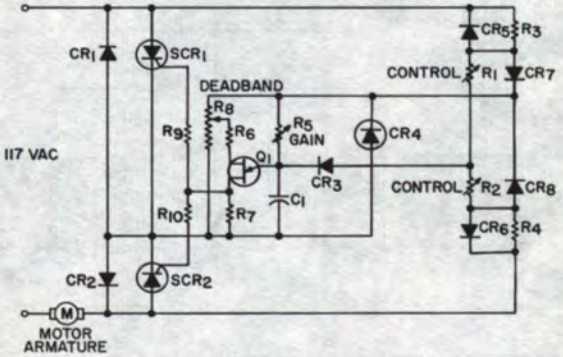
For adjustable speed operation of lower rated motors half-wave control has great economic advantages at quite adequate performance levels in many cases. The machines may have shunt fields, series fields (universal motors), or be of the permanent magnet type.

The drive discussed in connection with Figure 8.29 is illustrative of permanent magnet motors or separately excited shunt motors. However, one SCR is normally all that is required in the armature circuit for one direction of rotation. This feature is illustrated more fully in the universal motor speed control circuit shown in Figure 8.31.

8.8.3.1 Balanced-Bridge Reversing Servo Drive

A phase-sensitive servo drive supplying reversible half wave power to the armature of a small permanent magnet or shunt motor is shown in Figure 8.30. The power circuit consists of two half-wave circuits back-to-back (SCR_1, CR_1; and SCR_2, CR_2) fired by unijunction transistor, Q_1, on either the positive or negative half-cycle of line voltage depending on the direction of unbalance of the reference bridge resulting from the value of the sensing element R_1. R_1 can be a photo-resistor, a thermistor, a potentiometer, or an output from a control amplifier.

The potentiometer R_8 is set so that the DC bias on the emitter of unijunction transistor, Q_1, is slightly below the peak-point voltage at which Q_1 fires, by an amount dependent upon the deadband desired. With R_1 equal to R_2 the bridge will be balanced, UJT (Q_1) will not fire and no output voltage appears across the load. If R_1 is increased thus unbalancing the bridge, an AC signal will appear at the emitter of the UJT causing the emitter to be biased above the firing voltage during one half-cycle of the AC. Q_1 will fire and, since SCR_2 is forward biased, SCR_2 will fire. When R_1 is decreased, similar action occurs except that SCR_1 will fire, reversing the polarity across the load.



CR1, CR2, SCR1, SCR2 : AS REQUIRED BY LOAD

R1 : 3.3K } SEE NOTE	R6: 1K	C1 : 0.1μf
R2: 3.3K } SEE NOTE	R7: 47Ω	Q1 : 2N2646
R3: 3.3K, 2W	R8: 2500Ω	CR4: IN1776
R4: 3.3K, 2W	R9: 47Ω	CR5-8: IN1695
R5: 2 MEGOHMS	R10: 47Ω	CR3: IN1692

NOTE:
EITHER R1 OR R2 MAY BE A VARIABLE RESISTANCE TRANSDUCER, SUCH AS THE GE-B425B PHOTOCONDUCTOR, OR THE GE-ID301 THERMISTOR, OR A POSITION SENSING POTENTIOMETER.

Figure 8.30 Balanced-Bridge Reversing Servo Drive for Shunt-Wound Motor

8.8.3.2 Universal Motor Adjustable Speed Drive

The universal motor has found wide use in many applications which require high torque during starting and at low speeds. When used in a half-wave circuit, the series or universal motor has an added advantage over the shunt motor since its output torque is approximately proportional to the square of the RMS value of armature current rather than the first power of the average value as is the case with the fixed field shunt motor.

Speed control is achieved by varying the conduction angle of the SCR placed in series with the armature and field of the universal (AC-DC) motor. When conduction is initiated at a point determined by the motor speed, a regulated speed control results. Two methods of achieving this type of operation rely either on the residual field induced voltage of the motor for a speed signal, or on excitation of the series field during the "off" half-cycle for developing a similar speed sensitive signal.

The circuit of Figure 8.31(a) shows a speed control which makes use of the motor residual field to induce a counter emf in the armature proportional to speed. This voltage is employed as the speed feedback signal. This circuit is suggested particularly for applications requiring stable operation at low speeds.

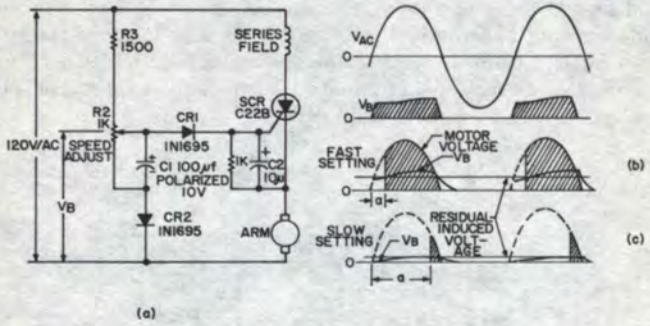


Figure 8.31 Universal Motor Adjustable Speed Drive

During the negative half-cycle of the supply voltage capacitor C_1, which may be of the polarized electrolytic type, is partially discharged through R_2. During the positive half-cycle C_1 charges from R_3 and the AC line with a sinusoidal current which produces a cosine voltage wave on C_1. If the motor armature is standing still, no voltage is induced in it by the residual field, and gate current to the SCR flows as soon as V_B exceeds the forward voltage drop of CR_1 and the gate drop of SCR. This will fire SCR early in the cycle, providing ample energy to accelerate the motor. As the motor approaches its preset speed, the residual induced voltage in the armature builds up. This voltage is positive on the top terminal of the armature and bucks the flow of gate current from capacitor C_1 until V_B exceeds the armature voltage. This higher voltage requirement on C_1 retards the firing angle and allows the motor to cease accelerating.

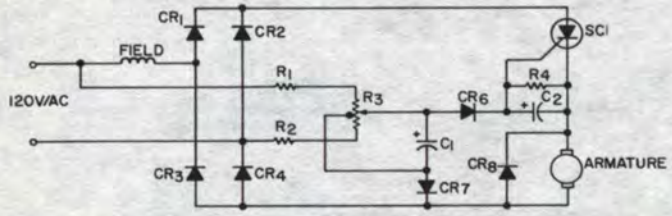
Once the motor has reached operating speed, the residual induced voltage provides automatic speed regulating action. For instance, if a heavy load starts to pull down the motor speed, the induced voltage decreases, and SCR therefore fires earlier in the cycle. The additional energy thus furnished to the motor supplies the necessary torque to handle the increased load. Conversely, a light load with its tendency to increase speed raises the motor residual induced voltage, retarding the firing angle and reducing voltage on the motor.

R_2 adjusts the desired speed by controlling the charging rate of capacitor C_1. The waveform of voltage, V_B on capacitor C_1 is shown in Figures 8.31(b) and 8.31(c). When R_2 is adjusted to a high value, V_B builds up higher and fires SCR early in the cycle. This high speed setting is depicted by the V_B waveform in Figure 8.31(b). When R_2 is set to a small value, V_B builds up slowly so that firing occurs late in the cycle as in Figure 8.31(c) and the motor speed is therefore low.

Not all types and makes of motors perform satisfactorily in the circuit of Figure 8.31 because of the varying degree of their residual induced voltage. Motors with low hysteresis iron tend to have a low residual induced voltage and therefore do not have ample feedback voltage for satisfactory operation of the circuit. Reference 5 discusses the motor characteristic requirements of this and other universal motor speed controls.

A reversing speed-control circuit, shown in Figure 8.32, operates in essentially the same manner. Direction of rotation depends on which half-cycle the SCR conducts, since the series field is in the AC leg of the bridge rectifier.

While the performance achieved by this circuit is entirely adequate for a majority of universal motor drive applications, a higher degree of speed regulation can be achieved by more sophisticated types of feedback and firing circuitry. Feedback gain and pulsed types of gate signals such as developed by unijunction transistors provide improved regulation and stability over wide speed ranges with little or no need for special calibrating adjustments for individual SCR characteristics. These more complex circuits also eliminate the effects of temperature on the SCR firing characteristics and therefore on the speed regulation also.



R_1 : 1500	C_1 : 200 µf	SCR : C20B
R_2 : 1500	C_2 : 5 µf	CR_8 : A40B
R_3 : 3000 CT	CR_{1-4} : A40B	MOTOR : SERIES, REVERSIBLE
R_4 : 1000	CR_{6-7} : IN1694	

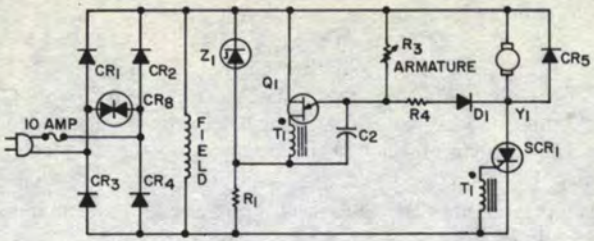
Figure 8.32 Reversible Half-Wave Speed Control for Series-Wound Motors

8.8.3.3 Full-Wave Speed-Regulator For Shunt Wound DC Motors

The circuit of Figure 8.33 features closed-loop feedback armature control to closely regulate the speed of a DC motor over a wide range. Loop gain is achieved by using the motor back EMF and inductive characteristics to control the inherently high-gain SCR. In the simplest case, regulation extends over about a 6:1 speed range. With a modest number of additional parts, this may be extended to a 20:1 range.

The circuit is simple, reliable, inexpensive and compact. When the motor is placed in this circuit, its speed becomes insensitive to line voltage, as well as torque, variations. The circuit operates equally well as a half-wave regulator. Minor modifications will provide soft-start and current limiting features.

Avalanche diode Z_1 supplies power to the firing circuit and, additionally, serves as a reference diode. When the circuit is first switched on, C_2 charges through R_3, and Q_1 fires when the voltage across C_2 reaches the avalanche voltage of Z_1 multiplied by the intrinsic standoff ratio of unijunction transistor Q_1. Diode D_1 prevents charging current from coming through the armature and R_4. The pulse from Q_1 is fed to SCR_1 via T_1, the return path being the supply and Z_1. When SCR_1 fires, voltage is applied to the armature, causing it to start to turn. After the armature has begun to rotate, the voltage across it will look like that in Figure 8.34.



R_1 – 4.7K, 10%
R_3 – 100K VARIABLE-SPEED CONTROL
R_4 – 100K, 1/2W, 10%
C_2 – 0.5μf, 50V
D_1 – G.E. IN536
Z_1 – 25V ZENER DIODE, 1W
T_1 – PULSE TRANSFORMER, SPRAGUE 93Z20 OR EQUIVALENT

CR_1–CR_5 GE A40B
SCR_1–GE C35B
Q_1 – GE 2N2646
CR_8–GE 6RS2ISA5D5
THYRECTOR (OPTIONAL–TRANSIENT PROTECTION)

Figure 8.33 Basic Control Circuit for ½ HP DC Motor

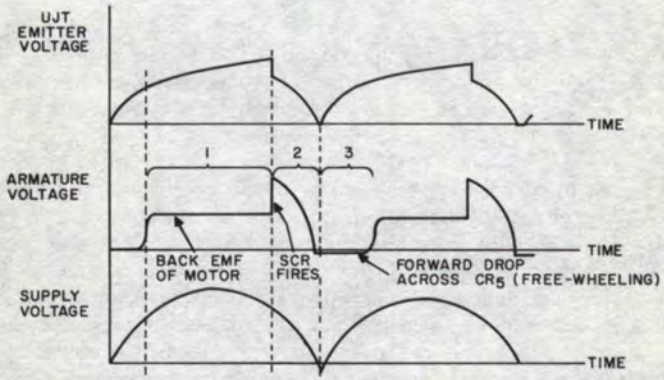


Figure 8.34 Circuit Voltages

The back EMF of the armature is shown as region 1 in Figure 8.34. When the SCR fires (region 2) a pulse of line voltage is applied to the armature. When the line voltage goes through zero, the SCR commutates, and the current flowing through the inductance of the armature "free-wheels," or, as it may also be termed, decays, through CR_5. This period when the current is decaying is shown as region 3. During this interval, the positive supply is actually slightly negative (by the value of the forward drop of CR_5) with respect to the anode of the SCR. This fact insures that D_1 will be blocking during this period. With D_1 blocking, C_2 charges at its maximum possible rate. When period 1 begins again, the armature voltage polarity reverses, forward-biasing D_1 and allowing charging current to be shunted from the capacitor via R_4. The amount of current shunted away from C_2 is determined by the back EMF of the motor and the value of R_4.

Next consider the result of applying torque to the motor. The motor does two things. (1) It attempts to slow down, and (2) it begins to draw more current. This latter effect widens region 3 in Figure 8.34, because there is now more current to decay through CR_5. The first effect, slowing down, reduces the motor back EMF.

Widening region 3 allows maximum possible charging current to flow into C_2 for a longer period of time. Reducing the back EMF (region 1) reduces the amount of charging current which is shunted through R_4 during region 1. Both of these effects allow C_2 to be charged faster, thereby widening region 2, which is the voltage pulse applied to the armature by the SCR firing. C_2 discharges through R_4 during region 2, when the cathode of diode D_1 is connected to the negative supply by the conducting SCR_1.

Thus we see that we have mechanisms for correcting both for speed and torque changes on the motor.

Different motors will, of course, have different armature characteristics. Corrections may easily be made to accommodate these differences by altering the values of R_3 and R_4.

Similarly, speed ranges for which regulation occurs may be widened or changed by altering R_3 and R_4. It should be noted that although the control *regulates* speed over a finite range, the range of speed control is from full off to full on.

8.9 POLYPHASE SCR CIRCUITS

The use of controlled rectifiers is by no means limited to single phase AC circuits. They may be used in polyphase circuits just as conventional two element semiconductor rectifiers. Regardless of the particular circuit configuration the two basic requirements that must be met are the supplying of a trigger turn-on signal at the appropriate time and provision in the circuit external to the controlled rectifier for turn-off.

With regard to turn-off the reversal of the line voltage across the device in common rectifier circuit configurations will return the controlled rectifier to a forward blocking state; this is often referred to as line commutation. On commutating, the rectifier is subjected to reverse voltage which facilitates the turn-off process. For this reason, common AC rectifier circuits do not impose unusual turn-off requirements on the controlled rectifier as do certain types of inverter or DC chopper circuits in which forward voltage is reapplied to the controlled rectifier immediately following turn-off. However, depending on the amount of phase retard the controlled rectifier and its associated rectifiers may be subjected to full peak reverse blocking voltage immediately after having conducted full rated current. This type of service is conducive to the generation of recovery voltage transients. Particularly, in cases where SCR's are used in series in a leg of such a circuit, steps must be taken to force proper sharing of these transients between all the cells of the leg. This is discussed more fully in Chapter 6.

The question of utilizing controlled rectifiers in polyphase circuits involves providing appropriately timed triggering signals in accordance with the type of circuit used and the degree of phase control required. For example, the circuit of Figure 8.35 shows the popular three phase bridge circuit in which the forward legs are controlled and the back legs consist of uncontrolled conventional two element rectifiers. This circuit will give full continuous control from zero to 100% of its DC output when triggering signals capable of being phase shifted over 180 electrical degrees are supplied as shown in Figure 8.36(a).

The circuit discussed in Section 8.10.3 will provide such triggering signals. If triggering signals are supplied as shown in Figure 8.36(b) such that they can be phase-shifted over 120 electrical degrees, the circuit will deliver full control from about 25% to 100% of full output power to the load. A circuit to do this is discussed in Section 8.10.2.

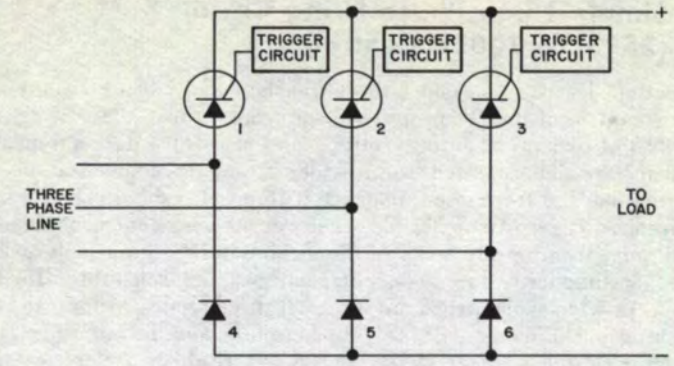


Figure 8.35 Three Phase Bridge Circuit With Three Controlled Legs

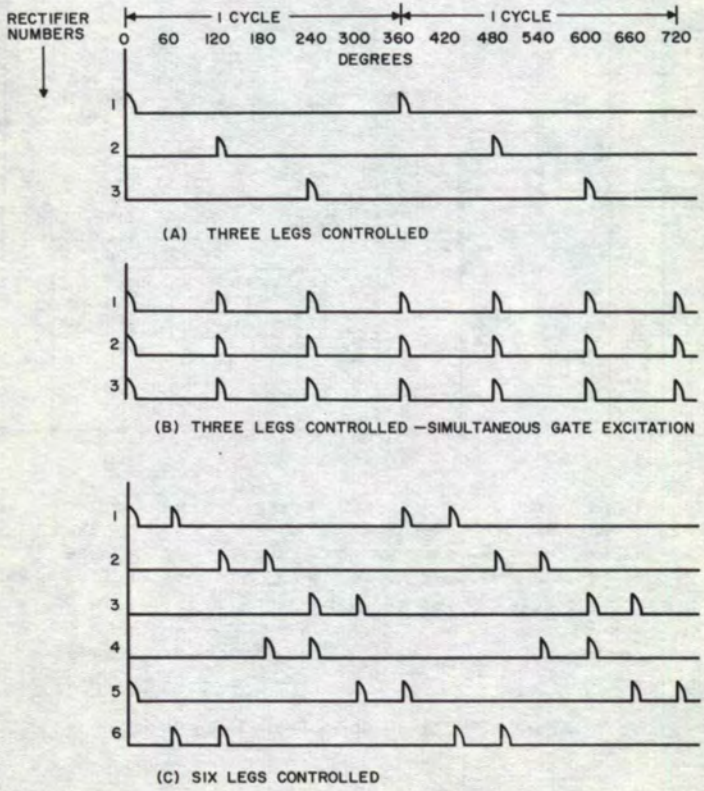


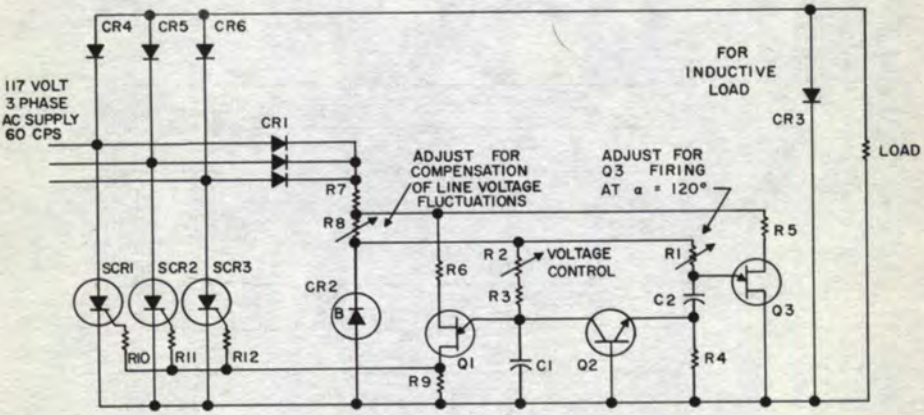
Figure 8.36 Triggering Pulses for Three Phase Bridge Circuit

In some special cases it is desirable to control all six elements of the three phase bridge circuit. Regenerative braking of a DC machine where either field or armature reversing is provided is an example of such a case. For this case, triggering signals capable of being phase-shifted over 120 electrical degrees must be supplied as shown in Figure 8.36(c).

8.9.1 Simple Three Phase Firing Circuit (25% To 100% Control)

This section describes a simple three-transistor SCR firing circuit that provides stepless control of the DC output voltage from a three-phase bridge between 25% and 100% of maximum output voltage, and also full interruption of output voltage. Means are incorporated to provide automatic compensation for line voltage fluctuations and for phase unbalance without closed-loop feedback.

This circuitry is readily applicable wherever stepless control is not required over the full range from zero to 100% of the maximum DC output voltage. Its main features are its simplicity, low cost, compactness, and reliability. Its inherent characteristics provide symmetrical output in all three phases without the need for special matching and adjustment of individual circuits, and the circuit is insensitive to power factor or phase reversal. It lends itself readily to electrical feedback techniques and does not require a separate control voltage supply. No magnetic components are needed.



CR1 — (3) G-E IN1695
CR2 — 20 VOLT, 1 WATT ZENER DIODE, IN1527
CR3, CR4, CR5, CR6 — AS REQUIRED FOR LOAD (e.g. IN2156)
SCR1, SCR2, SCR3 — AS REQUIRED FOR LOAD (e.g. C35B
Q1, Q3 — G-E 2N2646 Q2 — G-E 2N2923
R1 — 10K POT
R2 — 20K POT
R3 — 470 Ω
R4 — 100 Ω
R5, R6 — 390 Ω
R7 — 3.3K, 2W
R8 — 500 Ω POT, 2W
R9 — 100 Ω
R10, R11, R12 — 25 Ω
C1 — 0.5 MFD
C2 — 1.0 MFD

Figure 8.37 Simple Three Phase Firing Circuit

Figure 8.37 illustrates the complete firing circuit. CR_1 supplies positive line voltage to the control circuit whenever the anode voltage on an SCR swings positive with respect to the positive DC bus. This voltage is clipped at 20 volts by zener regulator CR_2 and supplies a conventional unijunction transistor relaxation oscillator firing circuit of a type described in detail in Chapter 4. R_2 controls the firing angle of Q_1 by regulating the charging rate to capacitor C_1. The pulse of voltage developed across R_9 as unijunction Q_1 discharges C_1 is coupled simultaneously

to the gates of all three controlled rectifiers, SCR_1, SCR_2, and SCR_3, through R_{10}, R_{11}, and R_{12}. Whichever SCR has the most positive anode voltage at the instant of the gate pulse starts conduction at that point.

The circuit composed of transistors Q_2 and Q_3 prevents Q_1 from firing at any delay angle greater than 120°. If triggering pulses are retarded beyond 120°, the output voltage rises abruptly to 100% as the following phase is fired at the beginning of its cycle. Q_3 is an independent unijunction oscillator which initiates its timing cycle at the same instant as Q_1. R_1 is set at a fixed value so that Q_3 fires at an angle slightly less than 120°. Two modes of operation are possible:

1. If Q_1 triggers before retard angle $\delta = 120°$, it fires the SCR whose positive anode voltage is providing the interbase bias for the unijunctions through CR_1. Firing this SCR shorts the control circuit supply voltage. The interbase bias voltage of Q_3 drops to zero, causing Q_3 to fire and discharge C_2 in preparation for the next cycle. This is the mode of operation when Q_1 is controlling the DC output voltage between 25% and 100% of maximum. In this mode, Q_2 and Q_3 have no effect on the functioning of the bridge.
2. If Q_1 is delayed beyond $\delta = 120°$, Q_3 fires, discharging C_2 through the base-emitter junction of Q_2, saturating this device, and discharging C_1 through Q_2. This alternate mode of discharging C_1 does not impose a pulse on the SCR gates, and the DC output voltage is therefore zero in this mode.

Instead of mechanical manipulation of potentiometer R_2 to control the DC output voltage, electrical signals can be used to control the output by inserting a transistor in series with R_2 in the charging path for C_1, or alternately a transistor in shunt with C_1. Both methods are readily useful in conjunction with feedback systems and are described in Chapter 4, and in Section 8.4.

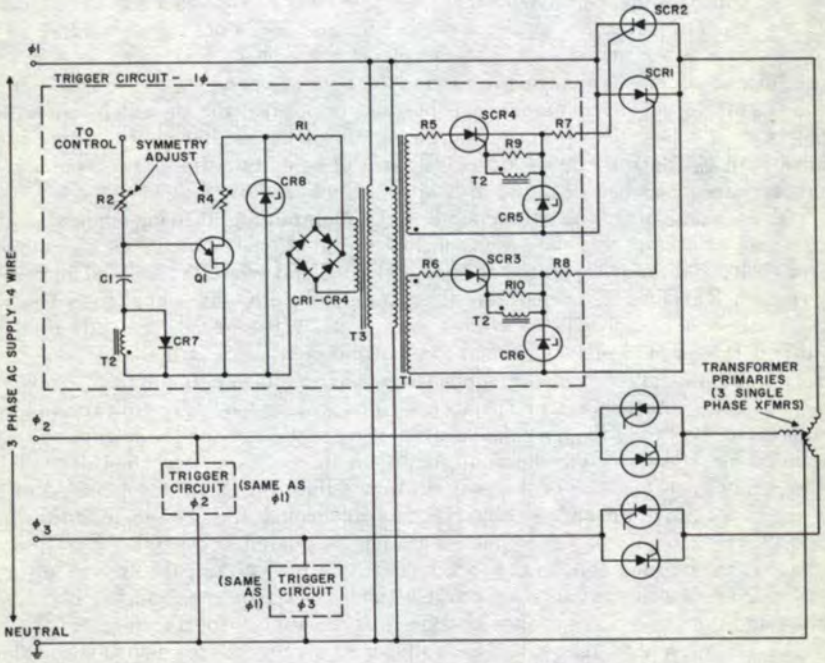
The success of this circuit depends on Q_3 maintaining its firing angle at slightly less than 120°. For this reason, base 2 of unijunction transistor Q_3 is connected through R_5 to a point separated from the clipped and regulated voltage across CR_2 by resistor R_8. This acts to maintain the timing cycle of Q_3 fixed at slightly less than 120° regardless of normal line voltage variations. Without this precaution, a drop in line voltage would make Q_3 fire at a somewhat greater angle than 120° due to the lesser slope on the front of the clipped sine wave voltage being applied to R_1.

R_8 serves another useful purpose. By connecting base 2 of unijunction transistor Q_1 to the top of R_8, a marked degree of regulation of the DC output voltage is provided for AC line voltage fluctuations. If the line voltage rises, the interbase bias voltage and therefore the peak-point emitter voltage on Q_1 rises depending on the setting of R_8. Since the emitter charging circuit through R_2 is connected to the fixed voltage across regulator CR_2, the firing angle is phased back and the output DC voltage is maintained constant. For a decrease in line voltage, this action advances the firing angle to maintain the output constant. This inherent action is instantaneous and does not depend on a change in the actual output voltage to take corrective action. Where unequal phase voltages exist, this circuit also acts to balance the contribution of the individual phases to the DC output voltage, thus reducing the fundamental frequency ripple content in the DC. Since the compensation provided by R_8 is not constant at all firing angles, R_8 should be adjusted for optimum action near the voltage level at which operation will normally take place.

With a three-phase 117 VAC supply, the circuit in Figure 8.37 can be varied steplessly over DC output voltages from 40 volts to 150 volts DC, a range of 3.75 to 1. It can also be turned off completely. With line voltage variations of $\pm 10\%$, R_8 can be adjusted to provide essentially constant DC output voltage at both extremes of line voltage. Test data with $R_8 = 350$ ohms, with 10 ohms of load, and with G-E C35B cells as the SCR's showed that for a variation in AC line input voltage from 130 volts to 100 volts the DC output varied from 93 volts to 92 volts.

8.9.2 Full Range Three Phase Control System

Figure 8.38 illustrates a phase-controlled circuit for a four wire AC system feeding three wye connected transformers. One pair of SCR's is connected in series with each of the lines and the transformer neutral is connected to the system neutral. Trigger circuits similar to the single phase type are connected from line to neutral of each phase. For illustrative purposes, a unijunction transistor is used to trigger the pilot SCR's. So that all three trigger circuits can be controlled simultaneously with a single adjustment or electrical signal, each unijunction circuit is isolated from the power circuit by a transformer T_3. This permits the three unijunction circuits to be electrically inter-connected at any convenient point. Several variations for controlling the three unijunctions from a master signal are shown in Figure 8.39. The most suitable type depends on whether manual or electrical control is desired, also the magnitude and impedance level of the available master control signal.



R1 – 3.3K, 5 WATT
R2 – SEE FIG. 8
R4 – 10K, 1 WATT
R5, R6 – 22Ω, 2 WATT
R7, R8 – 33Ω, 2 WATT
R9, R10 – 47Ω, 1/2 WATT

C1 – 0.1 MFD
Q1 – G-E 2N2646
SCR1, SCR2 – AS REQUIRED
SCR3, SCR4 – G-E 2N1595
CR1 TO CR4 – G-E 1N1693
CR5, CR6 – G-E 1N1765
CR7 – G-E 1N1692
CR8 – G-E 1N1776

T1 – ISOLATION TRANSFORMER WITH 12.6 VOLT, 1/4 AMP, SECONDARIES, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE

T2 – PULSE TRANSFORMER PE 2229, UTC H51 OR EQUIVALENT

T3 – ISOLATION TRANSFORMER WITH 120 VOLT, 50 MA SECONDARY, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE (FOR 120 VOLT PRIMARY, TRIAD N-51X)

Figure 8.38 Phase Control for Three Phase, Four Wire Power System Feeding Wye Connected Transformers

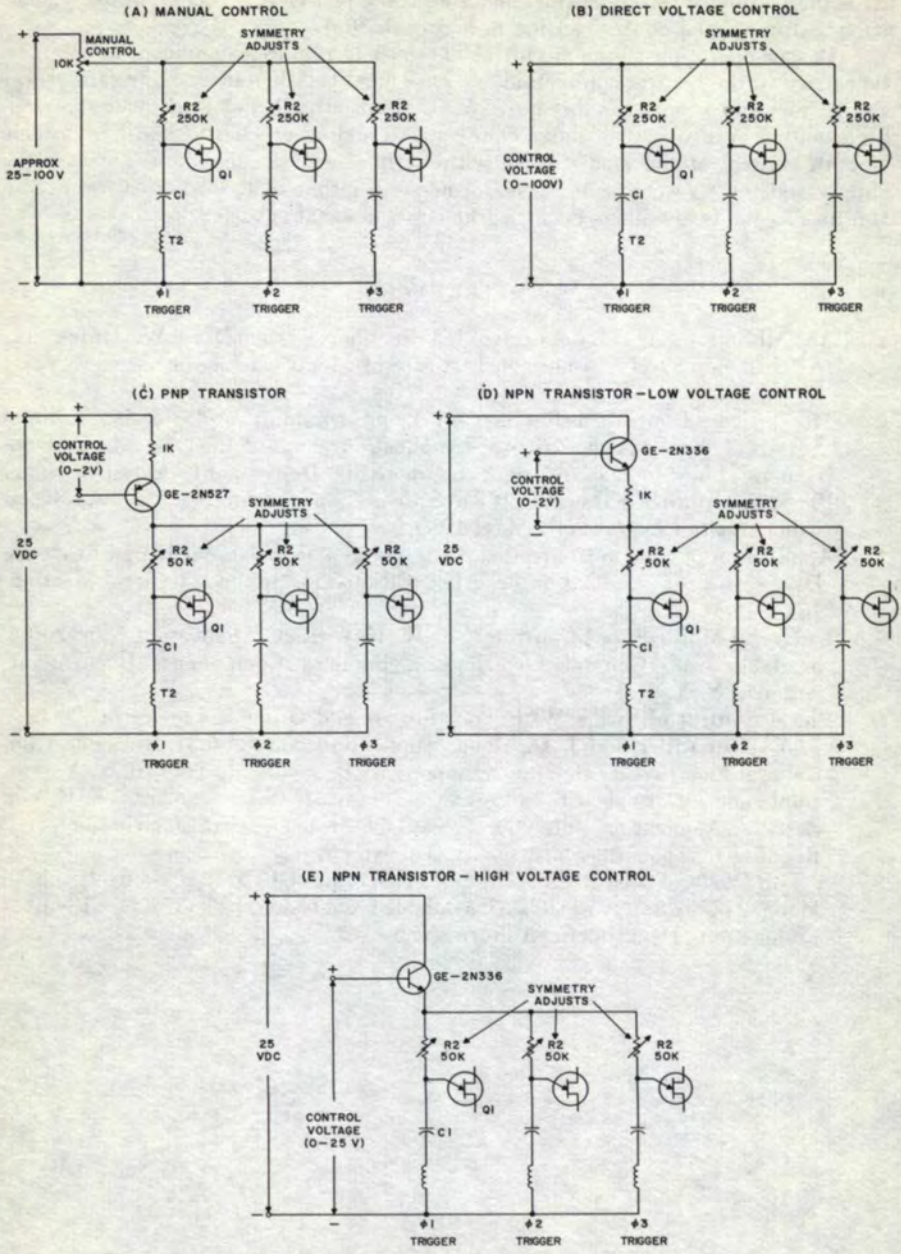


Figure 8.39 Control Circuits for Three Phase Circuit of Figure 8.36

Adjustments are provided in each unijunction circuit for establishing symmetrical firing between the phases. R_4 in each circuit is set so that all three unijunctions trigger at the same emitter voltage (voltage across C_1 and primary of T_2).

R_2 is then adjusted for equal tracking of all three phases to a single control signal, such as the manual control setting in Figure 8.29(a).

Proper operation of the circuit of Figure 8.38 requires significant currents to be carried in the neutral connection and care must be taken in designing the power conductors and supply for this purpose. This circuit will not work over the complete voltage range with a delta connected transformer. Neither will it provide smooth control of the load voltage without the neutral connection between the supply and the wye connected transformers. In either of these two cases discontinuities in the load voltage occur as the control signal is varied.

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2. "The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service," E. E. Von Zastrow, Application Note 200.14, available from General Electric Co., Rectifier Components Department, Auburn, N. Y.
3. "Phase-Controlling Kilowatts With Silicon Semiconductors," F. W. Gutzwiller, *Control Engineering*, May, 1959.
4. "Application of Silicon Controlled Rectifiers in a Transistorized High-Response DC Servo System," C. Cantor, AIEE CP 60-864, Summer General Meeting, June, 1960.
5. "Universal Motor Speed Controls," F. W. Gutzwiller, Application Note 200.4, available from General Electric Co., Rectifier Components Department, Auburn, N. Y.
6. "Phase Control of SCR's With Transformer and Other Inductive AC Loads," F. W. Gutzwiller and J. D. Meng, Application Note 200.31, available from General Electric Co., Rectifier Components Department, Auburn, N. Y.
7. "Simple and Low Cost SCR Trigger Circuits for AC Phase Control," E. E. Von Zastrow, Application Note 200.26, available from General Electric Company, Rectifier Components Department, Auburn, N. Y.
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Choppers, Inverters And Cycloconverters

This chapter describes choppers, inverters and cycloconverters using SCR's which perform the functions previously performed by electrical machines, mechanical contacts, spark gaps, vacuum tubes, thyratrons and power transistors. These functions include standby power supplies, vibrator power supplies, radio transmitters, sonar transmitters, variable-speed AC motor drives, battery-vehicle drives, ultrasonic generators, ignition systems, pulse-modulator switches, etc.

The advantages of using equipment with solid-state switches to perform these functions are:

Low maintenance
Reliability
Long life
Small size
Light weight
Silent operation
Insensitivity to atmospheric cleanliness or pressure
Tolerance of freezing temperatures
Operable in any attitude
Instantaneous starting
High efficiency
Low cost

9.1 CLASSIFICATION OF INVERTER CIRCUITS

The following definitions are used in this chapter:

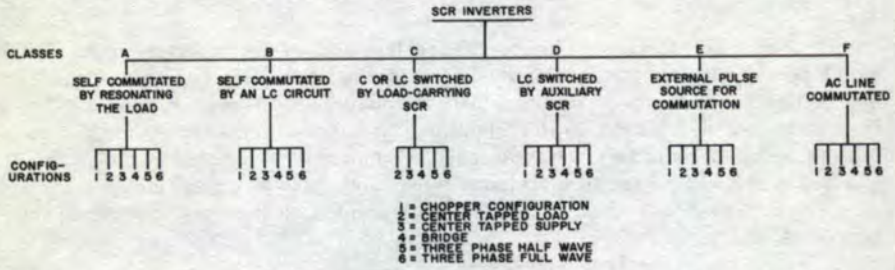
Rectifier:	Equipment for transforming AC to DC
Inverter:	Equipment for transforming DC to AC
Converter:	Equipment for transforming AC to AC
DC Converter:	Equipment for transforming DC to DC
Cycloconverter:	Equipment for transforming a higher frequency AC to a lower frequency without a DC link
Cycloinverter:	The combination of an inverter and a cycloconverter
Chopper:	A "single ended" inverter for transforming DC to DC or DC to AC

Note: The term inverter is also used in this chapter as a generic term covering choppers, inverters, and the several forms of converters. Thus "Classification of Inverters" covers classification of Choppers, Inverters, Converters, and DC Converters.

9.1.1 Classes of Inverter Circuits (Table 9.1)

The basic classification of inverter circuits is by methods of turn-off. These have been described in Chapter 5. There are six classes:

Class A Self commutated by resonating the load[1]
Class B Self commutated by an LC circuit[2]
Class C C or LC switched by a load-carrying SCR[3]
Class D C or LC switched by an auxiliary SCR[4]
Class E External pulse source for commutation[5]
Class F AC line commutated[6]



9.1.2 Properties of the Inverter Classes

Class A—Self commutated by resonating the load. These inverters are most suitable for high-frequency operation, i.e. above about 1000 cps, because of the need for an LC resonant circuit which carries the full load current. The current through the SCR is nearly sinusoidal and so the initial di/dt is relatively low. Class A inverters lend themselves to output regulation by varying the frequency of a pulse of fixed width (time ratio control). These inverters are sensitive to load changes.
Class B—Self commutated by an LC circuit. The great merit of this class is circuit simplicity, the Morgan chopper being an outstanding example. Regulation is by time ratio control. Where saturable reactors are used, some skill is necessary in the design of these components, and manufacturing repeatability must be checked.
Class C—C or LC switched by a load-carrying SCR. An example of this class of inverter is the well known McMurray-Bedford inverter. With the aid of certain accessories this class is very useful at frequencies below about 1000 cps. External means must be used for regulation.
Class D—C or LC switched by an auxiliary SCR. This type of inverter is very versatile as both time-ratio and pulse-width regulation is readily incorporated. The commutation energy may readily be transferred to the load and so high efficiencies are possible.
Class E—External pulse source for commutation. This type of commutation has been neglected. It is capable of very high efficiency as only enough energy is supplied from the external source for commutation. Both time-ratio and pulse-width regulation are easily incorporated.
Class F—AC line commutated. The use of this type of inversion is limited to those applications where a large amount of alternating power is already available. Efficiencies are very high.

9.1.3 Inverter Configurations

Rectifier circuits occur in several configurations such as half-wave, full-wave, bridge, etc. Inverter circuits may be grouped in an analogous manner.

Figure 9.1 shows the different types of configurations. Methods of triggering and commutation have been left out for clarity.

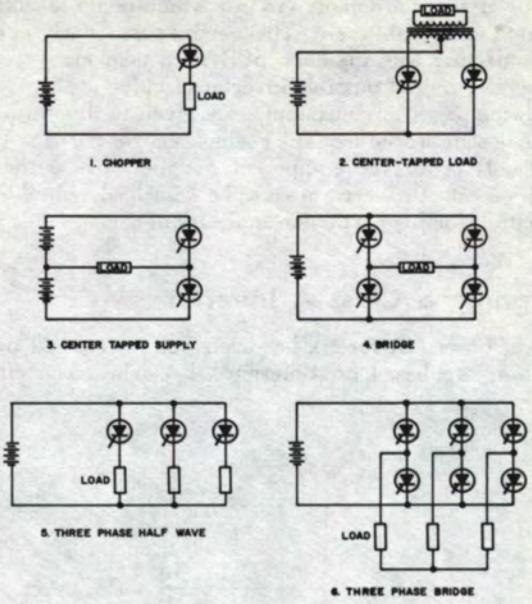


Figure 9.1 Inverter Configurations

9.1.4 Properties of the Different Inverter Configurations

CONFIGURATION	1	2	3	4	5	6
	Chopper	CT Load	CT Supply	Bridge	3φ Half-Wave	3φ Bridge
Blocking Volts (1)	E	2E	E	E	E	E
Peak Load-Volts	E	E (2)	½ E	E	E	E (3)
DC in Load	yes	no	no	no	yes	no (4)
Number of SCR's	1	2	2	4	3	6
Ripple Frequency in Supply	f	2f	f	2f	3f	6f
Ave SCR Current (1) / Supply Current	1	1/2	1	1/2	1/3	1/3
Transformer-less Operation Possible	yes	no	yes	yes	yes	yes

(1) Ignoring overshoot due to commutation.
(2) Using a 1:1:1 transformer.
(3) Line-to-line voltage.
(4) Assuming symmetrical loading.

9.1.5 Discussion of Classification System

This method of classification gives thirty-five (35) different classes and configurations. However there are many circuits which could fall into the same classification and which are yet different. This occurs particularly in Class D where the method of commutating the auxiliary SCR may take many forms. There must therefore be several hundred possible inverter circuits.

In the following pages three examples are given to illustrate the scope of SCR inverters and the design procedure. The examples cover perhaps 1% of the possible circuit variations. It is for the equipment designer to use the classes and configurations together with the accessories to be described as building blocks to form the best combination for his particular application.

9.2.1 Designing a Class A Inverter

The design of Class A inverters has been well covered in the literature.[1] The following equations are based on Reference 1.4. The basic circuit is shown in Figure 9.2.1.

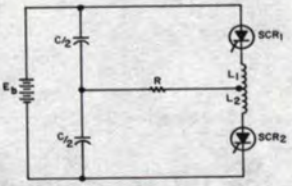


Figure 9.2.1 A Basic Class A Circuit

The operation is as follows: Triggering SCR_1 will produce a half sine-wave pulse through R and charge C. This charge, and consequently the reverse voltage across SCR_1, will be held until SCR_2 is triggered. On triggering SCR_2 a current pulse, this time of opposite polarity, now flows through R. C is discharged and recharged in the opposite direction ready for the next gate pulse on SCR_1.

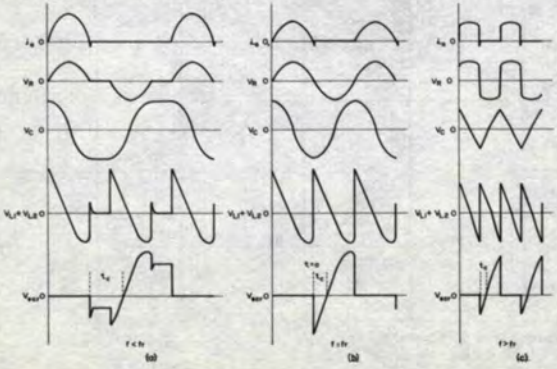


Figure 9.2.2 Class A Inverter Waveforms

Figure 9.2.2(a) shows the current and voltage waveforms with the triggering frequency less than the resonant frequency of L and C, i.e. $f < f_r$. Figure 9.2.2(b) shows the same waveform with $f = f_r$ and Figure 9.2.2(c) with $f > f_r$. Figure 9.2.2(b) is the sinusoidal case and is generally the most desirable. With most loads however, changes in reactance occur and excursions into the modes of (a) and (c) are possible.

Note that the current pulses through L_1 and L_2 combined are in the same direction and occur at twice the triggering frequency. DC current flows through L_1 and L_2 equal to the supply current. Saturation must be avoided.

9.2.1.1 Design Procedure

Required Specifications

Required output power P_o (watts)
Required output frequency f (cycles/second)
Available DC supply voltage E_b (volts)

Input Power

Assume 90% efficiency

$$P_I = P_o \times \frac{100}{90} \text{ (watts)}$$

Supply Current, I_b = Average Current Through SCR, $I_{AV(SCR)}$

$$I_b = I_{AV(SCR)} = \frac{P_I}{E_b} \text{ (amps)}$$

As the current flows in half-sine wave pulses, $f = f_r$,

$$I_b = I_{AV(SCR)} = \frac{I_{PK(SCR)}}{\pi} \text{ (amps)}$$

This value of $I_{AV(SCR)}$ makes a preliminary choice of SCR possible.

Peak Anode Current

$$I_{PK(SCR)} = \pi I_b \text{ (amps peak)}$$

Load Resistor

$$R = \frac{2\,E}{\pi^2\,I_b} \text{ (ohms)}$$

Load Voltage

$$V_{R(PK)} = \frac{2\,E_b}{\pi} \text{ (volts peak)}$$

Q

Choose a value of Q between 1 and 4. A high value of Q has the advantage of increasing the turn-off time t_c. The disadvantages of high Q are: Higher voltage SCR must be used; the dv/dt is higher; the size of L and C increases.

Capacitor

$$C = \frac{10^6}{2\,\pi\,Q\,f\,R} \text{ } (\mu f)$$

Inductor

$$L = L_1 = L_2 = \frac{QR}{2\,\pi\,f} \times 10^6 \text{ } (\mu H)$$

Peak Voltage Across Capacitor

$$V_{C/2(PK)} = Q v_{R(PK)} \text{ (volts peak)}$$

RMS Current through Inductor

$$I_L = \frac{I_{PK(SCR)}}{2} \text{ (amps rms)}$$

The following three relations are derived from $v_{scr} = 2\, v_{R(PK)}\ (Q \cos \omega t - \sin \omega t)$

Peak Forward Voltage Across SCR

$$v_{(PK)SCR} = \frac{4E}{\pi} \sqrt{Q^2+1} \text{ (volts peak)}$$

Maximum Circuit dv/dt

$$dv/dt = \frac{8Ef\sqrt{Q^2+1}}{10^6} \text{ (volts per } \mu s)$$

Circuit Turn-Off Time

$$t_c = \frac{10^6}{2\pi f} \tan^{-1} Q \ (\mu s)$$

Losses in Capacitors

$$P_c = \frac{Q}{Q_c} P_I \text{ (watts)}$$

where Q_c is the Q of capacitor C

Losses in Inductors

$$P_L = \frac{Q}{Q_L} P_I \text{ (watts)}$$

where Q_L is the Q of inductor L_1, L_2

SCR Losses

Plot the current waveform on the instantaneous power dissipation versus time curves (Figure 3.10) given in the specification sheet. Replot the intersections of the current curve and the power lines on linear paper. Integrate graphically to find the average power dissipation. Check that the current curve does not cross the turn-on power limit line. Derate for frequency as needed.

Other Losses

The following losses have been neglected:

Resistance of wiring
Transformer losses
H.F. current in filter capacitor
Trigger-circuit losses
SCR losses due to leakage current

Power Output

$$P_O = P_I - (P_c + P_L + 2\, P_{SCR}) \text{ (watts)}$$

Efficiency

$$\eta = \frac{P_O}{P_I} \times 100\%$$

If η differs appreciably from 90%, recalculate using the revised value of P_I.

9.2.1.2 An Ultrasonic Generator

An ultrasonic generator design is given as an illustrative example of the application of a Class A inverter.[1-5]

A frequency doubling mode is used in order to obtain satisfactory operation at 25 kc/s using inexpensive SCR's.

Figure 9.2.3 shows the basic circuit.

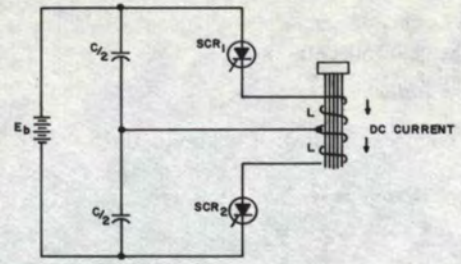


Figure 9.2.3 Class A Frequency Doubler with Transducer Load

Note that the load resistance is in the magneto-strictive transducer winding L. The frequency-doubling effect can be seen by reference to Figure 9.2.2. The circuit is actually a 25 kc inverter being triggered at a 12.5 kc repetition rate. The procedure is to calculate the component values using double the power output. For current and power figures divide the 25 kc results by two.

Required Specifications

$P_o = 100$ watts
$f = 25$ kc/s
Available supply voltage = 50 volts DC
Q of the transducer = 5.

Input Power

$$P_I = 100 \times 2 \times \frac{100}{90} = 220 \text{ watts}$$

Supply Current = Average Current Through SCR

$$I_b = \frac{220}{50} = 4.4 \text{ (2.2 amps for 12.5 kc triggering)}$$

A suitable low-cost SCR for this application is the G-E C20X31 SCR which has a specified turn-off time of 20 μs.

Peak Anode Current

$$I_{PK(SCR)} = \pi(4.4) = 13.8 \text{ amps peak}$$

Load Resistor

$$R = \frac{2}{\pi^2} \cdot \frac{50}{4.4} = 2.3 \text{ ohms}$$

Load Resistor Voltage

$$v_R = \frac{2 \times 50}{\pi} = 32 \text{ volts peak}$$

Q is given as 5.

Capacitor

$$C = \frac{10^6}{2\pi 5 \times 12{,}500 \times 2.3} = 1.1 \ \mu\text{f total}$$

$$C/2 = .55 \ \mu\text{f}$$

Inductor

$$L = L_1 = L_2 = \frac{5 \times 2.3 \times 10^6}{2 \times \pi \times 12{,}500} = 145\ \mu H$$

Peak Voltage Across Capacitor

$$v_{C/2} = 5 \times 32 = 160 \text{ volts peak}$$

RMS Current Through Inductor

$$I_L = \frac{6.9}{2} = 3.45 \text{ amps RMS } (\approx 2 \text{ amps RMS for 12.5 kc triggering})$$

Peak Forward Voltage Across SCR

$$v_{PK(SCR)} = \frac{4 \times 50}{\pi}\sqrt{5^2+1}$$

$$= 325 \text{ volts}$$

Maximum Circuit dv/dt

$$dv/dt = \frac{8 \times 50 \times 12{,}500\sqrt{5^2+1}}{10^6}$$

$$= 25.5 \text{ volts per } \mu s$$

Circuit Turn-Off Time

$$t_c = \frac{10^6}{2\pi \times 25{,}000}\tan^{-1} 5$$

$$= 8.7\ \mu s$$

Add one half cycle or 20 μs for 12.5 kc triggering which gives $t_c = 28.7\ \mu s$.

Losses in Capacitors

Assume a capacitor Q of 100

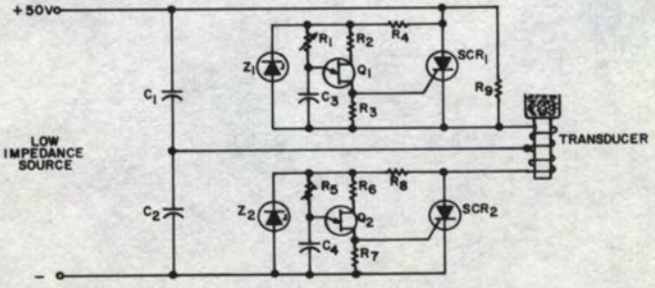
$$P_C = \frac{5}{100} \times 110 = 5.5 \text{ watts}$$

Losses in Inductor

The inductor losses are, in this case, incorporated in the Q of 5.

The Ultrasonic Generator Circuit

Figure 9.2.4 shows a complete circuit.



C_3 - 0.003μf, 100V PAPER
C_4 - 0.003μf, 100V PAPER
C_1 AND C_2 - 0.5μf, GE 28F1310
R_1 - 25K, 2W POTENTIOMETER
R_2 - 180Ω, 1W
R_3 - 100Ω, 1/2W
R_4 - 2.2KΩ, 2W
R_5 - 25K, 2W POTENTIOMETER
R_6 - 180Ω, 1W
R_7 - 100Ω, 1/2W
R_8 - 2.2KΩ, 2W
R_9 - 10KΩ, 2W
Q_1 - GE 2N2647
Q_2 - GE 2N2647
SCR_1 - GE C20DX3I
SCR_2 - GE C20DX3I
Z_1 - Z4XL22
Z_2 - Z4XL22

Figure 9.2.4 100W, 25kc Ultrasonic Generator

The trigger circuit consists of two UJT relaxation oscillators each deriving its power from the anode to cathode voltage of an SCR. This arrangement gives great triggering reliability as an SCR cannot be triggered until the blocking voltage has been applied. This reliability is achieved at some cost of output power. Resistor R9 allows some current to bypass SCR_1 and charge up the capacitors thus initiating the oscillations by triggering SCR_2.

The choice of the General Electric C20D is adequate for this circuit provided an adequate heatsink is used. The standard unit has no guaranteed dynamic characteristics so some selection may be necessary for this operation. Use the GE C20DX31.

9.2.2 Designing a Class C Inverter

Typical of the Class C inverter is the well-known "McMurray-Bedford Inverter."[3-2] This inverter circuit is shown in Figure 9.2.5. It operates as follows. Assume SCR_1 conducting and SCR_2 blocking. Current from the DC supply flows through the left side of the transformer primary. Autotransformer action produces a voltage of $2E_b$ at the anode of SCR_2 charging capacitor C to $2E_b$ volts. When SCR_2 is triggered, point (A) rises to approximately $2E_b$ volts, reverse biases SCR_1, and turns it off. Capacitor C maintains the reverse bias for the required turn-off time. When SCR_1 is again triggered, the inverter returns to the first state. It follows that the DC supply current flows alternately through each side of the transformer primary producing a square-wave AC voltage at the secondary.

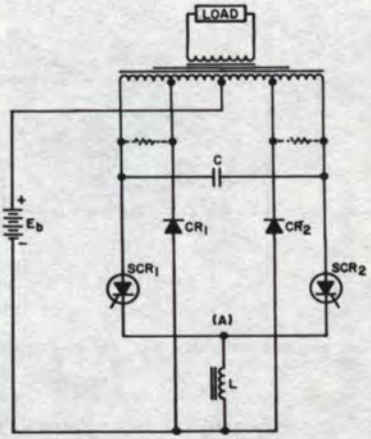


Figure 9.2.5 McMurray Bedford Inverter

Rectifiers CR_1 and CR_2 feed back, to the DC supply, reactive power associated with capacitive and inductive loads. With inductive loads, energy stored in the load at the end of a half cycle of AC voltage is returned to the supply at the beginning of the next half cycle. Conversely with capacitive loads, energy stored in the load at the beginning of a half cycle is returned to the supply later in that half cycle.

The feedback rectifiers are connected between the negative supply terminal and taps on the transformer primary. In applications where losses would not be

excessive, the diodes may be returned to the SCR anodes through small resistances as indicated by the dashed lines in Figure 9.2.5. In the tap connection some energy trapped in L is fed to the load. Use of the tap connection results in some variation of output with load power factor, but far less than with no feedback rectifiers.

Optimum values for the commutating elements of a "McMurray-Bedford Circuit" are:

$$C = \frac{t_c\, I_{com}}{1.7\, E_b}$$

$$L = \frac{t_c\, E_b}{0.425\, I_{com}}$$

where t_c = minimum turn-off time presented to the SCR

I_{com} = maximum value of load current at commutation

Inverter waveshapes for different load power factors are shown in Figure 9.2.6.

The above relations define C and L such that commutation is insured for maximum lagging load current.

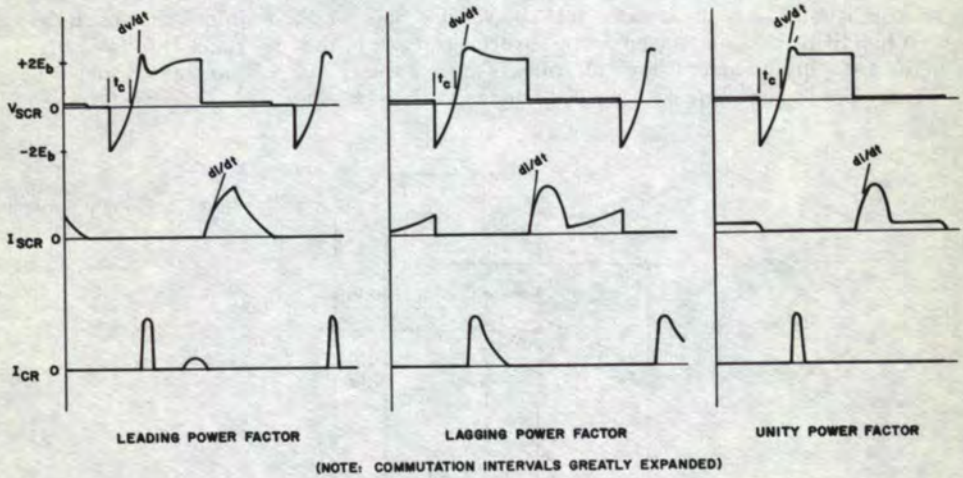


Figure 9.2.6 Inverter Waveshapes for Various Load Power Factors

A useful accessory which may gainfully be employed with the Class C inverter is the Ott filter (see Section 9.3.4.2). This filter provides a sine wave output with good load regulation while presenting a capacitive load to the inverter over a large range of load power factor. This capacitive load to the inverter simplifies the SCR commutation situation. The filter circuit is shown in Figure 9.3.5(a). Figure 9.3.5(b) relates load impedance to filter input impedance. The radial lines emanating from the origin represent loci of constant load phase angle, the circles with centers at the origin are loci of constant load impedance magnitude. The other two sets of loci represent filter input impedance (magnitude and phase angle). All impedance magnitudes are normalized to the filter design impedance. Note that for the input impedance to be capacitive for any load power factor, the normalized, rated, load impedance must be two or greater.

9.2.2.1 Design Procedure

The following is the design procedure for a Class C square wave inverter used in connection with the Ott filter to produce sinusoidal voltage.

Required Specifications

Output voltage (E_o)—Volts (RMS)
Output power (P_o)—watts
Output frequency (f)—cps
Rated load power factor (pf)
Available DC supply (E_b)—volts

FILTER DESIGN

Load Resistance

$$R_L = \frac{1}{P_o}\left[\frac{E_o}{1+\left[\frac{\sqrt{1-pf^2}}{pf}\right]}\right]^2 \text{ (ohms)}$$

Load Reactance

$$X_L = \frac{R_L}{pf}\sqrt{1-pf^2} \text{ (ohms)}$$

Load Impedance

$$|Z_L| = \sqrt{R_L^2 + X_L^2} \text{ (ohms)}$$

$$\angle Z_L = \cos^{-1} pf \text{ (degrees)}$$

Filter Design Impedance

$$Z_D \leqq \frac{|Z_L|}{2} \text{ (ohms)}$$

Design Radian Frequency

$$\omega_D = 2\pi f \text{ (radians/sec)}$$

Filter Element Values

$$C_1 = \frac{1}{6 Z_D \omega_D} \qquad C_2 = \frac{1}{3 Z_D \omega_D} \text{ (farads)}$$

$$L_1 = \frac{9 Z_D}{2 \omega_D} \qquad L_2 = \frac{Z_D}{\omega_D} \text{ (henrys)}$$

Filter Input Impedance

Z_{IN}, R_{IN} and X_{IN} are determined from Figure 9.3.5(b)

Input Voltage to Filter

$$E_{(SQ)} = \frac{\sqrt{2}}{4}\pi\left|Z_{IN}\right|\sqrt{\frac{P_o}{R_{IN}}} \text{ (volts)}$$

INVERTER DESIGN

Transformer Turns Ratio

$$n = \frac{E_{(SQ)}}{E_b}$$

Input Power, assuming 85% efficiency

$$P_I = P_o \times \frac{100}{85} \text{ (watts)}$$

Average Current in SCR

$$I_{AV(SCR)} \cong \frac{P_o \, |Z_{IN}|}{2 \, E_b \, R_{IN}}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} < 2.5 \, E_b$$

From the expressions for $I_{AV(SCR)}$ and $V_{PK(SCR)}$ a preliminary choice of SCR may be made.

Peak Current in SCR's

$$I_{PK(SCR)} = 4 \, E_b \sqrt{\frac{C}{L}}$$

Turn-Off Time

$$t_c = \frac{2\pi}{3} \sqrt{LC}$$

Rate of Reapplication of Forward Blocking Voltage

$$dv/dt = \frac{0.85 \, E_b}{\sqrt{LC}}$$

Turn-on di/dt

$$di/dt \Big|_{t=0} = \frac{2 \, E_b}{L}$$

From the preceding four relationships, L and C may be determined as follows

$$L = \frac{6 E_b \, t_c}{\pi \, I_{PK(SCR)}}$$

Choose the desired t_c and $I_{PK(SCR)}$ and determine L. Check dv/dt with the following

$$dv/dt = \frac{3.44 \, E_b^2}{L \, I_{PK(SCR)}}$$

If dv/dt is too high, increase L accordingly and recalculate $I_{PK(SCR)}$. Now:

$$C = \frac{3 \, t_c \, I_{PK(SCR)}}{8\pi \, E_b}$$

The minimum value of L should be such as to keep the turn-on di/dt well below specification.

9.2.2.2 A 400 CPS Inverter With Sine Wave Output

The design procedure for a 400 c/s inverter with sine wave output is given to illustrate the application of a Class C inverter used in conjunction with the Ott filter.

Required Specifications

Output power = 180 watts
Output voltage = 120 volts (RMS)

Output frequency = 400 cps
Rated load power factor = 0.7 lagging
Available DC supply = 28 VDC

FILTER DESIGN

Load Resistance

$$R_L = \frac{1}{180}\left[\frac{120}{1+\left[\frac{\sqrt{1-(.7)^2}}{.7}\right]}\right]^2 = 20 \text{ ohms}$$

Load Reactance

$$X_L = \frac{20}{.7}\sqrt{1-(.7)^2} = 20 \text{ ohms}$$

Load Impedance

$$|Z_L| = \sqrt{(20)^2+(20)^2} = 28.3 \text{ ohms}$$

$$\angle Z_L = \cos^{-1}(.7) = \frac{\pi}{4}$$

Filter Design Impedance

$$Z_D \leq \frac{28.3}{2}$$

Choose $Z_D = 15$ ohms

Design Radian Frequency

$$\omega_D = (2)\ (3.14)\ (400) = 2500 \text{ radians/sec}$$

Filter Element Values

$$C_1 = \frac{1}{(6)\ (15)\ (2500)} = 4.5 \times 10^{-6} \text{ farads}$$

$$C_2 = \frac{1}{(3)\ (15)\ (2500)} = 9 \times 10^{-6} \text{ farads}$$

$$L_1 = \frac{(9)\ (15)}{2\ (2500)} = 27 \times 10^{-3} \text{ henrys}$$

$$L_2 = \frac{15}{2500} \times 6 = 10^{-3} \text{ henrys}$$

Filter Input Impedance

From Figure 9.3.5(b) (point marked X)

$$Z_{IN} = (15)\ 5.5\ \angle -16^\circ$$
$$= 80 - j\ 23$$
$$R_{IN} = 80 \text{ ohms}$$
$$X_{IN} = 23 \text{ ohms}$$
$$|Z_{IN}| = 83 \text{ ohms}$$

Input Voltage to Filter

$$E_{SQ} = \frac{\sqrt{2}}{4}\ (3.14)\ (83)\ \sqrt{\frac{180}{80}} = 139 \text{ volts}$$

INVERTER DESIGN

Transformer turns ratio

$$n = \frac{139}{28} = 5$$

Input Power (assuming 85% efficiency)

$$P_I = 180 \times \frac{100}{85} = 212 \text{ watts}$$

Average Current in SCR's

$$I_{AV(SCR)} \cong \frac{(180)\ (83)}{(2)\ (28)\ (80)} = 3.4 \text{ amps}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} = (2.5)\ (28) = 70 \text{ volts}$$

From the above a G-E type C12A SCR is chosen.

Commutating Elements

The C12 has a maximum turn-off time of 12μ sec and maximum dv/dt of 20 volts/μsec. Choose $t_c = 16$ μsec and $I_{PK(SCR)} = 14$ amps.

$$L = \frac{6\ (28)\ (16)}{(14)\ (3.14)} = 60 \times 10^{-6} \text{ henrys}$$

Checking dv/dt,

$$dv/dt = \frac{(3.44)\ (790)}{(60 \times 10^{-6})\ (14)} = 3.2 \text{ volts}/\mu\text{sec}$$

$$C = \frac{(3)\ (16 \times 10^{-6})\ (14)}{(8)\ (3.14)\ (28)} = 1 \times 10^{-6} \text{ farads}$$

Turn-On di/dt

$$di/dt\Big|_{t=0} = \frac{2 \times 28}{60} = 1 \text{ A}/\mu\text{sec}$$

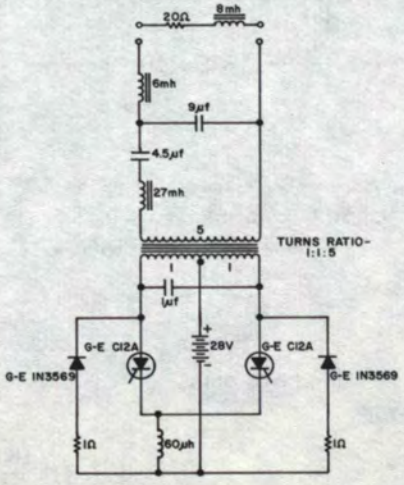


Figure 9.2.7 A 400 Cycle Inverter with the Ott Filter

NOTES:

1. Feedback rectifiers are chosen to have current and voltage capability similar to the SCR's.
2. One ohm series resistors are used to limit power dissipation in the feedback rectifiers.
3. The composite inverter-filter circuit for the 400 cps inverter is shown in Figure 9.2.7.
4. A suitable trigger circuit for the Class C inverter is shown in Figure 9.2.8.

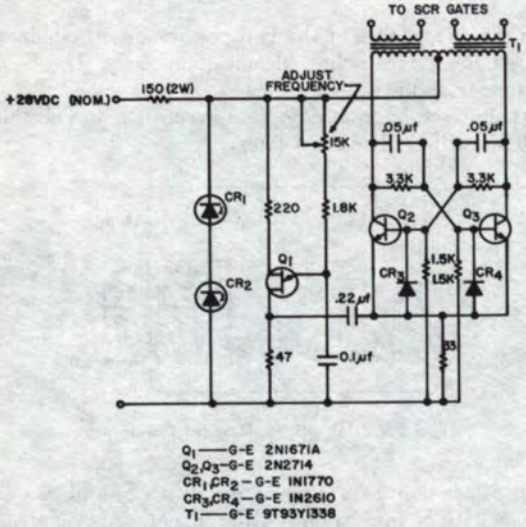


Figure 9.2.8 Trigger Circuit for Fig. 9.2.7

9.2.3 Designing a Battery Vehicle Motor-Controller Using The Jones SCR Chopper (Class D)

9.2.3.1 Introduction

Three methods are available for controlling the voltage to, and hence the speed of, a battery-driven DC series motor of any appreciable power:

1. A rheostat may be inserted in series with the motor. This method has a smooth action but power is wasted in the rheostat.
2. The battery or the field winding may be switched in series or parallel. This method is virtually lossless but the action is jerky.
3. The third method involves the use of a rapid-acting switch, called a chopper, in series with the motor.

The action of the chopper is shown in Figure 9.2.9.

At low speeds the "on" time is much less than the "off" time. The result is that the average voltage across the motor is low. As the "off" time is decreased so the average voltage increases, the change in the average voltage is as smooth as the "off" time may be readily adjusted by a potentiometer controlled timer. This

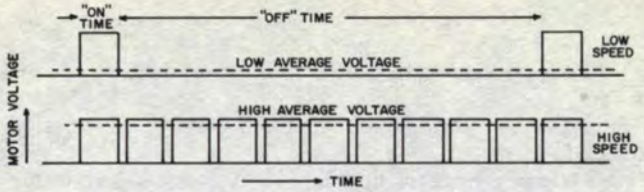


Figure 9.2.9 Chopper Waveforms

method combines the advantages of the two previous methods in that both smooth control and high efficiency are achieved simultaneously. The SCR makes an ideal switch for this chopper application.

Figure 9.2.10 shows a diagram complete except for the method of turning the SCR on and off. This will be discussed later.

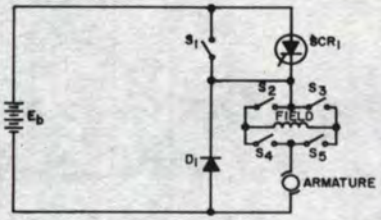


Figure 9.2.10 Basic Vehicle Connections

S_2, S_3, S_4 and S_5 are field-reversing relays. With S_2 and S_5 closed the direction is forward, whereas with S_3 and S_4 closed the direction is reverse.

This SCR chopper has a practical duty cycle ranging from about 20% to about 80%.

For the standstill state all four switches, S_2, S_3, S_4 and S_5, are open. When S_2 and S_5 are closed, and with the chopper operating at low speed, about 20% of the supply voltage is applied to the motor. This voltage may be increased to 80% of the battery voltage as more torque is required. When 80% is reached relay S_1 is closed applying full voltage to the motor and maximum torque is obtained.

The diode D_1 is the well known free-wheeling diode. Its purpose is to carry the inductive current when the SCR is turned off, thus preventing high voltages appearing across the motor.

The controller to be described uses a variable-frequency constant-pulse-width system. A variation is for the frequency to be held constant and the pulse width changed.

9.2.3.2 The Jones Commutation Circuit

Figure 9.2.11 shows the basic circuit.

SCR_1 is the load-current-carrying SCR. When the gate is triggered, current flows from the battery via winding L_1 of the autotransformer T_1 to the motor represented by an inductor L_m and a resistor R_m.

The start of the current flow induces a voltage into winding L_2 which charges up the capacitor C. This charge is held until "off" SCR_2 is triggered. The voltage across SCR_1 is then reversed and it is turned off.

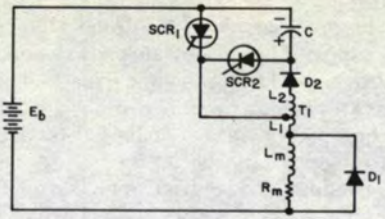


Figure 9.2.11 The Jones Chopper

One of the advantages of the Jones circuit over others is its ability to start reliably. Due to the autotransformer the capacitor is always charged up whenever load-current starts to flow and thus commutation energy is always available.

The turn-off time t_c that the circuit presents to the SCR is shortest during the first pulse of operation as the capacitor C must be assumed to be completely discharged. It is therefore important that calculations and measurements of turn-off are made with the capacitor starting at zero voltage.

Typical circuit waveforms are shown in Figure 9.2.12.

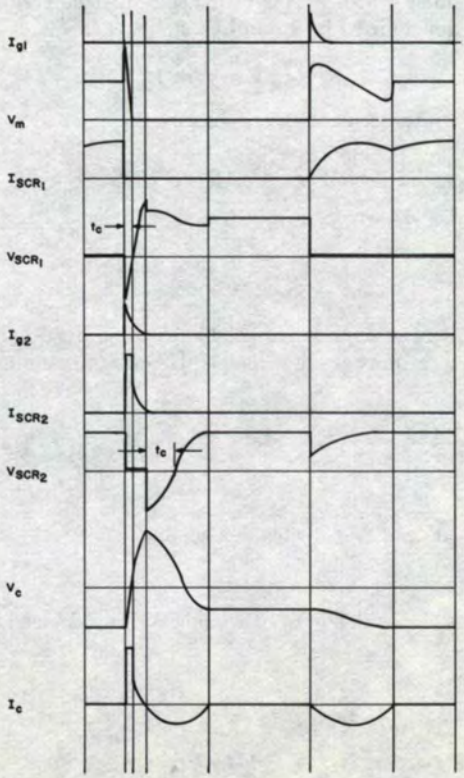


Figure 9.2.12 Waveforms in the Jones Chopper

9.2.3.3 Design Notes

At the time of writing no analysis of the Jones chopper has been made which would yield design equations. This is not surprising considering the contortions that the current goes through. The following equations are therefore given as a rough guide to the design engineer to enable him to construct a working circuit. The calculations must be checked in a breadboard model before components are specified. See 9.2.3.6 if plugging is to be used.

The following information is required: The battery voltage E_b; the locked rotor current of the motor, I_m.

Selection of SCR_1

When a bypass switch is used, such as S_1 in Figure 9.2.10, the following rule-of-thumb holds in practice. The RMS rating of $SCR_1 \geq I_m$. This assumes an adequate heatsink for SCR_1.

Capacitor C

$$C = \frac{t_{off} \times I_m}{E_b} \mu F$$

(where t_{off} is the turn-off time of SCR_1 in μs)

L_2 and Pulse Repetition Rate for 80% Voltage

The minimum pulse width that can be used must be greater than the charging time of C which is determined by L_2 and C.

Minimum pulse width $> \pi \sqrt{L_2 C}$ where L_2 is the unsaturated inductance.

A reasonable pulse width to use is $2\pi\sqrt{L_2 C}$.

For 80% voltage the period is $\frac{100}{80} \times 2\pi\sqrt{L_2 C}$

Thus, maximum pulse repetition rate

$$f = \frac{0.8}{2\pi\sqrt{L_2 C}}$$

In practice this frequency extends from 100 cps to about 400 cps. If the frequency is too low, the motor thumps at slow speeds. If too high, the motor heats up excessively.

Also

$$L_2 = \frac{16 \times 10^9}{f^2 C} \mu H$$

(where C is in μF and f in cycles per second)

Transformer T_1

A turns ratio of about 7:1 is used to achieve the desired turn-off time during the first pulse.

Thus

$$\frac{\text{Primary Turns}}{\text{Secondary Turns}} = \frac{N_1}{N_2} = \frac{1}{7} = \sqrt{\frac{L_1}{L_2}}$$

thus

$$L_1 = \frac{L_2}{49} \quad (L_1 \text{ is the unsaturated inductance.})$$

If the transformer core has an air gap made up of the ends of the laminations butting together with no spacer, the number of turns may be found from the following approximate relation.

$$N_2^2 A = \frac{L_2}{6}$$

The core is assumed to be of the stacked type where A is the core cross sectional area in square inches and L_2 is in μH.

The choice of number of turns and core size must be checked regarding the maximum flux density in the core.

$$\text{Flux density} = \frac{15\ E_b \sqrt{L_2\ C}}{N_1\ A}$$

This flux density may be run just below saturation.

Free-Wheeling Diode D_1

A rule-of-thumb for the maximum average current in D_1 is a quarter of the motor locked-rotor current I_m. (Assume 180° conduction angle.)

Average Current in SCR_2, D_2, C and L_2

The same average current flows in all four components

$$I_{avg} = f\ (CE_b + 2\ I_m \sqrt{L_1\ C}) \times 10^{-6} \text{ amps average}$$

RMS Current in L_1

A rule-of-thumb for the RMS current in winding L_1: half the motor locked-rotor current I_m.

Voltage Rating of SCR_1, SCR_2, D_1, and C

The peak forward and reverse blocking voltage across SCR_1 and SCR_2, the peak reverse voltage across D_1, and the peak voltage across C are found from the expression

$$V_{PK(SCR_1)} \leq E_b + I_m \sqrt{\frac{L_1}{C}} \text{ volts peak}$$

Voltage Rating of D_2

$$V_{PK(D1)} = \frac{N_2}{N_1} V_{PK(SCR_1)}$$

SCR Dynamic Characteristics

SCR_1

$$dv/dt = \frac{I_m}{C} \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{E_b}{L_1} \text{ amps per } \mu s$$

Circuit Turn-off time $t_c = \frac{E_b C}{I_m}$ μs

SCR_2

$$dv/dt = \frac{V_{PK(SCR_1)}}{\sqrt{L_2 C}} \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{V_{PK(SCR_1)}}{\text{Stray Inductance in Loop Formed by } SCR_1, SCR_2 \text{ and } C}$$

Circuit Turn-off time $t_c = \pi/2\sqrt{L_2 C}$ μs

9.2.3.4 Worked Example

Given: $E_b = 36$ volts
$I_m = 110$ amps

Selection of SCR_1:

The C55 has an RMS rating of 110 amps.
The turn-off time t_{off} is 20 μs at 50 amps.

Capacitor C

$$C = \frac{20 \times 110}{36} = 61 \ \mu f$$ Use a 70 μf ±10% capacitor

L_2 and Pulse Repetition Rate for 80% Voltage

Choose 250 pulses per second.

$$L_2 = \frac{16 \times 10^9}{250^2 \times 70} = 3600 \ \mu H$$

Transformer T_1

$$L_1 = \frac{3600}{49} = 73 \ \mu H$$

$$N_2^2 A = \frac{3600}{6} = 600$$

If a core of .75 sq inch cross sectional area is used

$$N_2 = \sqrt{\frac{600}{.75}} = 28 \text{ turns}$$

$N_1 = 4$ turns

$$\text{Flux Density} = \frac{15 \times 36 \times \sqrt{3600 \times 70}}{4 \times .75}$$

$= 90{,}000$ lines per square inch

With this flux density most of the silicon steel materials will do for the core.

Free-Wheeling Diode D_1

$$\frac{I_m}{4} = \frac{110}{4} = 27.5 \text{ amps}$$

Average Current in SCR_2, D_2, C and L_2

$$I_{AV(SCR_1)} = 250 \ (70 \times 36 + 110 \times 2\sqrt{73 \times 70}) \times 10^{-6}$$

$= 4.6$ amps average

RMS Current in L_1

$$\frac{I_m}{2} = 55 \text{ amps RMS}$$

Voltage Rating of SCR_1, SCR_2, D_1, and C

$$V_{PK(SCR_1)} \leq 36 + 110\sqrt{\frac{73}{70}}$$

$$= 148 \text{ volts}$$

Voltage Rating of D_2

$$V_{PK(D_2)} \leq 7 \times 148$$

$$\approx 1000 \text{ volts}$$

SCR Dynamic Characteristics

SCR_1

$$dv/dt = \frac{110}{70} = 1.6 \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{36}{73} = 0.5 \text{ amps per } \mu s$$

$$t_c = \frac{36 \times 70}{110} = 23 \ \mu s$$

SCR_2

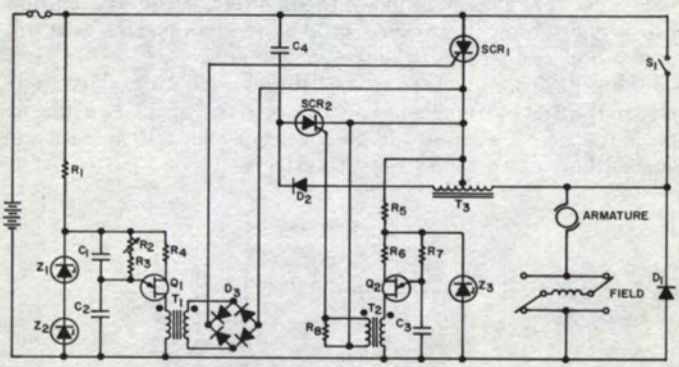
$$dv/dt = \frac{148}{3600 \times 70} = 0.3 \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{148}{\text{Estimated 1 } \mu H}$$

$$= 148 \text{ amps per } \mu s$$

$$t_c = \pi/2 \ 3600 \times 70 = 780 \ \mu s$$

The chosen components are listed in the complete schematic in Figure 9.2.13.



C1—0.1μf, 100V
C2—0.1μf, 100V
C3—0.22μf, 100V
C4—100μf, 115VAC, G-E 28F1103
D1—G-E IN2155
D2—G-E A27P
D3—G-E IN536(4)
Q1—G-E 2N2646
Q2—G-E 2N2647

R1—220Ω, 2W
R2—0 TO 100K POTENTIOMETER (TAPER Z)
R3—20K, 1/2W
R4—330Ω, 1/2W
R5—270Ω, 2W
R6—330Ω, 1/2W
R7—15K, 1/2W
R8—100Ω, 1/2W

SCR1—G-E C55B
SCR2—G-E C35B
T1—PE 2229
T2—PE 2229
T3—G-E 9T45Y7009
Z1—G-E IN1771
Z2—G-E IN1771
Z3—G-E IN1773

Figure 9.2.13 Battery Vehicle Controller Using The Jones Chopper

9.2.3.5 Testing Procedure

The circuit should first be tested with a resistor of 1 ohm in place of the motor. The frequency range and pulse width should be checked. The turn-off time should be measured and should be from 50 to 70 μs.

The 1-ohm resistor should be removed and the motor connected. After the operation has been confirmed, the turn-off time of SCR_1 should be measured with the heaviest load using a fully charged battery. The turn-off time (t_c) must be greater than 20 μs in the worked example.

9.2.3.6 A Note on Motor Plugging

Plugging means throwing the motor in reverse while it is coasting forward. The result is that the motor acts as a generator with the polarity reversed. High values of current flow in the free-wheeling diode and the load resistance seen by SCR_1 is extremely small.

In these circumstances the value of C or alternatively the product $L_1 \times L_2$ must be increased in order to increase the circuit turn-off time.

9.3 INVERTER ACCESSORIES

In practical applications of inverters it is often necessary to modify the design to accommodate one or more of the following requirements:

1. The ability to operate into inductive loads
2. Over-current protection
3. Open-circuit operation
4. Sine wave output
5. Regulated output

9.3.1 The Ability to Operate Into Inductive Loads

When an inverter sees a reactive load as opposed to a purely resistive load several changes occur in the operation of the inverter. Without attention, a reactive load can cause high voltage transients to exist in the inverter resulting in loss of efficiency and power and jeopardizing the components.

Consider Figure 9.3.1. Assume that SCR_1 is conducting. Current is flowing in the primary of the transformer as shown by arrow "a" and in the load by "b". When SCR_1 is turned off, current "b" still needs to flow. If no path were provided in the primary, the voltage would rise excessively.

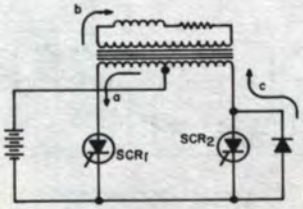


Figure 9.3.1 Flow of Reactive Current

A convenient means of providing a current path is to place a diode across SCR_2. Now current "c" can flow and this is magnetically the same path as current "a". There are disadvantages of using a diode directly across the SCR. The turn-off

time is increased due to the absence of negative bias greater than about 1 volt (Chapter 3). The dv/dt that the circuit applies to the SCR is greatly increased. Figure 9.3.2 shows the effect of a diode across the SCR on the voltage waveform. In Figure 9.3.2(b) it is seen that the voltage across the SCR is held at a low negative value while current is flowing through the diode. When the diode ceases to carry current, the voltage across the SCR suddenly snaps up to a high value. As the rise time is commonly less than 1 μs, the value of dv/dt can be very high. Where possible, it is preferable to avoid placing the diode directly across the SCR. The circuit of Figure 9.2.5 for example shows how an inductor can be used between the SCR and the diode. By this means both the high values of dv/dt and the low amount of reverse voltage can be avoided.

When Class A inverters are operated into inductive loads, detuning of the resonant circuit occurs. If this detuning shortens the turn-off time excessively, the resonant circuit must be retuned.

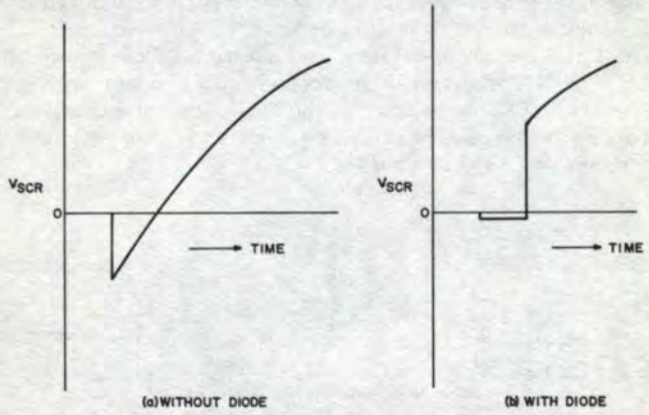


Figure 9.3.2 Voltage Waveform Across the SCR

9.3.2 Overcurrent Protection

If the load current in an inverter is increased beyond the rated output, some means must be provided for the protection of the components. The following methods may be considered.

9.3.2.1 Fuses and Circuit Breakers in the DC Supply

This, the most obvious of steps, has the advantage of simplicity. It is however necessary to match the overload capabilities of the SCR with the current-time rating of the fuses or circuit breakers. Thus the I^2t rating of the SCR must be greater than that of the fuse. This is complicated by the fact that the I^2t rating of the SCR drops substantially during the SCR turn-on time, and fuses or circuit breakers do not afford very good protection in this short time.

Another snag is the location of the fuse in the DC supply. Invariably a ripple current due to the load current flows in the DC supply. Thus the fuse will see a relatively high RMS current and may, in the case of high frequency inverters, have to be derated because of skin effect. If on the other hand a large filter capacitor is placed between the fuse and the inverter to carry the ripple current then the fuse does not isolate the SCR from the energy in the capacitor.

9.3.2.2 Current Limiting by Pulse-Width Control

The inverter components may be protected by sensing the output current and using this information to narrow down the pulse width when the output current exceeds the rated value. With a very heavy load the current pulses then become narrow and have a high amplitude. The circuit is then liable to present short values of turn-off time and high values of di/dt to the SCR. If the load is distributed to more than one piece of apparatus, there may not be enough current in the case of a current limited supply to blow the local fuse where a short circuit occurs.

9.3.2.3 Current Limiting by LC Resonance

The bridge circuit in the output lead of the inverter in Figure 9.3.3 is in series resonance at the output frequency. If the Q of the capacitors and inductors is high, the overall efficiency of the inverter will not be appreciably changed.

In the event of a current overload a fast acting switch is connected between points A and B. The bridge circuit then becomes a parallel resonant circuit at the operating frequency and the impedance to the load current becomes very high.

The fast-acting switch may be either a saturating reactor or one of the forms of SCR AC switches described in Chapter 7.

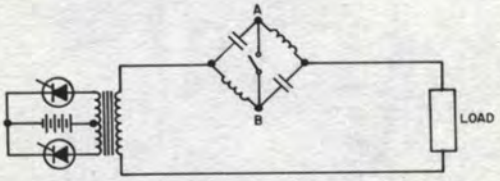


Figure 9.3.3 Current Limiting by L. C. Resonance

9.3.2.4 Current Limiting by Means of Clamping Diodes

In Class A inverters where the load current flows in an inductor it is possible to limit the load current by limiting the voltage across the inductor.

In the circuit of Figure 9.3.4 a secondary winding is coupled to the tapped inductor L. The voltage across this secondary winding is at twice the output frequency. As the load current becomes greater, the voltage across the secondary becomes greater. By suitable choice of turns ratio the diode D_1 will start to conduct current when the load current reaches a predetermined value. This means that the inductor L will see an increase of reflected resistance from the power supply and the output current will be limited.

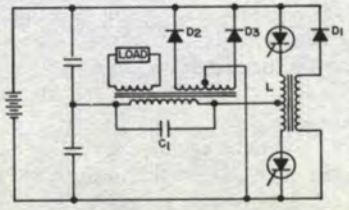


Figure 9.3.4 Current Limiting by Means of Clamping Diodes

9.3.3 Open-Circuit Operation

Class A inverters depend on the resonance of the load for commutation. If the load is lightened, the Q of the circuit may approach zero and the commutation may fail. Measures have to be taken to overcome this limitation. An example is shown in Figure 9.3.4.

A "by-pass capacitor" C_1 is connected across the load so that, when the load is open, the Q remains high although the resonant frequency increases and the output voltage rises rapidly. This rise can be limited by a tertiary winding on the transformer. Diodes D_2 and D_3 at the output carry current to the supply as soon as the voltage across the tertiary winding exceeds the supply voltage.

All other classes of inverters are relatively insensitive to load changes. With a light load, or in the case of a transformer coupled output, with magnetizing current flowing, AC will be present at all times at the output.

9.3.4 Sine-Wave Output[7]

Most applications of DC to AC inverters prefer a sine-wave rather than a square wave output. In conflict with this we are faced with the fact that the SCR is essentially a switch and switching a battery gives square waves. In fact the great efficiency with which SCR inverters operate is mainly due to the fact that the SCR switches at high speed from the fully-off to the fully-on mode.

Sine-wave output-waveforms may be obtained from SCR inverters by the following approaches:

1. Resonating the load
2. Harmonic attenuation by means of an LC filter
3. An LC filter plus optimum pulse-width selection
4. Synthesis by means of output voltage switching
5. Synthesis by control of the relative phase of multiple inverters
6. Multiple pulse width control
7. Selected harmonic reduction
8. Cycloinversion

9.3.4.1 Resonating the Load[1]

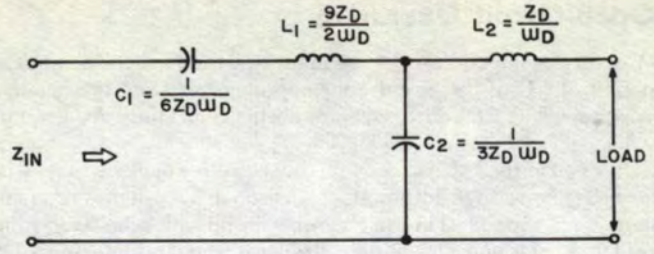
The waveform in the load may be made sinusoidal by inserting the load in a resonant circuit of a Q high enough to achieve the desired harmonic content. A typical circuit using this approach is found in Class A inverters. Owing to the large size of the LC components this circuit only becomes attractive above about 400 cycles.

9.3.4.2 Harmonic Attenuation by Means of an LC Filter[7.1, 7.4]

This filter can take many forms. The most attractive is that by Ott described in Reference 7.4. The circuit is shown in Figure 9.3.5. The Ott filter has the following very desirable characteristics:

1. Good voltage transfer characteristics.
2. Attenuation independent of the load.
3. The input impedance is always capacitive.

For details see the Class C inverter example in Section 9.2.2.



Z_D —— FILTER DESIGN IMPEDANCE
ω —— FILTER DESIGN FREQUENCY

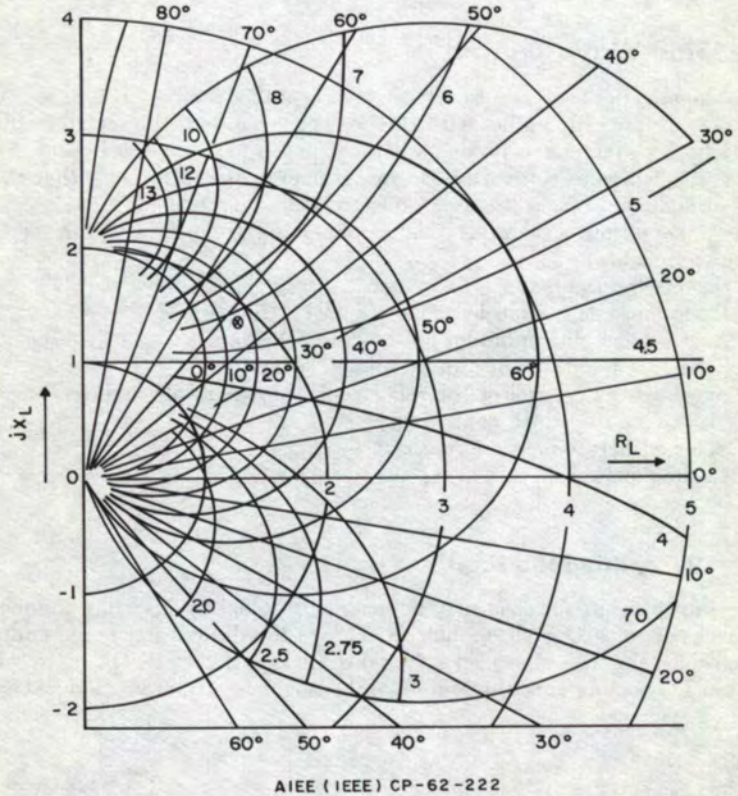


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Figure 9.3.5 Input Impedance Chart

9.3.4.3 An LC Filter Plus Optimum Pulse Width Selection[7.2]

The requirements of the LC filter can be appreciably reduced by using a narrower pulse width than 180°. Thus a 120° pulse has zero third harmonic distortion. See Figure 9.3.6.

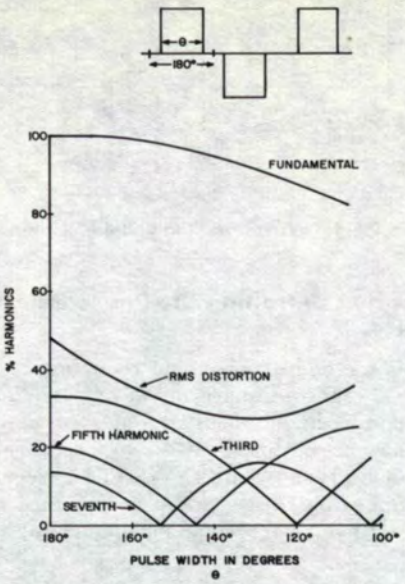

Figure 9.3.6 Harmonic Content Versus Pulse Width with Rectangular Waveforms

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9.3.4.4 Synthesis by Means of Output-Voltage Switching[7.1 and 7.6]

The output from an inverter is coupled through a transformer (Figure 9.3.7) to the load via SCR "tap switches". The appropriate SCR is triggered to give the output waveform shown in Figure 9.3.8. The inverter operates, in this case, at five times the output frequency. This waveform is easily filtered to give a good sine wave output.

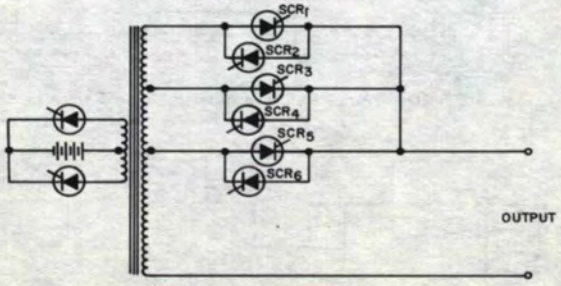


Figure 9.3.7 Output Voltage Switching Circuit

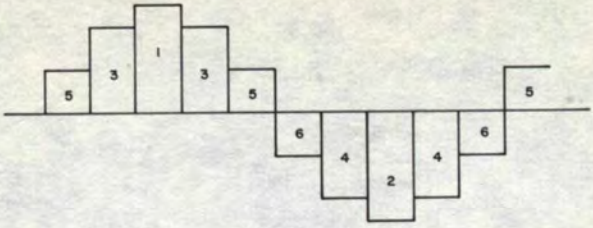


Figure 9.3.8 Waveform with Output Voltage Switching

9.3.4.5 Synthesis by Controlling the Phase Relationship of Multiple Inverters[7.1 and 7.5]

The basis of this method of harmonic reduction is to add the outputs of a multiplicity of inverters to form a quasi sine wave which has no low-order harmonic component. The remaining high-order harmonics are easily filtered.

Figure 9.3.9 shows an outline of a three phase bridge inverter circuit. The voltages across outputs a, b and c are shown in Figure 9.3.10 and the line-to-line voltage across the output transformer is shown in Figure 9.3.11. If more phases are used the steps in the waveform become smaller giving an even lower harmonic content.

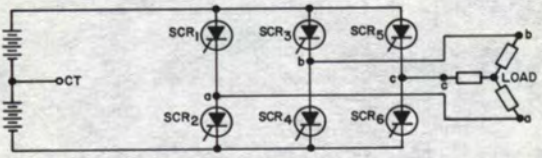


Figure 9.3.9 Three Phase Bridge Inverter Circuit

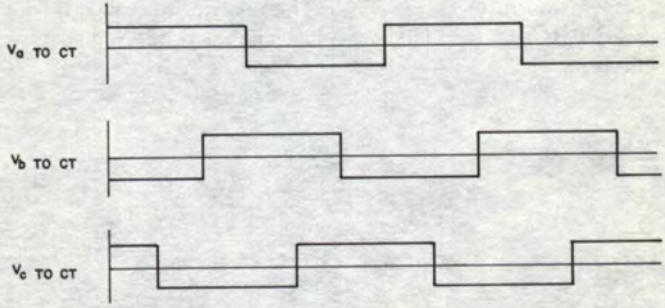


Figure 9.3.10 Phase Relationships in Three Phase Inverter

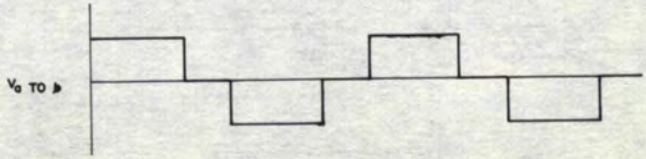


Figure 9.3.11 Output Waveform of Three Phase Inverter

9.3.4.6 Multiple Pulse Width Control[7.1]

This method of achieving a sine wave output is obvious from Figure 9.3.12. This waveform may be obtained from a bridge circuit (Figure 9.1.4). One pair of SCR's is triggered and turned off with various pulse widths to form the positive half cycle and then the other pair is operated similarly for the negative half cycle.

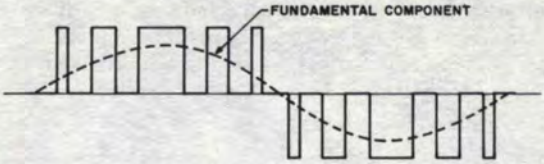


Figure 9.3.12 Output Waveform Using Multiple Pulse Width Control

9.3.4.7 Selected Harmonic Reduction[7.3]

The circuit in Figure 9.1.4 is triggered so as to give a load waveform as shown in Figure 9.3.13. With precise control of the pulse widths the output wave-shape can be made low in 3rd and 5th harmonic content.

The advantages of this method over other methods of synthesis are:

1. The fundamental output may be varied from zero to maximum amplitude without re-introducing the harmonic voltages.
2. A three-phase circuit using only twelve SCR's can eliminate all the harmonics below the eleventh while still being able to control the fundamental frequency from zero to maximum.
3. The triggering circuitry is considerably simplified.

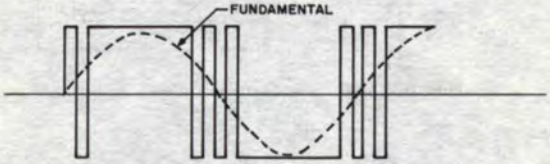


Figure 9.3.13 Output Waveform with Selected Harmonic Reduction

9.3.4.8 The Cycloinverter

A cycloinverter consists of an inverter, operating at about ten times the desired output frequency, to which is coupled a cycloconverter (see Section 9.4.3) producing the desired output frequency waveform and amplitude.

9.3.5 Regulated Output[8.1]

Most inverter customers specify that the inverter output be regulated both for input voltage and load current variations.

The inverter designer has three choices:

1. To regulate the supply voltage to the inverter
2. To regulate within the inverter
3. To regulate the output of the inverter

9.3.5.1 Supply-Voltage Regulation

If the supply is a battery, fuel cells or some other DC supply, then the pre-regulation takes the form of a regulated DC to DC converter, the logic for the DC to DC converter coming from the output of the inverter, Figure 9.3.14.

The DC to DC regulated supply can take many forms. These are discussed in Chapter 10 and in Reference 8. If the inverter supply is from a rectified AC line, then pre-regulation can be achieved by substituting phase controlled SCR's for the rectifier diodes. The logic for the triggering circuits is again supplied from the output of the inverter, Figure 9.3.15. Phase controlled rectifiers are discussed in Chapter 8.

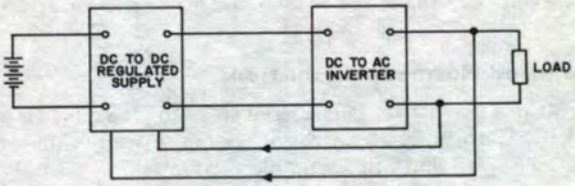


Figure 9.3.14 DC Supply Voltage Regulation

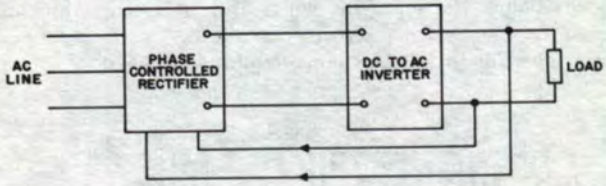


Figure 9.3.15 AC Supply Voltage Regulation

9.3.5.2 Regulation Within the Inverter

By using Class D or Class E inverters pulse-width control is readily achieved. In addition some of the methods of obtaining sine wave output may readily be adapted for output-voltage regulation, the following being the pertinent Sections:

9.3.4.6. Control of the relative phase of multiple inverters
9.3.4.7 Multiple pulse-width control
9.3.4.8 Selected harmonic reduction
9.3.4.9 Cycloinversion

9.3.5.3 Regulation After the Inverter

All the methods commonly used in 60 and 400 cps supplies are applicable to the regulation of the AC output of the inverter. These methods include the use of ferroresonant transformers, buck-boost switching of transformers, phase control of SCR's (Chapter 8), and saturating reactors. References 8.2 and 8.3 describe an excellent means whereby the weight of the saturating reactor may be greatly reduced by means of an SCR "amplifier".

9.4.1 Sequential Inverters[10]

This is a type of inverter that uses a multiplicity of SCR's in conventional circuits. The SCR's are triggered sequentially giving relatively long rest periods between anode-current pulses during which the junctions can cool down, the turn-off time can be long, and a long period is available to reapply forward blocking voltage. The advantage of this system is that SCR's with fairly poor dynamic characteristics may be used in audio frequency inverters or alternatively, high speed SCR's may be used as VLF and LF power generators.

Figure 9.4.1 shows a circuit[10-1] consisting of five sine-wave inverters (Class A). The gates are triggered sequentially 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1, 2, etc. The outputs from the five transformers are paralleled and connected to the load. The anode current through any one SCR is shown in Figure 9.4.2 and the voltage across the SCR is shown in Figure 9.4.3. Note the presence in the voltage waveform of the output voltage from pulses in other SCR's. One of the requirements of this circuit is that the resonant circuit Q be high enough so that the voltage to which each capacitor is charged is greater than the peak voltage across the transformer primary.

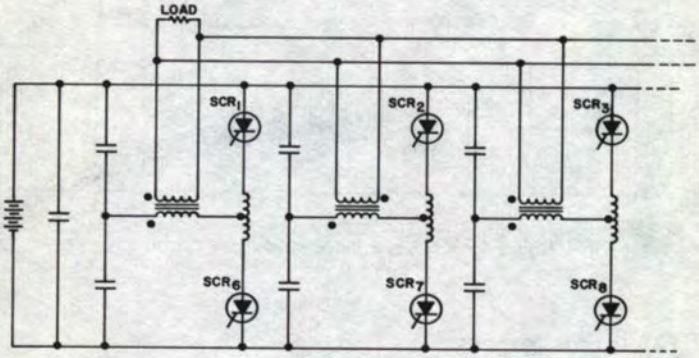


Figure 9.4.1 Sequential Inverter Circuit

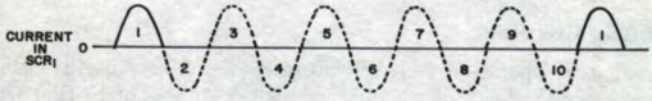


Figure 9.4.2 Current Waveform in SCR_1

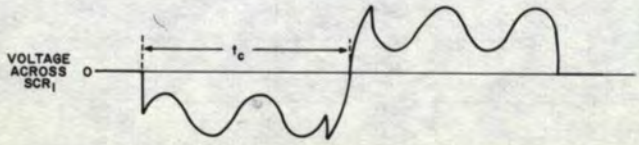


Figure 9.4.3 Voltage Waveform Across SCR_1

9.4.2 Pulse Modulator Switches[9]

The conventional pulse modulator circuit using SCR's as switches operates as a Class A inverter.

The current pulses through the SCR are narrow, ranging typically from .1 μs to 10 μs base width. The repetition rate is from several hundred to several thousand cycles per second.

Turn-off time and dv/dt are usually not critical characteristics of SCR's for this application. The most critical static characteristic is blocking voltage and dynamically, high values of di/dt. The stress of high values of di/dt may be alleviated by using a saturating reactor in series with the SCR.

In order to minimize jitter, and the delay and rise time, the gate of the SCR should be driven as hard as the ratings permit. The rise time of the gate pulse should be much less than 1 microsecond.

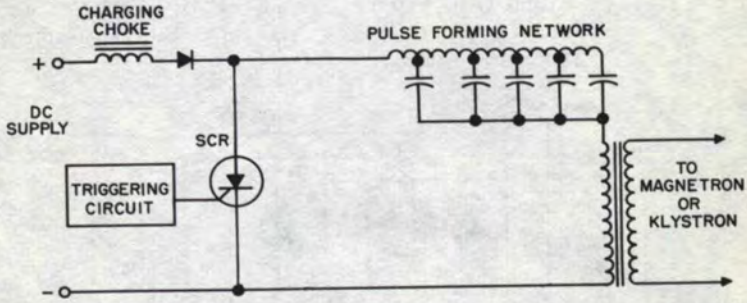


Figure 9.4.4 Basic Pulse Modulator Circuit

9.4.3 Cycloconverters[11]

A cycloconverter is a means of changing the frequency of alternating power using controlled rectifiers which are AC line (Class F) commutated. The cycloconverter is thus an alternative to the frequency changing system using a rectifier followed by an inverter.

9.4.3.1 Basic Circuit

The method of operation is readily understood from Figure 9.4.5. A single-phase full-wave rectifier circuit is equipped with two sets of SCR's, which would

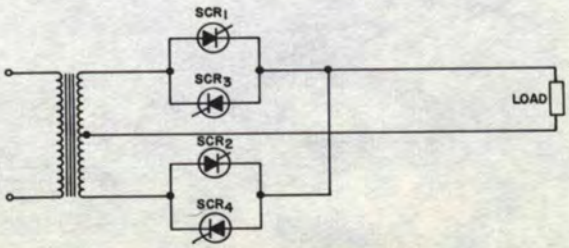


Figure 9.4.5 Single Phase Cycloconverter

give opposite output polarities. Thus if SCR_1 and SCR_2 are triggered the DC output would be in the polarity shown in Figure 9.4.5. If SCR_3 and SCR_4 were triggered instead, the output polarity would be reversed. Thus, by alternately triggering the SCR pairs at a frequency lower than the supply frequency a square wave of current would flow in the load resistor. A filter would be needed to eliminate the ripple.

In order to produce a sine wave output, the triggering of the individual SCR's would have to be delayed by varying degrees so as to produce the waveform shown in Figure 9.4.6.

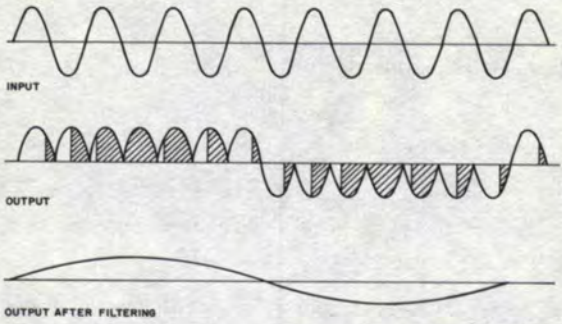


Figure 9.4.6 Single Phase Cycloconverter Waveforms

9.4.3.2 Polyphase Application

The SCR cycloconverter is important in two applications. In the variable-speed, constant-frequency system an alternator is driven by a variable-speed motor such as an aircraft engine, yet the required output must be at a fixed and precise frequency such as 400 cycles per second. A second application is where the required output must be variable in both frequency and amplitude for driving an induction or synchronous motor. This makes possible variable speed brushless motors which could for example be used to drive the wheels of vehicles operating in difficult environments.

Due to the advantages in AC motor design, most of the cycloconverter systems are polyphase. Figure 9.4.7 shows a typical schematic (excluding the trigger circuit).

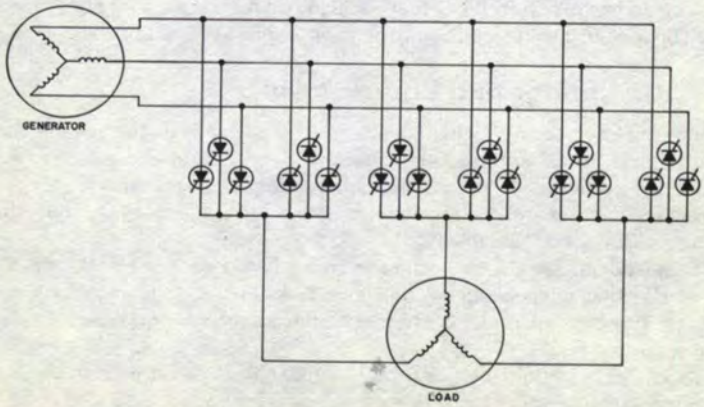


Figure 9.4.7 Three Phase Cycloconverter Circuit

9.4.3.3 Discussion

The pro's and con's of cycloconverters versus rectifier-inverters as frequency changers may be summarized as follows:

CYCLOCONVERTER	RECTIFIER-INVERTER
AC line commutation used	Additional commutation circuit necessary
Regeneration from overhauling loads possible	Regeneration in the rectifier stage not possible
Loads of any power factor may be accommodated	Sensitive to load power factor
Frequency range limited to below ⅓ of generator frequency	Wide frequency range
"Shoot through" of an SCR shuts the system down for less than one cycle provided the resulting current surge is non-destructive to the SCR	"Shoot through" of any one SCR shuts down the whole system
	Readily adapted to run from battery emergency supply
In a three-phase system a minimum of 18 load-carrying SCR's are required	In a three-phase system a minimum of 6 rectifier diodes and 6 load-carrying SCR's are required

9.5 TROUBLESHOOTING SCR INVERTERS

The purpose of this section is to aid the designer in diagnosing and curing poor performance in his inverter. This section also provides a step by step procedure for checking the design to ensure long life and reliable operation of the SCR's.

9.5.1 SCR Ratings and Characteristics

SCR's must be operated within their ratings as given in the specification sheet. Do not design around samples; the sample may well be much better than the type number would indicate. If production quantities are later involved, some SCR's may be received which are, for example, of lower voltage capability than the sample. *Design around the specification sheet.*

Voltage and current measurements must be made on all the SCR's in the prototype. For this purpose an oscilloscope is essential. It should have a rise time of less than 100 nanoseconds in order that the waveforms may be reliably scanned for steep wave fronts.

Measurements should be made under extreme as well as normal load conditions. Include open-circuit operation, momentary overloads, and the first starting cycle.

9.5.2 Voltage Measurement

Make sure that the probe is adjusted to give a flat response. Make sure too that no ground-current loops are present; the rule is that only one ground lead should run from the inverter to the oscilloscope.

9.5.3 Current Measurement

Current measurements are more difficult to make accurately than voltage measurements. No universal instrument is available but satisfactory results are obtained on inverters using a combination of the following types.

Current Probe. This is a clamp-on type of current transformer with the secondary connected to an oscilloscope. An example is the Tecktronix Type P6016 current probe, Figure 9.5.1. When used with an amplifier this probe can handle 15 amperes peak to peak and has a frequency response extending from 50 cps to 20 mc/s. It is especially useful for measuring gate-current pulses as the readings are free from external pick up.

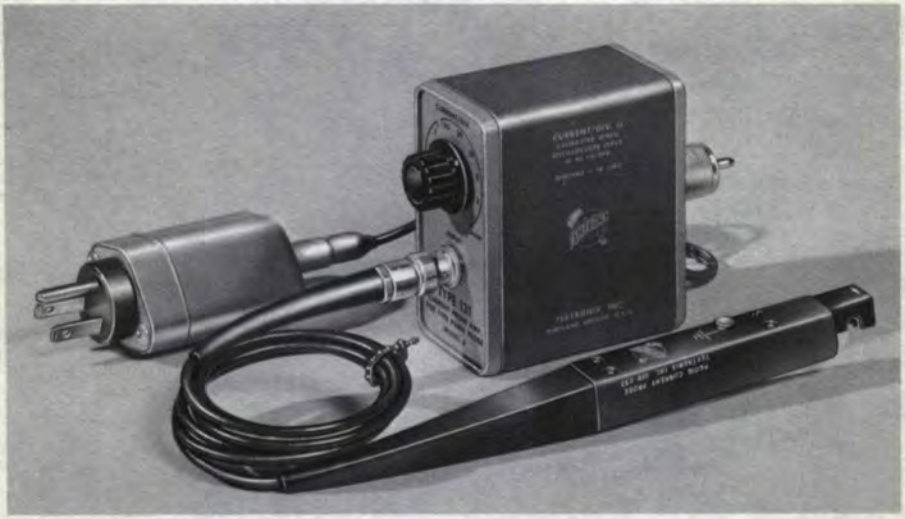


Figure 9.5.1 Current Probe and Amplifier

This type of instrument cannot measure DC and is liable to saturate if the DC component exceeds 0.5 ampere.

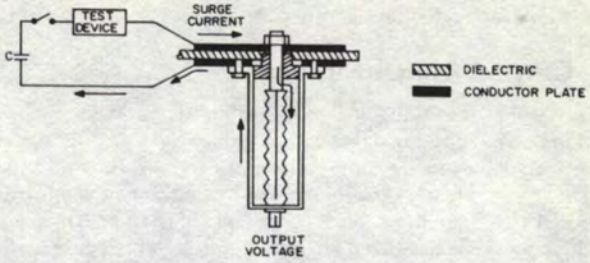
Current Shunt. The current shunt is a non-inductive resistor which is inserted in the circuit. The voltage across this resistor is then observed on an oscilloscope.

An inexpensive form of a current shunt is described in Chapter 18 and construction details are given in Figure 18.9. This shunt can handle about 20 amperes rms and has a usable frequency response from DC to about 1 mc/s.

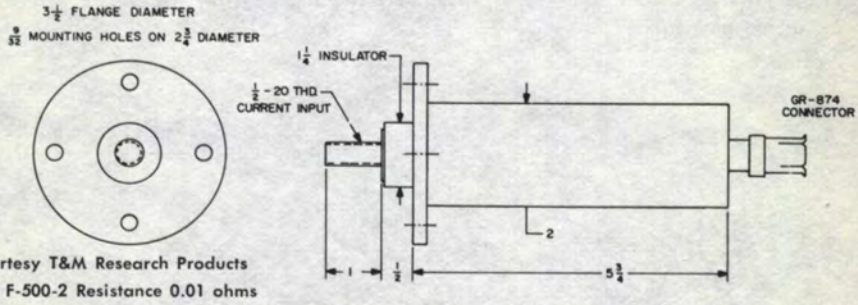
A much more elegant design is shown in Figure 9.5.2. This shunt, made by T & M Research Products, Albuquerque, New Mexico, has a frequency response from DC to 150 mc/s and can carry 60 amperes rms continuously.

The only limitations of this form of current measurement lie in the practical difficulty of inserting the shunt in the circuit and in avoiding false readings due to stray pick up from ground loops.

ELECTRICAL



MECHANICAL



Courtesy T&M Research Products
Type F-500-2 Resistance 0.01 ohms

Figure 9.5.2 Current Shunt

9.5.4 The Anode Circuit

The following anode voltage and current relations should be measured on all the SCR's in the circuit:

Peak forward blocking voltage
Peak reverse voltage
dv/dt
Turn-off time (t_c)
Rate of change of turn-on current (initial di/dt)
Forward current before turn-off
Peak reverse current

Each of these items is specified in the specification sheet. If the SCR is running outside specifications, either choose an SCR of another rating or modify the circuit so as to run the SCR within ratings.

9.5.5 Modifications to Soften dv/dt

Add a series RC network across the SCR. Note that this may, with low values of R, increase the di/dt. The effectiveness of the network may be increased by shunting a diode across the resistor. This increases softening of the dv/dt without worsening the initial di/dt (see Figure 6.3).

9.5.6 Modification to Soften Initial di/dt

The initial di/dt may be limited by means of a saturating reactor connected in series with the SCR. Figure 9.5.3 shows a typical modification. As the core sees a unidirectional current it may be necessary to add secondary windings carrying DC to L_4 and L_5 in order to reset the cores in preparation for the next cycle. The reverse recovery current of the SCR is partially effective in resetting the core. Figure 9.5.4 shows the effect of the saturating reactor in the anode current waveform. Notes on the design of the saturating reactor will be found in Chapter 3.

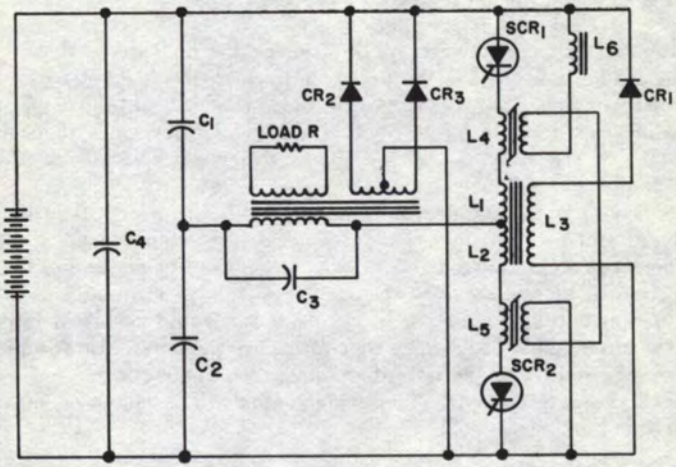


Figure 9.5.3 Class A Inverter with Saturating Reactors

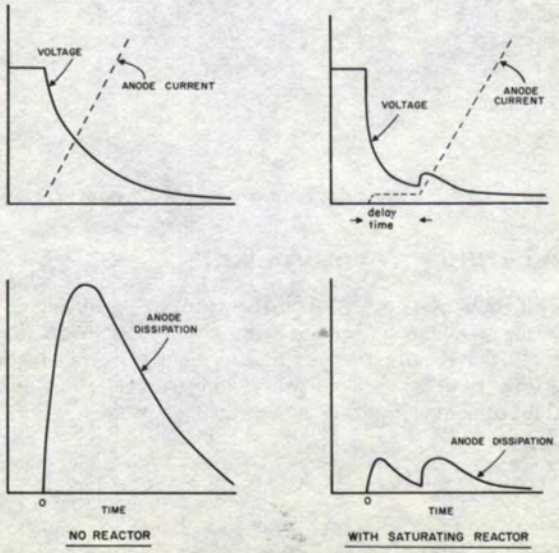


Figure 9.5.4 Effect of a Saturating Reactor on the SCR Waveforms

9.5.7 Gate Circuit

The following gate voltage and current relations should be measured:

Gate voltage before triggering
Peak gate triggering voltage
Pulse width of triggering gate voltage
Gate triggering current
Gate current rise time

From the above data check that the following are within the specified limits:

Peak and average gate power
Peak reverse voltage before triggering
Peak gate triggering voltage

Note that for short trigger pulses the peak gate voltage that will trigger all SCR's has to be increased as the pulse width decreases (Chapter 4).

Remember that a slowly rising gate pulse that will only just trigger an SCR is liable to increase local junction heating. Always trigger an SCR used in inverters with as steep a rise time as possible (preferably shorter than 500 ns) and with as high an amplitude as is permitted.

Negative gate bias voltage may be applied while the SCR is blocking to improve dv/dt and turn-off time. This also negates random triggering.

Where the anode current of an SCR is liable to oscillate due to resonance in the load, it will be necessary to trigger the SCR with a broad pulse. A gate pulse which did not extend to time t_1 in Figure 9.5.5 would result in only the shaded part of the anode current flowing. By continuing the gate pulse to time t_2, the SCR will be retriggered when the circuit again causes anode current to flow.

Check the gate current for spurious signals. The clamp-on current probe is ideal for this purpose.

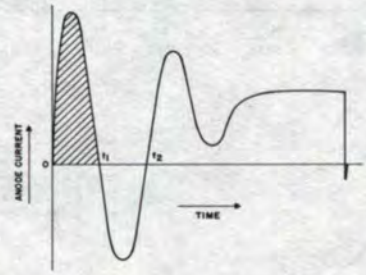


Figure 9.5.5 Typical Oscillatory Anode Current Waveform

9.5.8 Temperature Measurement

The junction temperature of an SCR has a strong influence on its characteristics. It is therefore necessary in checking the SCR's in an inverter to measure the case temperature and estimate the junction temperature. The estimated junction temperature should then be used in prescribing the required SCR characteristics. Methods of calculating the junction temperature are discussed in Chapter 3.

9.5.9 Magnetic Saturation

Iron cored inductors and transformers are liable to saturate and mar the performance of the inverter. There are two cases where untoward saturation is commonly encountered.

1. In the Class A inverter of Figure 9.2.1 the tapped reactor L_1-L_2 carries a DC component of current which must be considered if an iron cored inductor is used.

2. When any inverter is initially triggered, the voltage applied to the iron cored transformer may be in the same polarity as the half cycle before it was previously turned off. The additional magnetomotive force may cause saturation of the core.

Corrective methods include:

(a) Designing the core for operation at reduced flux density.
(b) Controlling the trigger pulses so that the magnetization polarity is always automatically reversed.
(c) Starting at a frequency which is momentarily higher than normal.

9.5.10 Supply Impedance

Check the power supply impedance. This should be low compared with the load impedance seen by the SCR. Remember that the supply has to carry output-frequency current. Electrolytic capacitors are not always suitable for carrying AC superimposed on DC owing to their relatively high loss factor. Oil impregnated paper capacitors are much better.

Avoid having mechanical switches in the line from the supply to the inverter or anywhere in the commutation circuit. Contact bounce is a common cause of trouble.

9.5.11 SCR Inverter Check List

Measure and check the following against the component specifications.

Max. Load	Min. Load	Starting Load	
☐	☐	☐	Peak forward blocking voltage
☐	☐	☐	Peak reverse voltage
☐	☐	☐	Rate of change of turn-on current at the operating frequency
☐	☐	☐	Forward current before turn-off
☐	☐	☐	Average forward current
☐	☐	☐	RMS forward current
☐	☐	☐	Peak reverse current
☐	☐	☐	Maximum gate voltage before triggering
☐	☐	☐	Maximum gate reverse voltage before triggering
☐	☐	☐	Peak gate triggering voltage
☐	☐	☐	Peak gate triggering current
☐	☐	☐	Peak gate power
☐	☐	☐	Average gate power
☐	☐	☐	Gate voltage rise time is less than 1 microsecond
☐	☐	☐	No spurious signals on gates
☐	☐	☐	Gate pulse width suitable for the circuit
☐	☐	☐	No undesired saturation in magnetic cored reactors
☐	☐	☐	No undesired saturation in magnetic cored transformers
☐	☐	☐	Low power supply impedance
☐	☐	☐	No contact bounce effects from mechanical switches
☐	☐	☐	Electrolytic capacitors checked for high AC current
☐	☐	☐	Junction temperature
☐	☐	☐	Operation satisfactory at maximum ambient temperature
☐	☐	☐	Operation satisfactory at minimum ambient temperature

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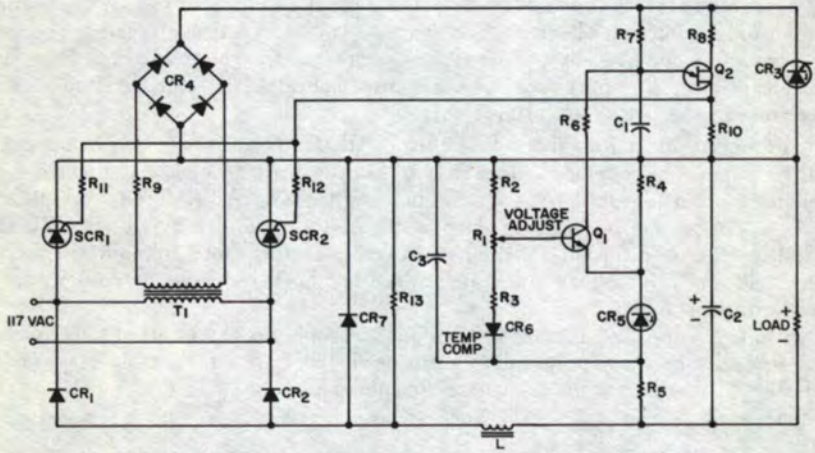
10 DC Regulated Power Supplies

The SCR may be used to regulate DC in two basic modes of operation: (1) As a phase-controlled rectifier, and (2) as a time-ratio controlled chopper. The fundamental principles of both modes are described in Chapters 8 and 9. The SCR regulator may derive its control from output voltage or current, or may be simply manually controlled. Loads which need very low ripple or precise control require the use of some form of filtering. Capacitive filtering is usually preferred at low currents, while inductive filters are better for high currents. Power transistors may be used to provide both dynamic filtering and precise "fine" regulation following an SCR "coarse" regulator. An example of this is given in Chapter 12, following a gate-turn-off switch time-ratio control circuit.

10.1 PHASE-CONTROLLED REGULATED POWER SUPPLY

Figure 10.1 shows a typical phase-controlled constant voltage power supply using the C36H or C35H SCR's.



R_1	10K, LINEAR POT	R_9	3.3K, 2 WATT	CR_3	IN1527
R_2	2.2K, 1/2 WATT	R_{10}	47 OHM, 1/2 WATT	CR_4	IN1692
R_3	10K, 1/2 WATT	R_{11}, R_{12}	250HM, 1/2 WATT	CR_5	IN468
R_4	330, 1 WATT	R_{13}	500 OHM, 5 WATT	CR_6	G-E IN1692
R_5	2.2K, 5 WATT	C_1	0.2 MFD	Q_1	G-E 2N335
R_6	4.7K, 1/2 WATT	C_2	15,000 MFD, 75 VOLT ELECTROLYTIC	Q_2	G-E 2N1671A
R_7	3.3K, 1/2 WATT	C_3	2000 MFD, 15 VOLT ELECTROLYTIC	T_1	117/117V ISOLATION TRANSFORMER 50 MA
R_8	330, 1/2 WATT	SCR_1, SCR_2	G-E C35H OR C36H		
		CR_1, CR_2, CR_7	G-E IN2156	L	10 MH, 20 AMPS

Figure 10.1 50 V, 10 A, Phase Controlled Constant Voltage Power Supply

It is designed to maintain a constant 50 volt DC output as the line voltage and line current vary over a wide range. Rated output is ½ kilowatt, although power

levels up to 1½ KW at this voltage level (using C35H's) are practical with additional filtering. With a 4 to 1 load current change and line voltage variations of ±20% around 117 volts, this circuit will hold output voltage within ±½%.

SCR_1 and SCR_2 are phase-controlled elements in a single phase bridge operating directly from the 117 VAC line. Diode rectifiers CR_1 and CR_2 form the other two legs of the bridge. The two SCR's are fired by gate signals from a common source, UJT Q_2, which operates in a manner similar to that described in Chapter 8. If the feedback circuit through R_6 to the emitter of Q_2 is opened, Q_2 will fire within ten degrees of the beginning of each half cycle of the supply voltage. At this minimum firing angle, the SCR's will deliver maximum voltage to the load.

By means of Q_1 operating in the shunt transistor mode of UJT control, the firing angle can be controlled electrically. The feedback signal to Q_1 is an error voltage developed from comparing a voltage on the base of Q_1 which is proportional to the output voltage, to the reference voltage across breakdown diode CR_5. If the load voltage tries to rise, more base current flows through Q_1. The resultant increase in collector current in Q_1 diverts charging current from C_1 and lengthens the time required to reach the peak point voltage of Q_2. This retards the firing angle and returns the load voltage to normal. If the load voltage starts to drop, the reverse action takes place.

For optimum control of a constant voltage system operating on a single phase supply, the ratio of nominal input AC voltage to the regulated value of DC load voltage should be approximately 2.2. In order for the circuit to operate stably, a large value of filter capacitance C_2 is required across the load. If the ripple voltage across this capacitor becomes greater than approximately 0.1 volt, the circuit has a tendency to hunt from one-half cycle to the next. This can lead to non-symmetrical conduction during the alternate half cycles. At the expense of system response, stability can be achieved by adding capacitance C_3 in the relatively high impedance feedback circuit. For optimum response and stability, all filtering should be incorporated in the main load circuit only.

The variation of forward voltage drop with temperature in CR_6 compensates for the temperature effects on the base to emitter voltage of Q_1. If a germanium transistor is used for Q_1, a 1N91 should be used for CR_6. A "Reference Amplifier," G-E Type RA-1, may be used in place of transistor Q_1 and zener diode CR_5, thus eliminating the need for CR_6. CR_7 acts as a free-wheeling diode to maintain current in the load and filter choke when the SCR's are both blocking. It contributes to overall circuit stability.

A voltage supply of at least 100 volts is desirable for the input of CR_4. Accordingly, when lower AC supply voltages are used, the transformer ratio of T_1 should be chosen so that its secondary voltage is approximately 117 volts.

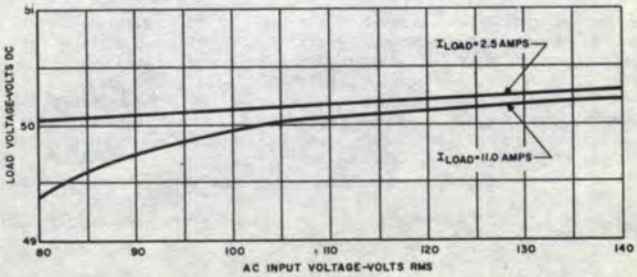


Figure 10.2 Regulation Curves of Constant Voltage Power Supply

The voltage regulating performance of the circuit in Figure 10.1 is shown in Figure 10.2 at two levels of load current. Output ripple voltage with the indicated filter parameters is less than one volt under the worst combination of high input voltage and heaviest load. Additional filtering or the addition of a power transistor stage in series with the load could be expected to improve both the ripple and regulation characteristics if this is necessary. At 10 amperes load and 110 volts AC line input, overall circuit efficiency is 85%.

A simple overcurrent protection scheme for this type of circuit is discussed in Chapter 13.

10.2 CHOPPER-CONTROLLED REGULATED POWER SUPPLY

Figure 10.3 shows the circuit of a power supply based on the Morgan chopper arrangement. (Also see Chapter 5.)

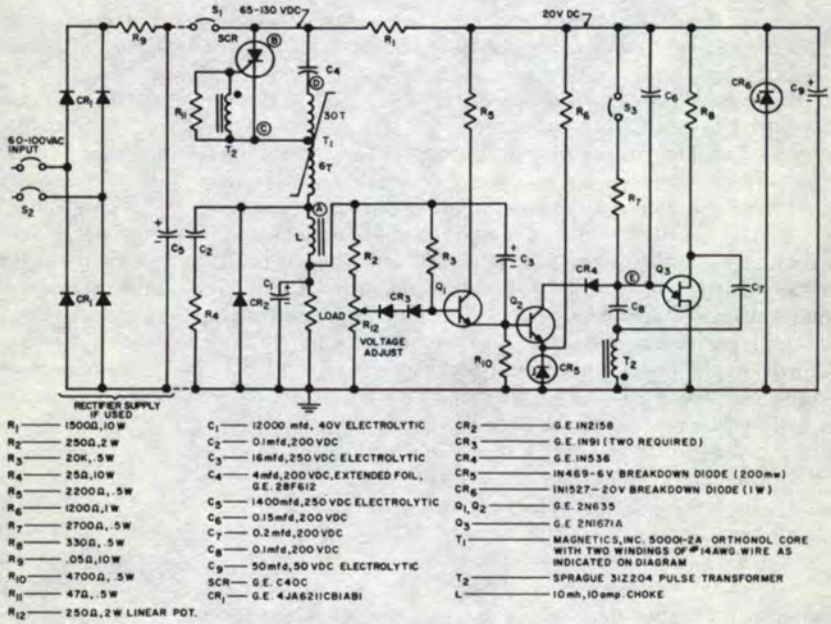


Figure 10.3 28 VDC 10 Amp Regulated Power Supply

It is capable of operating directly from a DC line, or from an AC supply through use of a rectifier and rough filter as shown on the left hand side of the diagram. This circuit has several advantages over the AC phase controlled circuit discussed previously in addition to being able to operate from a DC source. It is capable of operating stably over a wide range of frequency of the AC input. Because the chopping circuit operates in the 500 to 2000 cps range, this circuit also has inherently faster response than a phase-controlled circuit operating at normal line frequencies. Filter requirements are less, and the AC supply sees essentially a unity power factor load with little distortion effects on the line voltage as compared to phase-controlled circuits.

Basic operation of this circuit is as follows: An SCR is connected across the DC bus in series with the load, a saturating current transformer T_1, and filter choke

L. The SCR acts as a switch in series with the load, applying pulses of approximately constant width to the load. The repetition rate of these pulses is controlled by the feedback circuit on the right hand side of the diagram and thus regulates the average voltage being applied to the load. Choke L, in conjunction with capacitor C_1 and free-wheeling diode CR_2, filters the pulses so that essentially pure DC current flows through the load. Since the power control device (SCR) is operating in a switching mode, this is basically a "lossless" method of regulating power although some losses do exist, namely the forward conduction drop through SCR and the filter choke, and switching and control losses. Efficiency is inherently high compared to variable resistance techniques using tubes or transistors in series with the load.

The switching action of the SCR in the Morgan circuit is discussed in Chapter 5. When the SCR is fired by a gate pulse from T_2, power is delivered to the load, and the bottom plate of C_4 is charged positive with respect to its top plate by the auto-transformer action of T_1. When T_1 saturates, the voltage on C_4 is applied to the SCR in the inverse direction, reverse biasing it for a period of time dependent on the load current and the value of C_4. This interrupts the flow of current from the DC supply until the SCR is again triggered. In the interim, however, current continues to flow in the load through CR_2 due to the inductive effect of choke L and the energy stored in C_1.

Waveshapes across the major elements in the power circuit are shown in Figure 10.4 at a DC bus voltage of 90 volts and an average load current of 1.4 amperes. The time interval t_0 indicated on the voltage waveform across the SCR is the turn-off time. Under no circumstances must this time interval become less than 12 microseconds or so-called "shoot-through" may result. "Shoot-through" occurs when an SCR is not reverse biased for a sufficient time to recover its forward blocking ability after having conducted load current. In this event SCR will remain turned on, since T_1 will not be reset and C_4 will not build up a negative commutating voltage. The SCR will remain on indefinitely, thereby applying the full supply voltage to the load. By using the component values indicated in Figure 10.3, an ample safety factor in turn-off time is available up to 10 amperes load current and under all likely load variations and switching conditions. Overcurrent protection schemes of the type described in Chapter 13 can be incorporated if there is a possibility of short circuits or overloads.

The feedback control of the output voltage relies on a UJT relaxation oscillator Q_3 to develop firing pulses for the gate of SCR. These pulses are coupled to the gate through T_2, the primary of which is in series with the emitter capacitor C_8 of the UJT oscillator. With the voltage adjust pot, R_{12}, at its bottom position, no feedback signal is present. Under these conditions, the UJT oscillates at its maximum rate, approximately 2 Kc per second, and maximum voltage is applied to the load. As the arm of R_{12} is moved up so that its portion of the load voltage exceeds the reference voltage of CR_5, transistors Q_1 and Q_2 will start to conduct and part of the current flowing down through R_7 is then diverted from C_8 through CR_4 and the collector of Q_2. C_8 then takes longer to charge to the peak point voltage of Q_3, and the repetition rate of the UJT oscillator and SCR decreases. Load voltage is thereby decreased also. For a given setting of R_{12} so that the load voltage is at or near the design objective of 28 volts, the feedback circuit will regulate the repetition rate so as to maintain load voltage constant with variations in supply voltage and load current.

The control circuit derives its 20 volt supply from the main DC supply through dropping resistor R_1 and breakdown diode CR_6. C_3 transmits a supplementary feedback signal which is a function of the rate of change of load voltage. This signal stabilizes the overall performance and increases the speed of response. It also reduces the supply frequency ripple content of the voltage across the load.

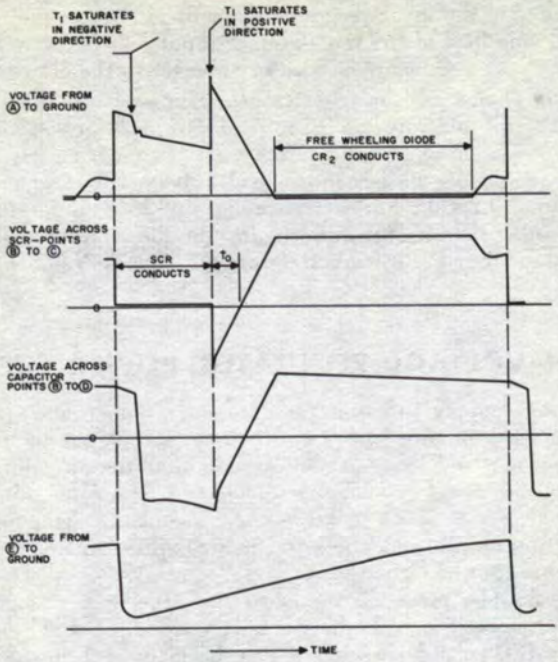


Figure 10.4 Voltage Waveforms in Regulated Power Supply

The two diodes, CR_3, compensate for temperature variations in the base to emitter voltage drop of Q_1 and Q_2. If silicon transistors are used instead of germanium for Q_1 and Q_2, CR_3 should consist of two 1N1692 diodes. If a reference amplifier (RA-1) is used in place of Q_2 and CR_5, CR_3 may be reduced to one diode.

R_9 is a surge resistor designed to protect CR_1 against excessive inrush current to C_5 when the AC line switch is closed. If an equivalent impedance already exists in the AC line, this resistor can be omitted. Starting and stopping of the circuit can be accomplished either by operating switch S_1, S_2, or S_3.

Regulation performance of this circuit is indicated in Figure 10.5. Output voltage is maintained within ±1% with a 7 to 1 load current change and input voltage variation from 60 to 100 VAC. Maximum ripple voltage across the load over this range was 70 millivolts RMS. With 70v RMS input and a load of 10

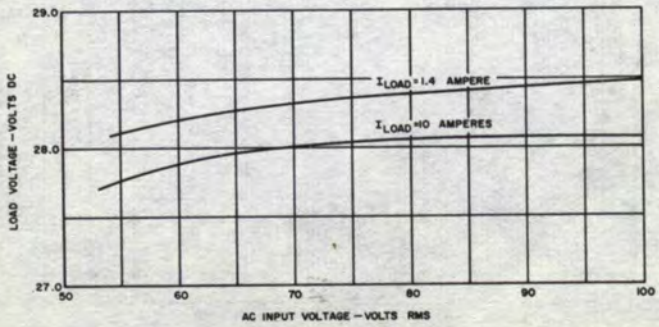


Figure 10.5 DC Voltage Regulator Performance

amps, the efficiency of the inverter (including control but not the rectifier supply) was 86%. At 1.4 amp load at the same voltage input, efficiency was 61%. Overall performance on a pure DC bus was equal or superior to the above figures.

On an abrupt change of load from 1.4 to 10 amperes, the load voltage dipped approximately 0.2 volt and returned to normal within 20 milliseconds. An abrupt drop from 10 to 1.4 amperes caused an overshoot of approximately 1 volt and a return to normal within 50 milliseconds. Load voltage variation over a two-hour period was less than 0.2 volt. All tests were made at 25°C. Reference 4 at the end of this chapter will prove useful in designing the filter required to meet specific ripple requirements across the load. Reference 2 covers design of the saturable transformer T_1.

10.3 HIGH VOLTAGE REGULATED POWER SUPPLY

Another power supply utilizing the Morgan chopper and quite similar to Figure 10.3 is shown in Figure 10.6. Here the load is replaced by the primary of a step-up transformer and since it is desirable that the transformer "ring" in order to reset itself, the free-wheeling diode and associated filter components have been omitted. Series diode D_3 keeps the transformer "ringing" voltages out of the commutating circuit and choke L_2 insures successful commutation under heavy or shorted output conditions.

A half-wave doubler circuit is used to rectify the high voltage in order that both polarities of voltage across the secondary are loaded. Filtering is accomplished by the 3 MFD capacitor which is also the main load on the supply. A portion of the output voltage is selected by a voltage divider and fed to the input of the feedback regulator, emitter follower Q_1. It is then compared to zener D_1, amplified by Q_2, and used to vary the UJT frequency in the shunt mode.

Transistor Q_4 provides constant current charging of the UJT timing capacitor.

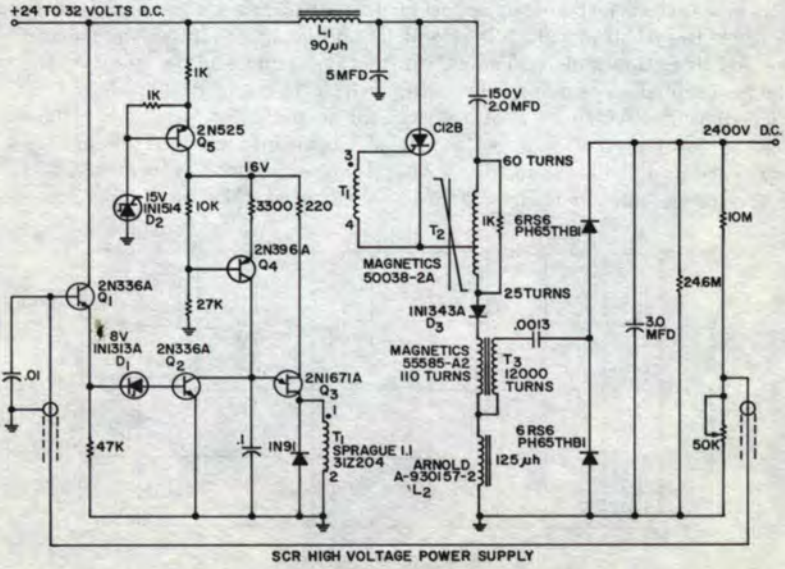


Figure 10.6 SCR High Voltage Power Supply

This insures a linear sawtooth of voltage across the capacitor and hence better noise immunity when the UJT frequency needs to be varied over a very wide range. Otherwise at low frequencies the capacitor would be charged to very nearly the UJT firing voltage for relatively long periods of time and any noise or hum could cause "jitter" in the repetition rate. In most supplies, the required frequency change is small enough that Q_4 can be replaced by a resistor.

A "lock-out" circuit is provided by transistor Q_5. Whenever the main B+ drops to too low a value to insure commutation of the SCR, Q_5 will withhold voltage from the UJT trigger circuit and the SCR will not be fired. This precaution is necessary only when the DC supply is apt to vary over an unusually wide range, or when the DC is turned on at zero volts and slowly increased to the operating range. On a nominal 28 volt system, commutation was successful down to 14 volts, so in the usual case a lock-out circuit for low voltage is not required. The regulated 16 volt supply generated by Q_5 is not necessary for proper operation of the trigger circuit.

Choke L_1 and the adjacent .5 MFD capacitor suppress RF energy from being conducted back into the DC supply. As shown, the supply will readily exceed the requirements of MIL-I-6181B. Interference and its suppression in SCR circuits is further discussed in Chapter 15.

Temperature compensation is readily attained as the switching action of the SCR is inherently quite stable. "On" time of the chopper power pulse is a function of the commutating transformer, commutating capacitor, and the load. None of these components is particularly temperature sensitive, with the result that "on" time is fairly constant with temperature. Repetition rate, or frequency, is determined by the regulator except during the initial charging of the 3 MFD capacitor when the UJT runs at a maximum frequency determined by the timing R and C. By using stable R and C in the emitter timing circuit and proper selection of R_2 in base 2 (General Electric Transistor Manual, 5th Ed., page 141) maximum frequency can easily be held constant over the temperature range. A frequency of 2 to 3 KC is usually satisfactory for the maximum rate.

Approximately 2 seconds after turn on, the output is up to the design value of 2400 volts and the SCR firing rate is reduced from 2 KC to less than 100 cycles. The magnitude of the output voltage and its temperature characteristics are dependent on only a very few components, namely the voltage divider, the emitter base diodes of Q_1 and Q_2 and zener diodes D_1. Q_1, Q_2 and D_1 are directly in series and may be self compensated as follows: Q_1 and Q_2 input diodes will each change a negative 2 mV/°C for a total of 4 mV/°C, while D_1 will change a positive 4 mV/°C. The temperature coefficient of a zener diode is a strong function of its zener voltage; below 6 volts it is negative, above 6 volts it is positive. Since all changes in the amplifier are linear, compensation will track over the temperature range. The voltage divider must provide a constant ratio as temperature varies. Compensation of the divider can take many forms:

1. Break up the 10 meg resistor into several smaller resistors which have temperature coefficients more nearly equal to the potentiometer.
2. Addition of various series, parallel combinations of thermistors.
3. Use of a higher voltage zener at D_1 to "tilt" the amplifier characteristic opposite to the divider characteristic.

Voltage and current waveshapes at various points in the circuit are shown in Figure 10.7 and performance curves vs. temperature are shown in Figures 10.8–10.10. Output voltage regulation vs. input voltage (curve not shown) exhibited no discernible change over a range of 20 to 38 volts. While not directly measured, the over-all system was observed to have fast transient response with no tendency to overshoot, undershoot, hunt or oscillate. See also Reference 2.

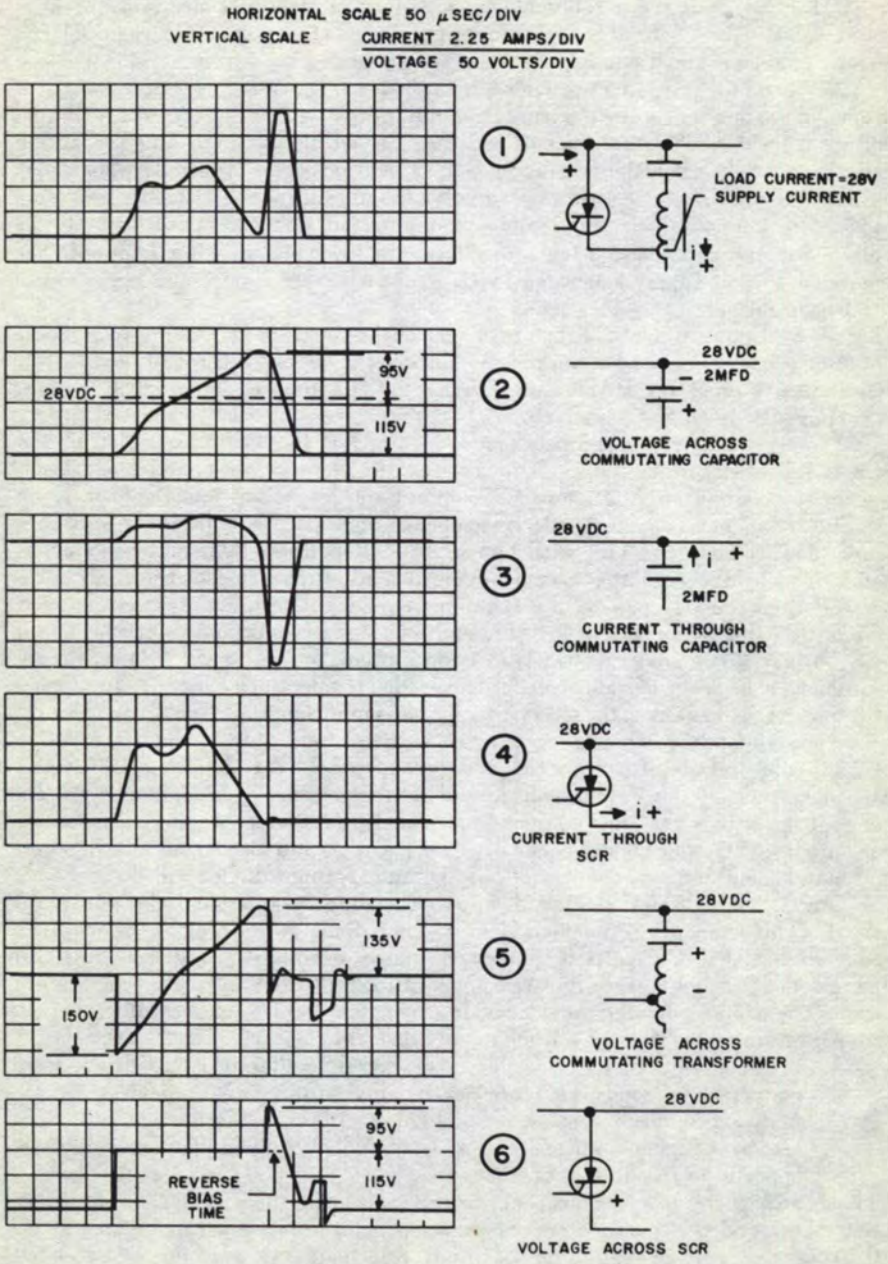


Figure 10.7 Oscillograms

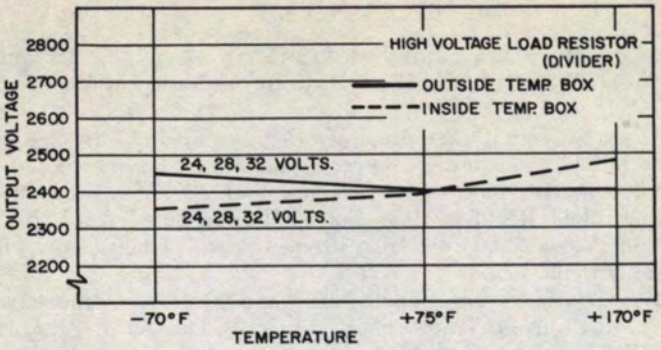


Figure 10.8 Output Voltage High Voltage Load Resistor (Divider)

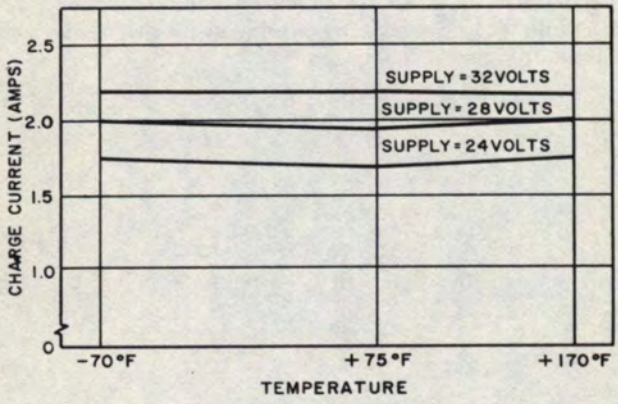


Figure 10.9 Charge Current (Amps)

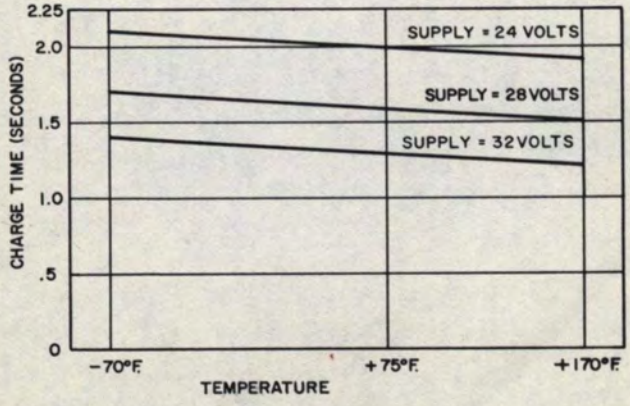


Figure 10.10 Charge Time (Seconds)

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1. "An All-Solid-State Phase Controlled Rectifier System," F. W. Gutzwiller, AIEE Paper CP 59-217, American Institute of Electrical Engineers, New York, N. Y., 1959.
2. Morgan, R. E., "A New Power Amplifier Using a Single Controlled Rectifier and a Saturable Transformer," AIEE, Conference Paper #60-410 (copies available from AIEE, 33 W. 39th St., New York 18, N. Y.).
3. "Silicon Controlled Rectifier High Voltage Power Supply," G. E. Snyder, Application Note 200.6, available from General Electric Co., Rectifier Components Dept., Auburn, N. Y.
4. "30V 10A Regulated Power Supply using the Variable Output Transistor Oscillator with Current Transformer," Stuart P. Jackson, AIEE Conference Paper 61-717, available from AIEE, New York, N. Y.
5. "Regulated Battery Chargers Using the SCR," D. R. Grafham, Application Note 200.33, available from General Electric Co., Rectifier Components Dept., Auburn, N. Y.
6. "Integrated Reference Amplifier for Precision Power Supplies," T. P. Sylvan, Application Note 90.15 available from General Electric Coil, Semiconductor Products Dept., Syracuse, N. Y.

Light Sensitive Applications

The use of light as a means of transfer from mechanical information to electrical signal has been well established in past photoelectric control work. More recent additions to the family of photoelectric sensors is now expanding this field and is opening a new field in which light is used as a signal-processing stage.

11.1 LIGHT ACTIVATED SCR (LASCR)

The General Electric Light Activated SCR's (LASCR), types L8 and L9 (formerly developmental type ZJ227), are small Silicon Controlled Rectifiers*, similar to the C5 type, with a glass window to permit triggering by means of light (see Figure 11.1) as well as by the normal gate signal. Rated for 440 mA DC at 25°C ambient; these units are available in voltage grades from 25 volts to 200 volts. The L8 differs from the L9 only in the *amount* of incident radiant energy (light) required to initiate switching. Types L811 and L911 are the same as L8 and L9 except that the added base increases the current rating to 770 mA DC at 25°C ambient. When mounted on a heatsink, the rating can be increased to 1.6 amperes DC for case temperatures below 75°C. Being high speed power switches, either type can actuate directly solenoids, contactors, motors, lamps and similar 120 volt AC loads, far beyond the capability of previous light-activated components. Latching properties in DC circuits also give the LASCR an inbuilt "memory" which can be an extremely useful feature in opto-electrical logic circuitry. Note also that complete electrical isolation between output and input provides the LASCR advantages over other types of PNPN switches.

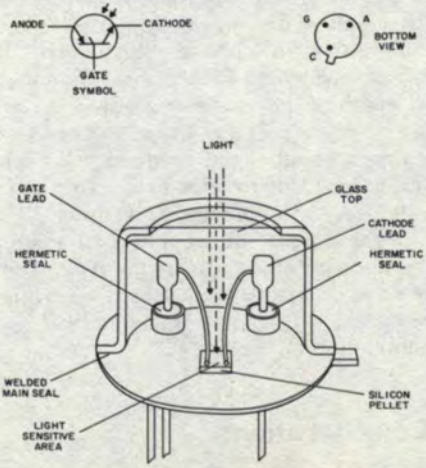


Figure 11.1 L8, L9, Light Activated SCR

* For a complete discussion of the LASCR, including circuits, optics and radiometric design procedure, write for Application Note 200.34, "The Light Activated SCR."

value. The LASCR responds to a much greater range of wavelengths than the eye, extending slightly into the ultraviolet region but primarily in the near infrared region. Since response is down to 50% at 1.09 and 0.76 microns, twice the power is required for switching at these wavelengths as at 1.0 microns.

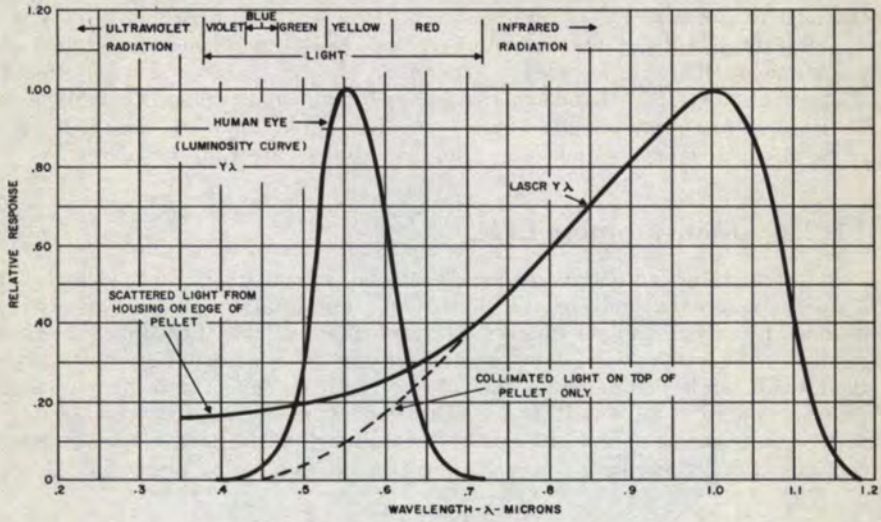


Figure 11.2 Relative Response Curves

Most light sources emit radiation outside the visible region. Since photometric measurements are concerned only with visual effects, such measurements *do not* indicate directly the effect upon silicon except when correlated with the total spectral output of the source. Therefore, if a particular LASCR triggers at 500 footcandles (visible) from a tungsten lamp operating at 2800°K color temperature, the triggering level will be some different number of footcandles from any other type of lamp, or even from the same lamp operating at a different color temperature.

11.2.3 Effective Irradiance

In order to accurately specify and use the LASCR, radiometric units are required and these must be weighed according to the response curve of the device. This is the "Effective Irradiance," H_E, which is expressed in terms of flux density, watts per square centimeter, falling on the receiving surface.

Consider a LASCR which required an "effective-irradiance-to-trigger" H_{ET} = .0075 watts/cm² = 7.5 mw/cm². If very narrow band radiation at 1.0 microns (such as from a LASER) is directed on the pellet, a flux density of 7.5 mw/cm² will cause the device to trigger. If the wavelength is shifted to 1.09 microns (response down to 50%), the triggering flux density will be $\frac{7.5}{0.5} = 15$ mw/cm². Now suppose we supply 5 mw/cm² at 1.0 microns, then 2.5 mw/cm² additional energy will be required to trigger. This can be obtained by supplying 5 mw/cm² at 1.09 microns, because effective energy is additive.

For broad-band radiation, with a spectral distribution of energy H_λ, the total effective energy may be found by breaking up the wide band into many narrow bands, then multiplying the energy in each narrow band by the relative response.

Y_λ, in that band, and adding the resulting incremental effective energies together.

$$H_E = \text{Total Effective Irradiance} = \int Y_\lambda H_\lambda \, d\lambda \qquad (11.2.1)$$

This same method is used to evaluate the effective energy of "light," in which the relative response Yλ is the "luminosity curve" of Figure 11.2.

Equation 11.2.1 shows that energy lying outside the response band does not contribute to the effective energy. Therefore, the relationship between effective energy for the eye (light) and effective energy for silicon depends entirely upon the distribution of energy produced by a particular source. Likewise, the relationship between effective energy and total energy is also dependent on the source.

11.2.4 Measurement of H_E

Although there are several ways to calculate effective irradiance* based upon lamp characteristics and physical dimensions, the accuracy of such calculations depends heavily upon data which is not generally available. Certainly the easiest method of determination of effective irradiance is to measure it. Fortunately, the LASCR can be calibrated for current vs. H_E when connected in the p-n-p mode (see Section 11.4) to permit direct measurement of H_E simply by connecting a battery, microammeter and calibrated LASCR in series. The ZJ227UX4 is a factory calibrated LASCR available for evaluation of lamps and optical designs.

11.2.5 Variations of H_{ET}

Since the total light-generated current in the LASCR is very low, the triggering level of these devices is much lower than normal SCR's. As a result, the light activated units exhibit greater sensitivity to operating conditions. The effective irradiance to trigger (H_{ET}) is reduced by increasing anode voltage, increasing junction temperature, increasing the rate-of-change of anode voltage, and by increasing either gate-to-cathode resistance or externally supplied gate current. Therefore, these devices should not be used as threshold detectors for light if accuracy is required. Stability is improved by holding temperatures, load currents, and voltages constant and well below maximum ratings.

11.2.6 Light Sources

Tungsten lamps are very well suited for operating the LASCR. With proper choice of lamp and proper de-rating, excellent life and reliability can be achieved. For example, operating a tungsten lamp at ½ its normal voltage extends its life about 10,000 times its nominal value. This drop in voltage reduces the effective radiation to about 20% of normal, hence one must start with a higher-power lamp, but this is advantageous because it means a more rugged filament.

Sources suitable for pulsed triggering, hence useful for AC phase-control or long-distance work, are the xenon flash lamps. These lamps have very high peak output intensities and are a reasonably good spectral match to silicon.

Gallium arsenide injection luminescent diodes, operating in either the LASER or the non-coherent mode, are excellent sources for pulse triggering and will probably soon be useful for continuous work. The spectral match is virtually

* See Application Note 200.34 for details of calculations of irradiance.

perfect, hence very high radiant efficiency is obtained. These diodes operate at low voltage and can easily produce 1 microsecond pulses of radiation. Since no visible radiation is produced, they are very well suited for systems requiring visual security.

11.2.7 Optics

Innumerable lenses and reflectors are available which can increase irradiance on the LASCR, but always at the expense of restricting the "angle-of-view." The maximum irradiance which can be obtained with optical systems is limited to the emittance of the source.

Fiber optics provide the best coupling between a source and a LASCR, and can be used to couple several sources and several LASCR units in a complex matrix pattern for logic operations.

11.3 APPLICATIONS OF LASCR

11.3.1 Relay Replacement

The LASCR, basically, is a semiconductor analog of the electromechanical relay. When so used, the device has all the well-known solid state virtues of small

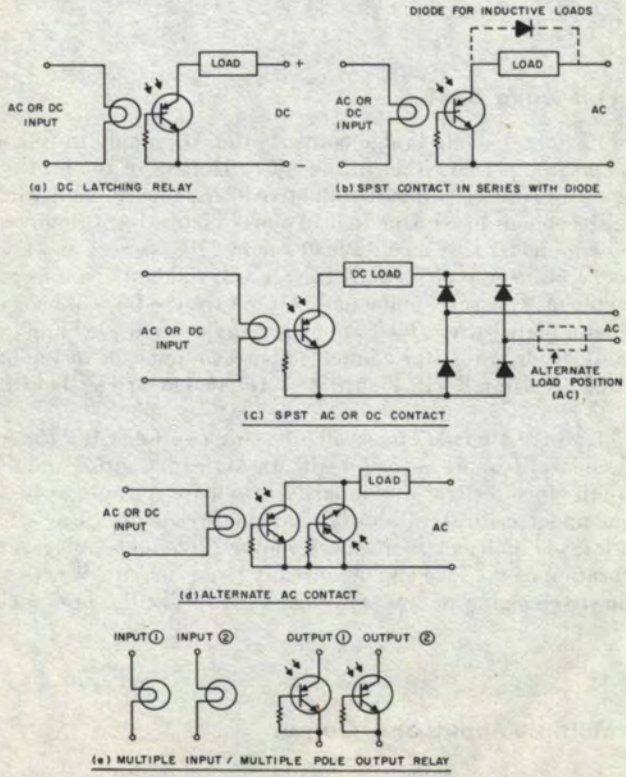


Figure 11.3 LASCR "Relay" Configurations

size, completely static operation (freedom from contact "bounce," etc.), microsecond response, ruggedness and long life PLUS the unique feature of complete electrical isolation between input and output. Figure 11.3 depicts some basic LASCR "relay" configurations and lists their major characteristics.

11.3.1.1 Latching

Figure 11.3 (a): With input (lamp) unenergized the LASCR is equivalent to an open SPST contact, rated at 200 volts peak and 440 mA DC (25°C). When the input is energized, the LASCR will switch, latch and deliver power to the load; the input may then be de-energized. The circuit must be reset externally (beware of dv/dt).

11.3.1.2 Half-wave SPST

Figure 11.3 (b): The same circuit as (a) with an AC supply to the LASCR. Here, the equivalent circuit is a SPST contact in series with a silicon rectifier. The circuit is non-latching on AC since the LASCR is reset each cycle by the reversing supply voltage. Note the use of a free wheeling diode across inductive loads—this diode allows stored coil energy to circulate current through the load while the LASCR blocks negative half cycles of the supply; relay or solenoid "chatter" is thus eliminated.

11.3.1.3 Full-wave SPST

Figure 11.3 (c): A diode bridge converts the AC supply to full wave rectified DC. The load may be placed either in the AC or DC legs of the bridge. Care should be taken when using this circuit with inductive loads, since difficulty in LASCR commutation may be encountered. Due to load power factor, LASCR current and supply voltage are not coincidentally zero. As load current goes to zero and the LASCR tries to commutate, a finite step of forward voltage will suddenly be impressed across it. This voltage step may possess sufficient dv/dt to turn the LASCR back on again. The effect can be eliminated with *DC loads* by placing a "free wheeling" diode around the load. On AC loads, a resistor connected between one side of the bridge and one side of the line (resistor R4 in Figure 11.7 for instance) can help this condition somewhat.

Figure 11.3 (d): Alternate form of (c) using two LASCR's for full wave control. Remarks on dv/dt apply as for (c) with an AC load. Caution should be observed with this circuit since a slight dissimilarity in sensitivity to light between the two LASCR's can, under critical, or slowly changing irradiation, cause half-wave conduction. With loads such as transformers, motors, solenoids, relays, etc., this could result in saturation of the load and abnormally large current. Where such loads are used with slowly-changing or limited-range light levels, the bridge circuit is preferable.

11.3.1.4 Multiple Input and Output

Figure 11.3 (e): Illustrates the possibilities of multiple input/multiple pole output combinations.

11.3.2 LASCR as SCR Driver

The power handling ability of any of these relay arrangements may be increased, as desired, by using the LASCR as a gate amplifier to trigger a larger SCR (Figure 11.4 a). Repositioning the LASCR with respect to the driven SCR (Figure 11.4 b) converts the circuit into the equivalent of a normally closed contact, a useful configuration in many monitoring and alarm circuits requiring load current flow in the *absence* of light.

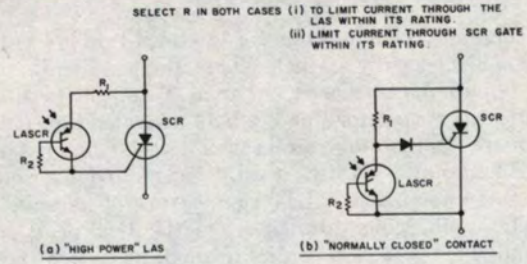


Figure 11.4 LASCR/SCR Combinations

11.3.3 Opto-Electrical Logic Using the LASCR

The unique binary nature of the LASCR makes it an ideal element for use in opto-electronic logic circuitry. Figure 11.5 illustrates a selection of the more common types of logic functions, as performed by the LASCR.

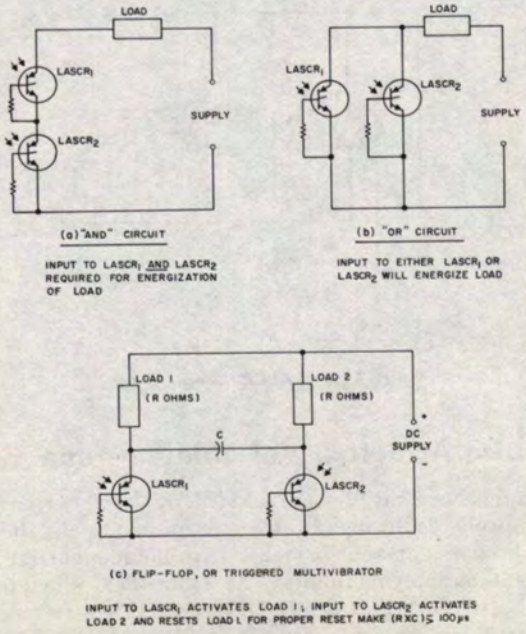


Figure 11.5 Logic Operations With The LASCR

The circuit of Figure 11.5 (c) is of particular importance in working with DC control circuits. Variations of the basic flip-flop circuit are numerous because the loads do not have to be equal and an SCR can be used in one leg for handling large loads.

11.3.5 Variable Pulse-Width LASCR "Single Shot" (Counting or Delay Circuit)

Simple and economical commutation for the LASCR in low voltage DC circuits can often be accomplished with a single "bootstrapped" unijunction transistor, Figure 11.6. The circuit may be used either as a pulser (by differentiating the square wave output with a capacitor), or as a light activated time delay (by "stretching" the output square wave up to several seconds with suitable UJT constants).

With light incident on the LASCR, it will trigger and deliver power to the load. The load voltage now energizes the UJT timing/turn-off circuit. While the UJT emitter capacitor C_1 is charging through R_1 to the UJT peak point voltage, C_2 charges rapidly to the load voltage potential through R_3. When the UJT eventually "fires"—determined by ($R_1 \times C_1$) and the UJT constants—the output pulse from R_4 is coupled through C_2 and CR_1 to the LASCR cathode, raising cathode potential above supply voltage long enough for the LASCR to commutate.

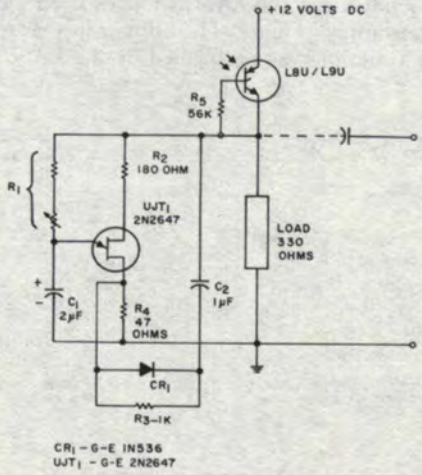


Figure 11.6 LASCR "Single Shot"

11.3.6 Impulse Actuated, Variable On-Time Switch

A random impulse of light fires the LASCR, applying current to the load. Capacitors C_1 and C_2 discharge through R_2, R_3, and through R_1 and the LASCR. As long as this capacitor-discharge current is higher than holding current, I_H, the LASCR cannot commutate, thus applying full wave AC to the load. When the discharge current drops below I_H, the LASCR will turn OFF at the next succeeding current zero, assisted by R_4 for inductive loads. Decreasing R_3 reduces the time the switch remains ON.

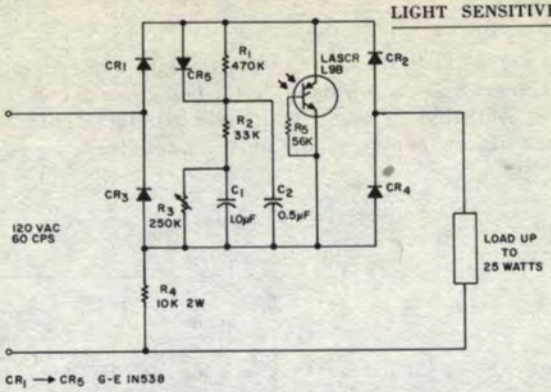


Figure 11.7 Impulse Actuated, Variable On-Time Switch

This switch can turn ON at any phase angle, but will turn OFF only at a current zero. During conduction, the full sine wave is applied to the load, with virtually no harmonic distortion. Radio noise is therefore negligible.

This circuit is useful for operation of solenoids, contactors, small motors, lamps, etc., particularly in conjunction with an optical programmer.

11.3.7 WSPC (World's Smallest Phase Control)

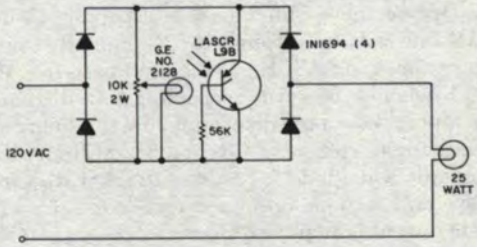


Figure 11.8 WSPC (World's Smallest Phase Control)

The miniature lamp No. 2128 has a small, low-mass filament with a short delay time compared with most lamps. With a low applied voltage, the time to reach the LASCR firing level for the lamp is about three cycles. As applied voltage is increased, this time is reduced, reaching about 1 millisecond when directly across the LASCR terminals thus providing phase control of the LASCR. Lamp voltage is removed when the LASCR fires, protecting the lamp and resetting it for the next half cycle. Lamp and LASCR should be in direct contact.

This circuit is very useful for small heating elements, such as a soldering iron, or for lamp dimming except at low end of range where flickering occurs as the result of changes in lamp resistance.

11.3.8 Production Line Flow-Monitor

This circuit has been used to monitor the smooth flow of small components down a high speed conveyor chute. It has the capability of "overlooking," or passing up, small self-clearing pile-ups, but it will shut the line down rapidly in the event of an impending catastrophic "jam."

Referring to Figure 11.9, the SCR is in series with a relay load, and is supplied from a 120 V AC line. SCR_1 is normally "off," being energized only when a fault condition occurs. With light "on," the LASCR conducts current, and prevents voltage from building up across capacitor C_1. Each time a passing component

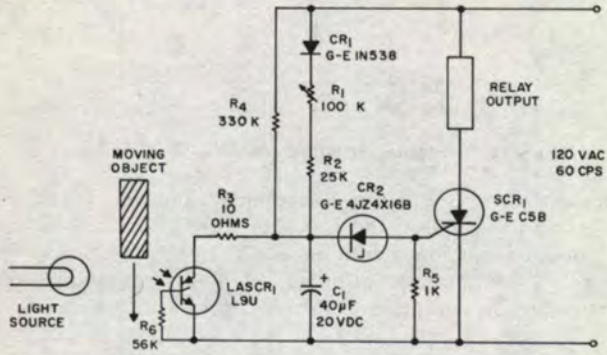


Figure 11.9 Flow Monitor

mementarily interrupts the light beam to $LASCR_1$, $LASCR_1$ is briefly commutated by the 60 cps AC line. During these "off" periods capacitor C_1 does start to charge (towards the peak AC line voltage through R_1, R_2 and CR_1) but is shorted to zero once more as light is restored to $LASCR_1$. If the light path to $LASCR_1$ is blocked for more than a few milliseconds, however, capacitor C_1 will *continue* to charge unimpeded by $LASCR_1$, and at some time determined by the time constant $C_1 \times (R_1 + R_2)$, will exceed the avalanche voltage of CR_2 and fire SCR_1. SCR_1 then activates the load. "Reset" is automatic when light is restored to $LASCR_1$. Circuit delay time can be adjusted from a few milliseconds up to several seconds by adjustment of R_1.

Where solid state output is required, the relay shown can be replaced with the actual load direct, or by moving the SCR inside a diode bridge (as Figure 11.3 c), full wave AC output can be realized.

11.3.9 "Slave" Electronic Flash

There is a need, in the photographic industry, for a fast photo-sensitive switch capable of triggering the "slave" flash units used extensively in multiple-light-source high speed photography. Figure 11.10 shows how an industry-standard flashgun circuit can be modified with an LASCR to serve as a fast acting slave unit. With switch S_1 closed, capacitor C_1 charges to 300 volts through R_1, and capacitor C_2, charges to approximately 200 volts through R_2 and R_3. When the master flashgun fires (triggered by the flash contacts on the camera) its light output triggers $LASCR_1$, which then discharges capacitor C_2 into the primary winding of transformer T_1. Its secondary puts out a high voltage pulse to trigger the flashtube. The flashtube discharges capacitor C_1, while the resonant action between C_2 and T_1 reverse biases $LASCR_1$ for positive turn-off. With the intense instantaneous light energy available from present-day electronic flash units, the speed of response of the LASCR is easily in the low microsecond region, leading to perfect synchronization between master and slave.

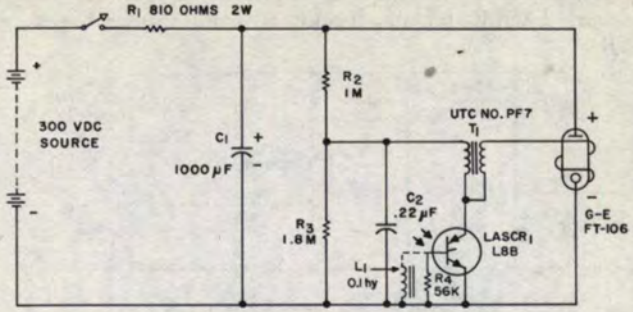


Figure 11.10 Slave Flash

High levels of ambient light can also trigger the LASCR when a resistor is used between gate and cathode. Although this resistance could be made adjustable to compensate for ambient light, the best solution is to use an inductance (at least 0.1 henry) which will appear as a low impedance to ambient light and as a very high impedance to a flash.

11.3.10 Precision Two-step Thermostat

The elementary bi-metal thermostat has problems of mechanical loading, slow make and break of contacts, and self-heating with current flow through it. Two light activated SCR's, a lamp, and a bi-metal can provide precise temperature regulation with two-step power control.

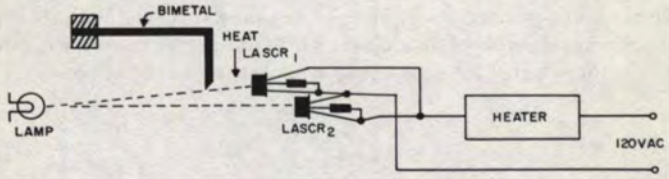


Figure 11.11 Thermostat

As temperature increases, the bi-metal blocks light from $LASCR_1$, reducing the heater to ½ power, then a further increase in temperature causes the bi-metal to block light from $LASCR_2$, turning the heater off completely. Since there is no mechanical loading, the differential of this thermostat is very small and is determined primarily by optics and the change in light-sensitivity of the LASCR with temperature and voltage.

11.3.11 Lamp Switching Circuit

For programmed operation of lamps in which the operation is repetitive for a large number of cycles, thermal stresses on lamps and on control are severe. A unijunction transistor control circuit, shown in Figure 11.12, can provide preheating of the lamp by triggering the LASCR late in each half-cycle. The setting of R2 will determine the minimum lamp current, as is required to maintain filament

temperature just below the visible level. Gate resistor, R1, may be adjusted to control sensitivity of the LASCR to light. One unijunction circuit may be used in conjunction with several LASCR and lamp circuits by using a separate gate resistor (R1) for each LASCR.

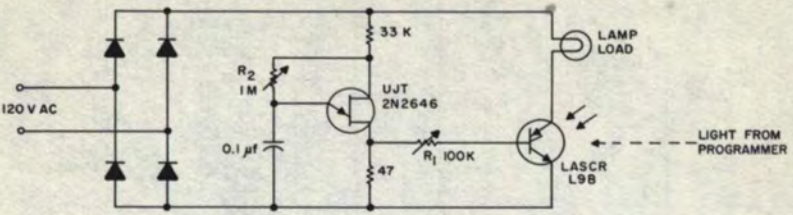


Figure 11.12 Lamp Switching Circuit

11.3.12 Temperature Compensation

Since light sensitivity of the LASCR is a function of junction temperature, some problems may be encountered where large variations in ambient temperature occur. If the changes in junction temperature caused by anode current are of negligible effect, some compensation for ambient temperature changes may be obtained by the use of a thermistor with series and parallel resistors in the gate circuit. Current is very low in the gate circuit, thus permitting the use of a small thermistor which can follow rapid changes of temperature.

11.4 P-N-P SYMMETRICAL PHOTO-TRANSISTOR CONNECTION

The region between anode and gate of the LASCR behaves as a reasonably symmetrical photo-transistor. Figure 11.13 shows typical voltage/current characteristics at several levels of irradiance. This connection is used with the ZJ227UX4 which is a factory-calibrated unit used for measurement of effective irradiance, H_E.

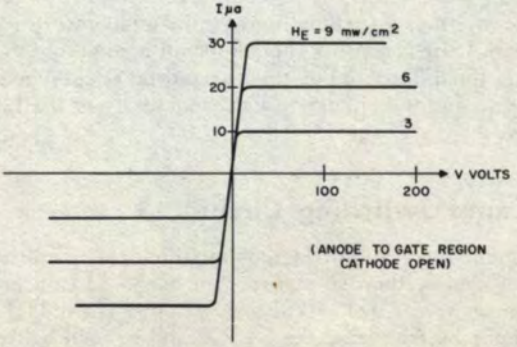


Figure 11.13 p-n-p Photo-Transistor Action of LASCR

11.4.1 Phase Detector

The photo-transistor action of the LASCR is useful in many ways, one of which is the phase-detector circuit shown in Figure 11.14.

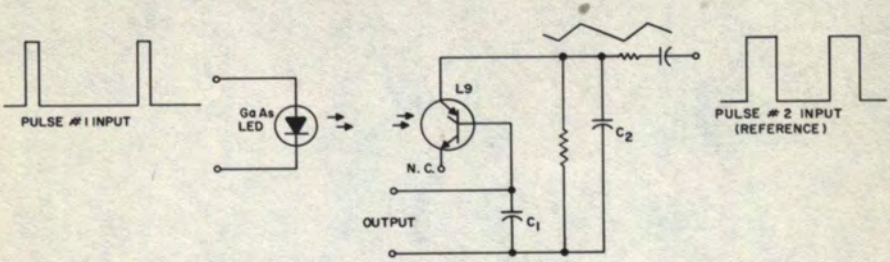


Figure 11.14 Phase Detector

The gallium arsenide light (IR) emitting diode produces a pulse of radiation coincident with the input pulse. The L9 charges capacitor C1 to a voltage determined by the phase relationship between pulse No. 1 and the integrated wave derived from pulse No. 2. Optical coupling provides balanced operation and isolation.

Gate Turn-Off Switch

12.1 INTRODUCTION

The gate turn-off switch (GTO) is a three terminal four layer p-n-p-n switching device. A logical development of the SCR, the GTO can be turned "off" as well as "on" from its gate input terminal. Thus, a positive pulse of gate current will latch the GTO into conduction, and a subsequent negative pulse will turn it off again. Current gain exists between anode and gate during turn-off as well as during turn-on. In DC switching applications, the GTO's two main advantages over SCR's are its gate turn-off capabilities *and* its higher speed operation. Commutating components are consequently smaller and less costly in GTO circuits, while device operation to 100 kc/s is attainable. Load waveform distortion is minimized because commutation transients are remote from the load carrying circuits. When compared to switching transistors, the GTO requires much less drive power, because of its true bistable nature, and is able to handle much higher load power for the same current rating, because it is inherently a high voltage device, whereas the transistor is not. In AC applications, the GTO can be phase controlled for power factor improvement purposes.[1]

12.2 GTO CHARACTERISTICS

The GTO, like the SCR, is triggered into conduction by injecting a pulse of forward current across its gate cathode junction. In general however, *more* gate current is required to trigger the GTO than an equivalently rated SCR. Latching and holding currents likewise are higher, as is power dissipation during forward conduction. As the potential turn-off capability of the GTO is increased, specifically its ability to commutate higher anode currents faster and with less gate energy, the wider these discrepancies between SCR and GTO become. They are the price paid for gate turn-off capability. The General Electric G5 series GTO features low trigger, latching and holding currents, with gate turn-off up to one ampere, while the G6 series requires higher trigger, latching and holding current, but has turn-off capability up to two amperes. For details on both these TO-5 packaged devices see Chapter 20 or Bulletin 150.60, available from General Electric Company, Auburn, N. Y.

12.2.2 V_{ROM} (rep) Rating

Since the GTO is intended primarily for use in DC switching applications, in most cases a high reverse voltage rating is unnecessary. For this reason all standard G5 and G6 devices have a nominal 25 volt reverse rating only. Where a higher reverse voltage capability is required of a G5 or G6, either a conventional silicon diode may be connected in series with a standard device, or special types* are available with equal forward and reverse voltage ratings up to 400 volts.

12.2.3 Turn-Off Requirements

To turn off a conducting GTO, sufficient *charge* must be extracted from its gate to cause internal regenration to cease (see Section 1.7). The amount of charge

*See your local General Electric semiconductor sales manager.

required may be computed from the *minimum turn-off gain* G_I)** of the device, and the gate pulse width at which G_I is specified. Since gain itself is a function of several variables, including pulse width, G_I is generally specified under a set of "worst case" conditions. The major factors affecting turn-off gain are:

(*a*) *Gate Pulse Width.* As the turn-off gate pulse duration is *decreased*, gate current magnitude must be *increased* to maintain the correct charge relationship. Figure 12.1 shows the relationship between turn-off gain and pulse duration for the G5/G6 GTO.

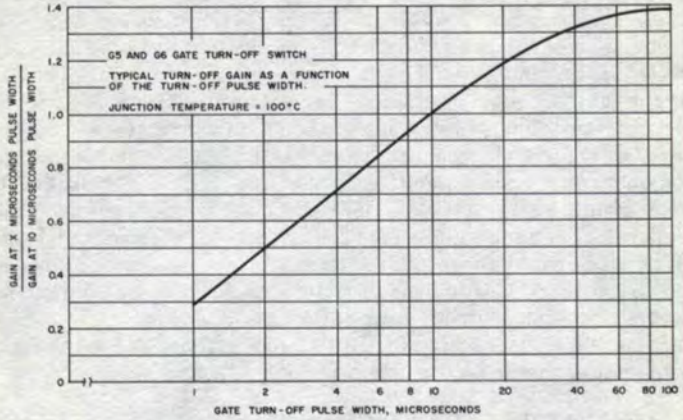


Figure 12.1. Turn-off Gain Versus Pulse Width

(*b*) *Anode Current.* Turn-off gain is dependent on the *magnitude* of anode current being turned off. As anode current is increased above the holding current level, turn-off gain drops rapidly from infinity at I_H to some minimum value, and then climbs steadily upward again. At slightly above the maximum anode current that can be gate-commutated, turn-off gain drops suddenly to zero. This effect is caused by the inability of the gate to maintain control over the *whole* GTO cathode region at high current levels, and is a characteristic of all gate turn-off switches. *It is possible to destroy a GTO by attempting to gate-commutate more than the design level of anode current.* Figure 12.2 shows the variation in turn-off gain with anode current for the G6 GTO.

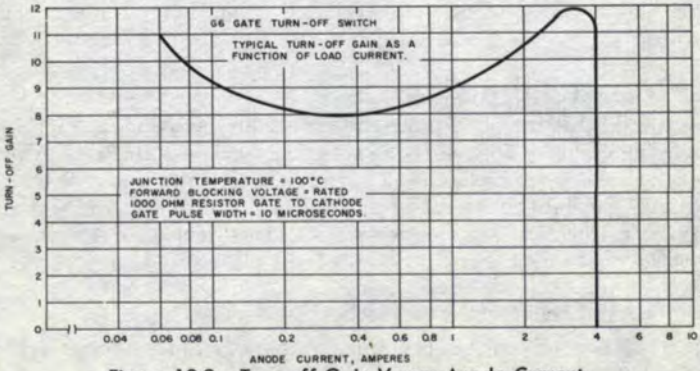


Figure 12.2. Turn-off Gain Versus Anode Current

**Turn-off gain is defined as the ratio of anode current being turned off to the negative gate current required to effect turn-off.

(*c*) *Junction Temperature.* In general, gain decreases as junction temperature increases. Minimum turn-off gain is usually specified, therefore, at maximum rated junction temperature (see Figures 12.1 and 12.2).

(*d*) *Anode Voltage and Load Impedance.* Turn-off gain is somewhat dependent on the anode supply voltage, and the nature of the load impedance in the anode circuit. As anode current starts to fall during the final phase of turn-off, the magnitude of the resultant voltage that develops across the center (blocking) junction of the GTO affects the ability of the gate to complete its job. The higher the voltage, the more difficult it becomes to complete commutation. Note that an unclamped inductive load can generate a high forward anode voltage during turn-off, which will affect gain in the same way as does a high supply voltage. Minimum turn-off gain specifications of all G-E GTO's apply at their rated anode voltage.

(*e*) *Turn-off Gate Pulse Rise and Fall Times.* A fast-rising negative gate pulse is beneficial to the turn-off process, but too rapid a pulse decay time can degrade the GTO's turn-off gain. Both these effects are associated with the GTO's gate-cathode capacitance. While the negative dv/dt of the pulse leading edge speeds up turn-off by discharging the gate capacitance *out of* the gate, the positive dv/dt of its trailing edge tends to *recharge the capacitance in a direction to retrigger the GTO.* A similar phenomenon affects the GTO during turn-on. Here a fast rising trigger pulse facilitates turn-on and a rapid decay encourages subsequent turn-off. The effect manifests itself during turn-on as an apparent decrease in gate trigger sensitivity and as an increase in anode latching current.

12.2.4 Gate Input Characteristics

The GTO is charge operated in the sense that positive gate current must flow for a finite period of time to trigger the device "on," while negative gate current

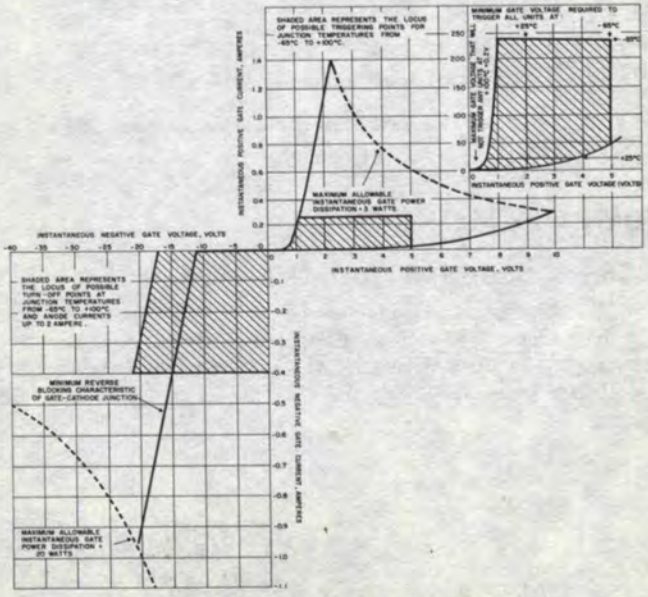


Figure 12.3. GTO Gate Characteristics

must flow to turn it off again. In either case *gate voltage* must also be provided to force the gate current through the GTO's internal gate impedance. Since the gate impedance is not constant, it is most convenient to display the gate volt-ampere characteristics of the GTO in graphical form. Figure 12.3 is a plot of the G6's gate characteristics.

The first quadrant defines the positive gate triggering voltage-current relationship, while the third quadrant displays the equivalent negative turn-off data. Note that to ensure turn-off of *all* G5/G6 devices, negative gate voltages *in excess of the static gate cathode avalanche voltage* of some units must be provided. This characteristic precludes the use of DC or long duration gate turn-off pulses, *unless* a silicon diode is connected in series with the GTO cathode lead. Without such a diode, overheating of the gate-cathode junction *after* turn-off might result. If the diode is not used, gate pulse duration must be less than specified in Figure 12.4, for a given gate pulse magnitude.

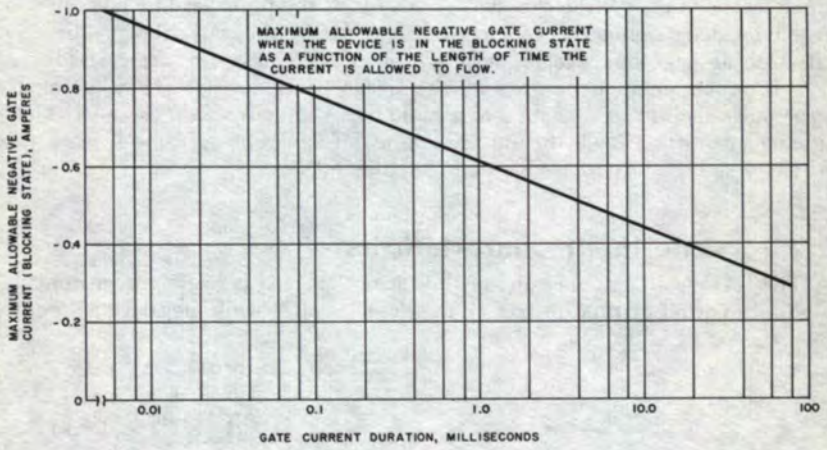


Figure 12.4. Avalanche Gate Current Versus Pulse Width

12.3 TURN OFF METHODS

12.3.1 Series Capacitor Turn-Off

Figure 12.5 shows how the GTO may be turned "on" and "off" by alternately charging and discharging a capacitor connected in series with its gate lead. When the switch S_1 is opened, capacitor C_1 charges to E_1 through R_1 and the GTO's internal gate impedance. For the GTO to trigger, the following equations must be satisfied:

$$R_1 \leq \frac{E_1 - V_{GTM}}{3 \cdot I_{GTM}} \quad \text{ohms} \qquad 12.1(a)$$

and

$$C_1 \geq \frac{t_1}{R_1 + \left(\frac{V_{GTM}}{I_{GTM}}\right)} \quad \text{farads} \qquad 12.1(b)$$

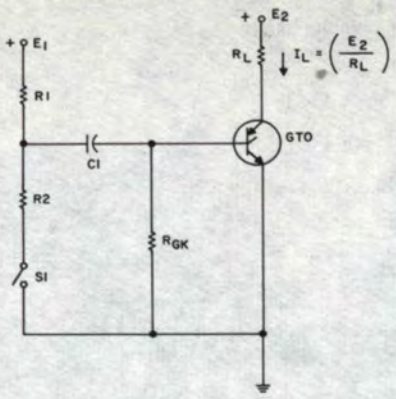


Figure 12.5. Series Capacitor Turn-off

where V_{GTM} = maximum gate voltage to trigger (volts)
I_{GTM} = maximum gate current to trigger (amps)
t_1 = pulse duration at which I_{GTM} is specified (seconds)

When S_1 is closed, the charged capacitor C_1 discharges through R_2 and the GTO's gate impedance, and the GTO will turn-off providing:

$$R_2 \leq \frac{E_1 - V_{GTO}}{2 \cdot I_{GTO}} \text{ ohms} \qquad 12.2(a)$$

and

$$C_1 \geq \frac{t_2}{R_2 + \left(\frac{V_{GTO}}{I_{GTO}}\right)} \text{ farads} \qquad 12.2(b)$$

where V_{GTO} = maximum gate voltage to turn-off (volts)
I_{GTO} = maximum gate current to turn-off I_L amps* (amps)
t_2 = time duration at which I_{GTO} is specified (seconds)
*I_L = anode current flowing at instant of commutation (amps)

Note that Equation 12.2(a) defines only the *maximum* value of R_2 for guaranteed commutation. In most practical circuits, for more rapid turn-off, R_2 can be made much *smaller* than its calculated value. The lower limit on R_2 is determined either by the peak reverse gate power rating of the GTO, or by some other limiting circuit consideration, such as the current rating of S_1, etc.

Example: Select R_1, R_2, and C_1 for a G6F GTO operating in the circuit of Figure 12.5, where $E_1 = E_2 = 28$ VDC, $T_A = 25°C$; $R_L = 28$ ohms.

Peak load current $I_L = \frac{E_2}{R_L} = \frac{28}{28} = 1$ amp.

From G6 Spec Sheet:
- maximum gate voltage to trigger at 25°C, $V_{GTM} = 2.0$ volts
- maximum gate current to trigger at 25°C, $I_{GTM} = 20$ mA
- minimum pulse width for 20 mA I_{GTM}, $t_1 = 20$ μs

From Equation 12.1(a)

$$R_1 \leq \frac{E_1 - V_{GTM}}{3 \cdot I_{GTL}}$$

$$\leq \frac{28-2}{3\times10^{-2}\times2}$$

$$\leq 430 \text{ ohms}$$

Let $R_1 = 390$ ohms (nearest 10% value).

From Equation 12.1(b)

$$C_1 \geq \frac{t_1}{R_1 + \left(\frac{V_{GTM}}{I_{GTM}}\right)}$$

$$\geq \frac{20\times10^{-6}}{820 + \left(\frac{2}{2\times10^{-2}}\right)}$$

$$\geq .0235\ \mu F$$

From G6 spec sheet, minimum turn-off gain $G_I = 5$ for 500 ma $\leq I_L \leq$ 2 amp, $T_J \leq 100°C$, $t_2 \geq 10\ \mu s$.

Maximum gate current to turn-off, I_{GTO}, is given by:

$$I_{GTO} = \frac{I_L}{G_I} = \frac{1}{5} = 200 \text{ mA}$$

From G6 Spec Sheet, maximum gate voltage to turn-off, $V_{GTO} = 21$ volts

From Equation 12.2(a)

$$R_2 \leq \frac{E_2 - V_{GTO}}{2 \cdot I_{GTO}}$$

$$\leq \frac{28-21}{2\times200\times10^{-3}}$$

$$\leq 17.5 \text{ ohms}$$

From Equation 12.2(b)

$$C_1 \geq \frac{t_2}{R_2 + \left(\frac{V_{GTO}}{I_{GTO}}\right)}$$

$$\geq \frac{10\times10^{-6}}{25 + \left(\frac{21}{200\times10^{-3}\times2}\right)}$$

$$\geq .129\ \mu F$$

Since the value of C_1 calculated for proper turn-off is higher than that required for turn-on, the higher of the two values must be used.

Let $C_1 = .15\ \mu f$ (nearest standard value)

From the G6 specification sheet, peak reverse gate power $P_{GM} = 20$ watts. The locus of all possible ($V_G \cdot I_G = 20$ watts) is plotted on Figure 12.3, and the gate turn-off source load line must lie to the right of this curve.

Open circuit gate source voltage $E_1 = 28$ volts

Maximum permissible short circuit current $I_{SC} = \left(\frac{E_1}{R_2}\right)$

where R_2 is the slope of the line drawn on Figure 12.3 from $E_1 = 28$ volts tangential to the 20 watt peak power locus. From Figure 12.3 slope of such a line $= 10$ ohms.

$\therefore R_2 = 10$ ohms min.

12.3.2 Parallel Inductor Turn-Off

The GTO can be turned off by attempting to interrupt DC current flowing in an inductor connected between its gate and cathode terminals. In the circuit of Figure 12.6, when switch S_1 is closed, current will flow through resistor R_1 and into the GTO's gate. Gate current will be a decaying exponential of peak value $\left(\frac{E_1 - V_{GTM}}{R_1}\right)$, and if $\left(\frac{E_1 - V_{GTM}}{R_1}\right) >> I_{GTM}$, the GTO will trigger. Assuming the GTO's gate impedance is high compared to the DC resistance of inductor L, in the steady state $i_L \cong \frac{E_1}{R_1}$. If switch S_1 is now opened, the current i_L must transfer from R_1 to the GTO's gate, and the GTO will turn off providing:

$$\frac{E_1}{R_1} \geq 2\ I_{GTO} \qquad 12.3(a)$$

and

$$\frac{L \cdot I_{GTO}}{V_{GTO}} \geq t_2 \qquad 12.3(b)$$

where I_{GTO} = gate current required to turn off I_L anode amps (amps)
V_{GTO} = gate voltage at I_{GTO} (volts)
t_2 = pulse width specified at I_{GTO} (seconds)

Because the switch S_1 is required to carry the *peak* turn-off current i_L for as long as the GTO is in conduction, it is usually necessary to select R_1 for *minimum* permissible turn-off current. In low speed circuits i_L can be minimized by stretching out the turn-off pulse time constant (see Section 12.2.3).

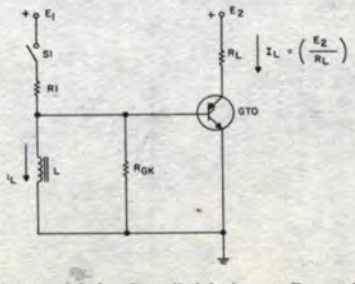


Figure 12.6. Parallel Inductor Turn-off

12.3.3 Load in Cathode Commutation

In the circuit of Figure 12.7 the load impedance is connected between the GTO's cathode terminal and ground. If a short positive pulse of gate current is applied to the GTO's gate terminal through diode CR_1, the GTO will trigger and energize the load. Diode CR_1, which should be a fast recovery type, decouples the gate triggering source as the GTO's gate and cathode terminals jump up to the supply voltage. The GTO can now be turned off by closing switch S_1, when current is diverted *out of* the gate terminal to ground through current limiting resistor R_1. The value of R_1 is selected so that as the load (cathode) current and voltage decay during the final phase of turn-off, sufficient current always flows out of the gate to satisfy the relationship.

$$R_1 \geq R_L(G_I - 1) - \frac{V_{GTO} - G_I}{I_A} \qquad 12.4$$

where G_I = minimum turn-off gain over the *anode* current range I_A to holding current

V_{GTO} = maximum turn-off gate voltage (volts)

I_A = peak *anode* current during commutation $= \dfrac{I_L}{\left(1 - \dfrac{1}{G_I}\right)}$ (amps)

Capacitor C_1, which provides a low impedance bypass around the load for the triggering pulse, also tends to aid the turn-off process by "holding up" the load voltage as cathode current falls. In circuits where the load impedance itself presents a sufficiently low impedance to the trigger pulse, C_1 can often be eliminated.

Because there is no energy storage needed in reactive commutating elements, as in the two previous turn-off methods, GTO circuits employing cathode commutation are capable inherently of very high speed operation. The main disadvantage of the method is that during the turn-off interval anode current is *increased* by the amount of gate current flowing through R_1. As a consequence the allowable load (cathode) current must be reduced by a like amount so that the total peak *anode* current rating (2 amps for the G6) of the GTO is not exceeded during turn-off.

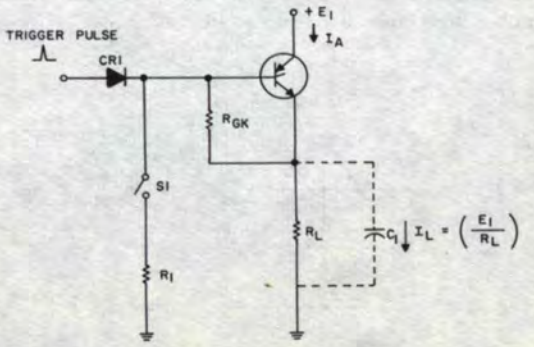


Figure 12.7. Load in Cathode Commutation

12.4 SPECIAL TURN-OFF CIRCUITRY

In some GTO applications it is possible to aid the gate turn-off action by means of special circuitry. One such circuit is shown in Figure 12.8.[3] Here, as the GTO starts to turn off under the influence of a negative gate signal, part of the diminishing anode current is diverted away from the GTO as charging current to capacitor C. The amount of current diverted depends on the size of C and on the rate of rise of anode voltage during turn-off thus:

$$I_C = C \cdot dv/dt$$

This circuit allows higher than rated anode current to be gate commutated, although at the expense of (load) turn-off speed. Resistor R is added to limit capacitor discharge current through the GTO during turn-on. Diode CR_1 bypasses R for maximum current diversion during turn-off.

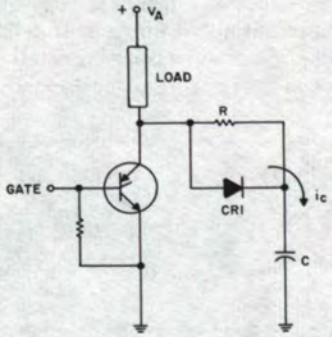


Figure 12.8. Circuit to Enhance Turn-off

12.5 GTO APPLICATIONS

12.5.1 High Voltage Flip-Flop, or Triggered Multivibrator

Figure 12.9 is a GTO adaptation of the SCR capacitor commutated flip-flop. As shown, the circuit transfers load current from one load to the other each time a positive trigger pulse is applied to the common input line. Operation to over 10 kc/s is possible, and the circuit will accommodate a wide range of load voltages and currents, with suitable component selection.

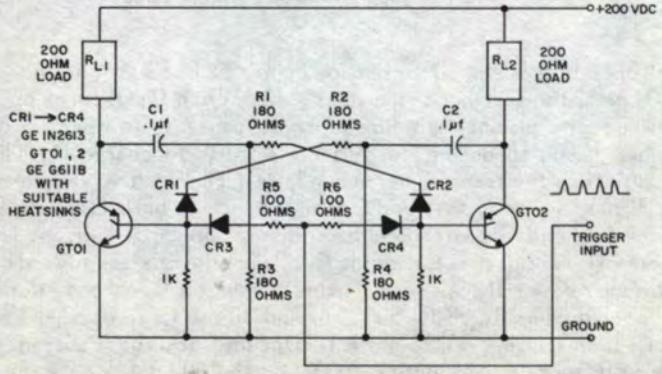


Figure 12.9. High Voltage GTO Flip Flop

Assume GTO_1 is conducting load current, and GTO_2 is blocking. Capacitor C_2 charges to the supply voltage through R_{L2} and resistor R_4. When GTO_2 is turned on by the next positive trigger pulse through R_6 and CR_4, the gate of GTO_1 is driven negative by the voltage on C_2, and GTO_1 turns off. Peak negative gate current is limited by resistor R_2. GTO_2 is commutated in turn by capacitor C_1, as GTO_1 is triggered on again.

12.5.2 SCR Trigger Circuit, or High Power Pulse Generator

The flip-flop configuration of Figure 12.9 can, with slight modifications, be used as a trigger pulse generator for high power SCR's in inverter circuits, or in other applications where high peak pulse power is required. Figure 12.10 illustrates such a trigger circuit that incorporates means for positive starting when power is first applied. Each of the four output windings will deliver over 1 amp peak into a 10 ohm load. Output pulse rise time is approximately 1 microsecond and pulse width is around 20 microseconds. The circuit has operated to 10 kc/s.

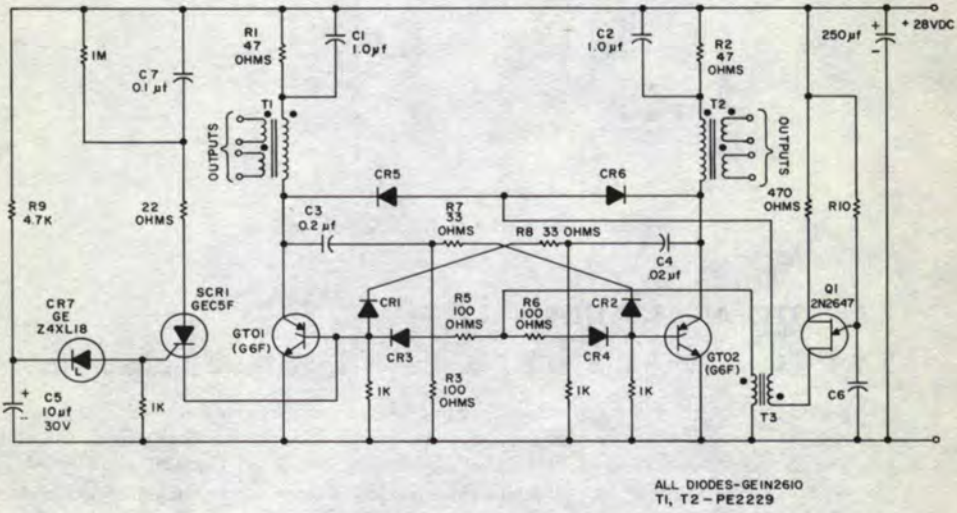
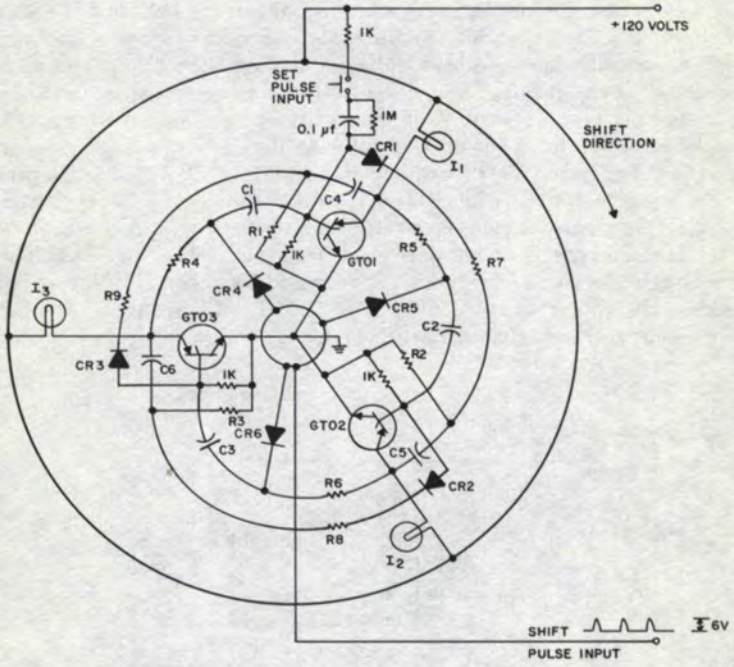


Figure 12.10. High Power SCR Trigger Circuit

Circuit operation is similar to that of Figure 12.8. Each time the unijunction transistor Q_1 fires, the GTO's change their state. When GTO_1 turns on, a pulse of current flows in the primary winding of transformer T_1 to charge capacitor C_1; similarly when GTO_2 turns on, current flows in T_2 to charge C_2. These pulses appear as outputs in the transformer secondaries. The positive start feature works as follows: When power is first applied to the circuit both GTO_1 and GTO_2 are "off." Diodes CR_5 and CR_6 are both back biased, interbase current is unable to flow in Q_1, and Q_1 cannot fire. Capacitor C_5 meanwhile charges towards the supply voltage through resistor R_9. As soon as the voltage on C_5 exceeds the breakdown voltage of zener diode CR_7, SCR_1 turns on and allows C_7 to charge. The charging current of C_7 then triggers GTO_1. With GTO_1 "on", interbase current for Q_1 can flow through CR_5 and the conducting GTO, and the UJT takes over the triggering.

12.5.3 Ring Counter

A ring counter may be considered as a circuit that sequentially transfers voltage from one load to the next, when a number of loads are connected to form a closed loop as in Figure 12.11. Transfer around the loop proceeds always in the same direction, and is initiated by pulsing a common shift line. The ring counter is actually an extension of the basic flip-flop circuit. a flip-flop being a two stage ring counter. In the circuit of Figure 12.11 three GTO's are used to drive a trio of incandescent lamps, but other types of load may be substituted and more stages added as desired. A ten stage circuit using 10 GTO's can be used to perform the function of a decade counter with direct lamp readout.



I_1, I_2, I_3, - 120 VOLT, 25 WATT INCANDESCENT LAMP
$CR_1, CR_2, CR_3, CR_4, CR_5, CR_6$, - GENERAL ELECTRIC IN2611
C_1, C_2, C_3, - .05 μf 200 VOLTS
C_4, C_5, C_6, - .02 μf 200 VOLTS
R_1, R_2, R_3, 1 K 1/2 WATT
R_4, R_5, R_6, 100 K 1/2 WATT
R_7, R_8, R_9, 1.2 K 1/2 WATT
GTO_1, GTO_2, GTO_3, - GENERAL ELECTRIC G6G

Figure 12.11. High Voltage Ring Counter

When power is first applied to the circuit none of the GTO's will turn on. To "start" the circuit, "the set pulse input" button is closed, which turns on GTO_1 and applies voltage to the lamp load I_1. At this point diodes CR_4 and CR_6 will be reverse biased by the full supply voltage while diode CR_5 will be reverse biased by less than 2 volts, as determined by the respective anode voltages of the GTO's.

If a positive pulse having amplitude greater than 4 volts, but less than the supply voltage, is applied to the shift line, CR_4 and CR_6 will block the pulse from the gates of GTO_1 and GTO_3 while the pulse will be transmitted to the gate of GTO_2 through CR_5 and C_2, causing GTO_2 to turn on. As GTO_2 turns on, GTO_1 is turned off by the negative gate transient coupled into its gate via C_5, R_7 and diode CR_1. When the next pulse arrives at the shift line, GTO_3 turns on and GTO_2 turns off etc., etc.

12.5.4 High Speed Solenoid Driver

Figure 12.12 shows how the G6 GTO can be used as a high speed "hammer" driver for a computer (or similar) read-out mechanism. Since speed is the primary objective here, the load solenoid is deliberately overdriven for a short time by connecting it suddenly across a high voltage bus, and then disconnecting it again before overheating can occur. The G6 has both the switching speed and high voltage ability for this type of duty. A short positive pulse of gate current turns on GTO_1, applying power to the load. Capacitor C_1 bypasses the load impedance for the triggering pulse. Since GTO's cathode and gate rise to B+ potential, diode CR_2 disconnects the gate source while GTO_1 is "on." When SCR_1 is triggered sometime later, GTO_1's gate is connected to ground through the current limiting resistor R_1, load current is momentarily diverted, and GTO_1 turns off. Thyrector CR_3 suppresses inductive kicks from the solenoid to acceptable levels, while at the same time allowing a short solenoid reset time. Load current rise and fall times are both considerably less than 1 millisecond.

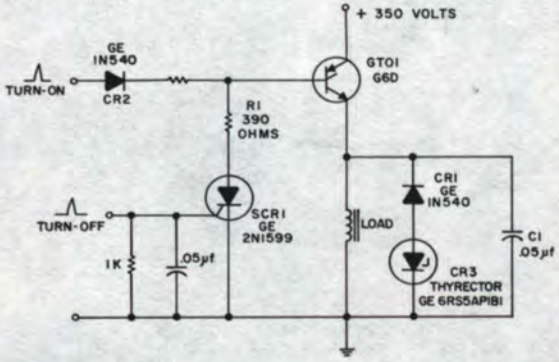


Figure 12.12. High Speed Solenoid Driver

12.5.5 Sawtooth Generator

Figure 12.13 illustrates a free-running high voltage sawtooth generator. When power is applied to the circuit, the G6 will trigger and connect the supply across C_1. As the voltage across C_1 rises above V_Z (the avalanche voltage of CR_1), GTO_1's gate becomes reverse biased, current in the gate lead reverses, and the device turns off. C_1 then discharges through R_1 and the parallel external load impedance, if any. GTO_1 will turn on and repeat the cycle when the voltage across C_1 decays sufficiently below V_Z for positive gate current to flow again.

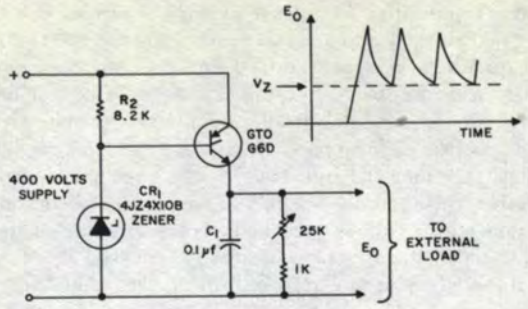


Figure 12.13. Sawtooth Generator

12.5.6 200 volt to 24 volt DC converter and Voltage Regulator

The GTO is an ideal device for use in DC to DC stepdown transformer applications. It has the necessary voltage capability to work from high voltage DC power sources, is able to switch efficiently at high frequency for good transformer utilization, is small, rugged and has silicon reliability. Figure 12.14 shows how a single GTO, operating as the prime switching and regulating element, is combined with a silicon power transistor to form a high performance 200 volt DC to 24 volt DC regulated power supply. This type of circuit, by virtue of its low weight, small size and good efficiency is adaptable to many computer, missile, and airborne power supplies, test equipment and various other industrial applications.

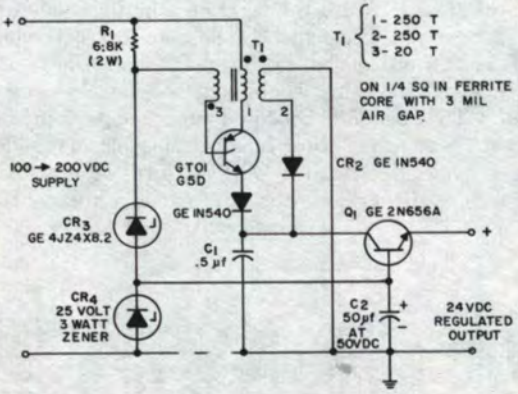


Figure 12.14. DC Converter and Voltage Regulator

With power applied to the circuit GTO_1 is gated on via resistor R_1. As GTO_1 starts to turn on and current flows in the primary winding of transformer T_1, a positive pulse of voltage is coupled into the GTO gate winding to regeneratively speed up GTO turn-on time and minimize GTO switching losses. With GTO_1 "on," capacitor C_1 charges up towards the supply voltage, charging current being limited by the inductance of T_1's primary winding. As the voltage across C_1 rises

above the breakdown potential, V_Z, of the avalanche diodes (CR_3 and CR_4), GTO_1's gate becomes reverse biased and negative gate current starts to flow. GTO_1 then turns off. GTO turn-off time is reduced by the regenerative "kick" induced in the GTO gate winding by the falling primary transformer current. With GTO_1 completely turned off, the inductive energy previously stored in T_1 is "pumped" into capacitor C_1 via feedback winding (2) and diode CR_2. The voltage across C_1 then decays under the influence of the external load until it falls below V_Z. As the capacitor voltage falls below V_Z, positive gate current again flows, the GTO turns on, and the cycle is repeated. Total voltage excursion across C_1 is 28–45 volts. This low voltage ripple content is removed by transistor Q_1, which, because it is connected as an emitter follower, also provides a very low output impedance to the load.

With input voltage varying between 100 and 200 volts DC, and/or load current varying between 0–100 milliamperes, output voltage regulation is less than 3%. Ripple at full load is less than 300 millivolts RMS.

Over-all circuit efficiency is around 50% with the components shown. Most of the circuit losses occur in resistor R_1, which has to provide gate trigger current for the GTO at the lowest expected supply voltage. For optimum efficiency with other supply voltages, R_1 should be selected to provide 10 milliamperes to the GTO gate.

12.5.7 High Frequency Chopper

The chopper circuit of Figure 12.15 is notable both for its versatility and extreme simplicity. When power is applied to the circuit, GTO_1 stays off until the volt-second integral across winding 1–2 of transformer T_1 is sufficient to cause T_1 to saturate. As T_1 saturates, its impedance falls and positive gate current flows through R_1 and R_2 to trigger the GTO. Winding 3–4 provides regeneration to speed up the turn-on process. With the GTO conducting load current, the voltage across winding 1–2 reverses, since the GTO's gate and cathode terminals are at +28 volts, and T_1 comes out of saturation. GTO_1 continues to conduct until T_1 saturates in the reverse direction, when negative gate current flows to ground through R_2 and the GTO turns off. On-to-off time is determined by the setting of potentiometer R_2; alternatively a third bias winding may be added to T_1 to effect control of the duty cycle electrically. With a third winding added, DC control current in one direction will increase the duty cycle, while control current in the

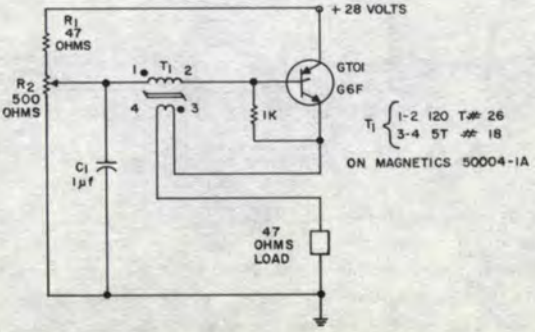


Figure 12.15. Single Ended 100 Kc/s Chopper

opposite direction will decrease the duty cycle. By applying AC to the control winding it is possible to modulate the average output load current. With the components shown in Figure 12.15, the circuit operates at approximately 100 kc/s.

12.5.8 High Voltage Generator

The circuit of Figure 12.16 may be used as a very high voltage pulse generator,* or as a DC to DC step up transformer. Operation is as follows: With transistor Q_1 biased "on," current flows through R_1 to trigger the GTO. With the GTO "on," current builds up both in the primary of transformer T_1 and in the inductor L_1. When Q_1 is shut off, the current flowing in L_1 transfers to the GTO gate, and the GTO turns off. As the GTO turns off a high voltage pulse is induced in the secondary of T_1. The pulse is in the form of a damped oscillation, of frequency determined by T_1 and capacitor C_1. The output may be rectified and integrated if desired. With the components shown, 3 to 5 kv peak is available at the output terminals of T_1.

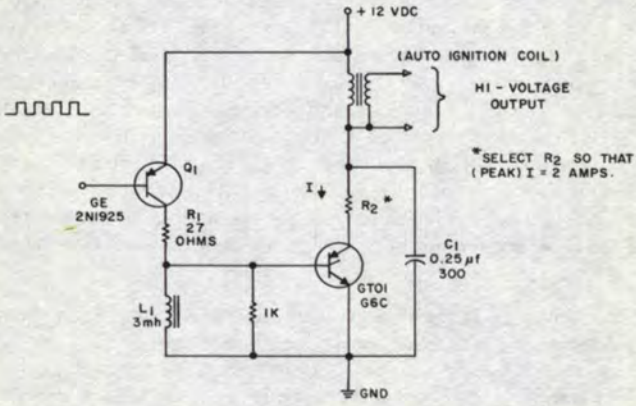


Figure 12.16. High Voltage Pulse Generator

12.5.9 GTO-UJT Astable Multivibrator

In the circuit of Figure 12.17(a), a gate turn-off switch and a unijunction transistor are combined to form an astable, or free-running, multivibrator. Rectangular current pulses of up to 2 amperes peak amplitude are available at the GTO anode terminal, while a further low power output may be taken from base two of the UJT. As shown the circuit operates with a 50% duty cycle at approximately 1 cps, but it may be modified for use from 0.1 cps to over 1 kc/s. The duty cycle also is variable.

When power is first applied to the circuit, gate current flows through R_1 and C_1, and through R_2 to trigger the GTO. With the GTO "on," the right hand plate of C_1 charges towards E, through R_1 and the GTO's gate junction. When the voltage across C_1 reaches the UJT's emitter peak point voltage (② on Figure

*With suitable components this circuit forms the basis of an extremely high performance automotive-type ignition system. Using a low-inductance ignition coil in conjunction with an experimental 7 ampere GTO, the circuit develops 25–30 kv with minimal output droop from 0 pps to 400 pps, equivalent to 0–6000 RPM for a four-stroke V8 auto engine.

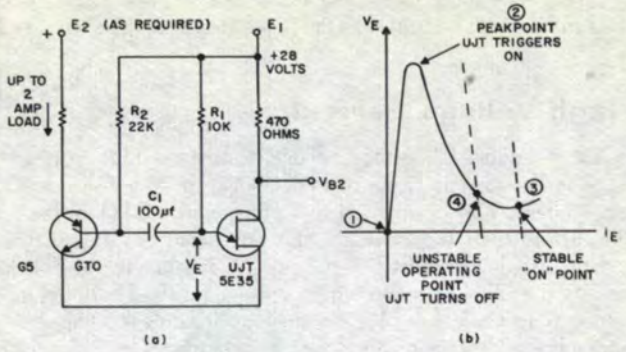


Figure 12.17. UJT—GTO Multivibrator

12.17(b)), the UJT fires and its emitter voltage falls. Simultaneously the gate of the GTO is driven negative and the GTO turns "off." With the GTO "off," the left hand plate of C_1 charges toward E, through R_2 and the conducting UJT's emitter. During this interval the UJT operates stably at ③ on Figure 12.17(b), its emitter current being the sum of the current through R_1 and the charging current of C_1. When the voltage on C_1 becomes sufficiently positive to forward bias the GTO gate however, the current in R_2 transfers from C_1 to the GTO's gate, the UJT's emitter current falls, and its operating point shifts to ④ on Figure 12.17(b). Now unstable, the UJT turns off (to ① on Figure 12.17(b)), and as the UJT turns off the GTO triggers on. The cycle then repeats itself ①—②—③—④—① etc.

Circuit frequency is inversely proportional to the capacitance of C_1, GTO "off" time is determined primarily by R_1, and "on" time by R_2. The GTO's anode load affects the circuit timing only in as much that the turn-off gate current precharges the left hand plate of C_1, an effect which tends to lower the GTO "off" time. The effect can be minimized by making C_1 large. For further variations of the circuit, see General Electric 5E35 specification sheet 60.65, available from Semiconductor Products Dept., GE Co., Electronics Park, Syracuse, N. Y.

REFERENCES

1. Introduction to Turn-Off Silicon Controlled Rectifiers, H. F. Storm, IEEE Conference Paper CP 63-321.
2. Characteristics of the Gate Controlled Turn-Off Trinistor Controlled Rectifier, J. W. Motto, Jr., IEEE Conference Paper CP 63-510.

Protecting the SCR Against Overloads and Faults

Satisfactory operation of SCR circuits and the equipment in which they operate often depends heavily on the ability of the system to survive unusual overcurrent conditions. One obvious answer to this requirement, although not usually an economical one, is to design the system to withstand the worst fault currents on a steady-state basis. This requires semiconductors and associated components that are rated many times the normal load requirements. Where this approach is not possible because of economics or other factors, an adequate overcurrent protective system is usually used.

13.1 WHY PROTECTION?

According to the AIEE Subcommittee on Electronic Converter Circuits,[1] the functions of an overcurrent protective system are any or all of the following:

1. To limit the duration of overloads and the frequency of application of overloads.
2. To limit the duration and magnitude of DC short circuits.
3. To limit the duration and magnitude of fault currents due to shorted cells.

The objective of these functions is to safeguard not only SCR's and diodes but also the associated electrical devices and buswork in the rectifier equipment from excessive heating and magnetic stresses. The trend toward high capacity systems feeding electronic converter equipment often results in extremely high available fault currents. Since both heating and magnetic stresses in linear circuit elements respond to the square of the current, the importance of adequate protection in "stiff" systems is self-evident.

Elaborating on function No. 3 above, SCR's as well as diode rectifiers may fail by shorting rather than by opening. In all power rectifier circuits except the simple half-wave circuit, such a cell fault results in a direct short from line to line through the low forward resistance of the good cells in adjacent circuit legs during

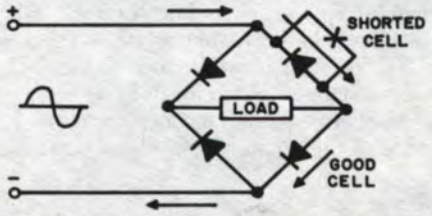


Figure 13.1 Arrows Indicate Flow of Fault Current Through Good Cell After Adjacent Leg Has Shorted. Load Resistance Does Not Limit Current.

at least part of the cycle. See Figure 13.1 where the diode symbol is used to represent both SCR's and diodes for the sake of generalization. Under these circumstances, a protective system functions either to shut the entire supply down, or to isolate the shorted cell in order to permit continuity of operation. This will be discussed at greater length later.

It is difficult to make broad recommendations for overcurrent protection since the concept of satisfactory operation means different levels of reliability in different applications. The selection of a protective system should be based on such individual factors as:

1. The degree of system reliability expected.
2. The need or lack of need for continuity of operation if a semiconductor fails.
3. Whether or not good rectifier cells are expendable in the event of a fault.
4. The possibility of DC bus faults.
5. The magnitude and rate of rise of available fault current.

Depending upon the application, these various factors will carry more or less weight. As the investment in semiconductors increases for a specific piece of equipment, or as an increasing number of parallel cells in a circuit increases the possibility of a single cell failure, or as continuity of operation becomes more essential, more elaborate protective systems are justified. On the other hand, in a low-cost circuit where continuity of operation is not absolutely essential, the semiconductors may be considered expendable and a branch circuit fuse in the AC line may be all that is needed, or justified, for isolation of the circuit on faults.

It is therefore reasonable that each circuit designer rather than the semiconductor component manufacturer decide precisely what level of protection is required for a specified circuit. Once the specific requirements are determined the component manufacturer can recommend means of attaining these specific objectives. This chapter is prepared to assist the circuit designer in determining his protection requirements, and then to select satisfactory means of meeting these requirements.

13.2 OVERCURRENT PROTECTIVE ELEMENTS

The main protective elements can be divided into two general classes. One class consists of those devices which protect by interrupting or preventing current flow, and the other class consists of those elements which limit the magnitude or rate of rise of current flow by virtue of their impedance.

Among the elements in the first class are:

1. The AC circuit breaker or fuse which disconnects the entire circuit from the supply.
2. The cell fuse or breaker which isolates faulted cells.
3. DC breakers or fuses which isolate load faults from the rectifier or a faulted rectifier from DC feedback from the load or parallel converter equipments.
4. Current limiting fuses and SCR circuit breakers.
5. Gate blocking of SCR's to interrupt overcurrent.

Among the elements of the second class which limit magnitude or rate-of-rise of current are:

1. Source impedance.
2. Transformer impedance.
3. Inductance and resistance of the DC circuit.

Throughout this discussion it is well to bear in mind that circuit interrupting devices that are tripped by magnetic circuits, such as solenoids in fast-acting breakers and interrupting devices that are tripped by thermal means, such as fuses or breakers with thermal overloads, all react to the RMS value of the current. The semiconductor itself reacts essentially to heating, but having a non-linear resistance, it heats proportional to a current value somewhere between the RMS and

average value. The considerable difference that may occur between these respective values of current in rectifier circuits is of particular importance in co-ordinating protective elements with one another and with the semiconductors.

13.3 CO-ORDINATION OF PROTECTIVE ELEMENTS

Depending upon their complexity and the degree of protection desired, con verter circuits include one or more of the various interrupting devices listed above. Functioning of these devices must be co-ordinated with the semiconductor and with each other so that the over-all protection objectives are met. Fuses or breakers must interrupt fault currents before semiconductor cells are destroyed. In isolating defective cells from the rest of the equipment, only the fuse or breaker in series with a defective cell should open. Other fuses and breakers in the circuit should remain unaffected. On the other hand, when a DC load fault occurs, main breakers or fuses should function before any of the cell-isolating fuses or breakers function. This fault discriminating action is often referred to as selectivity. In addition, the voltage surges developed across SCR's and diode rectifiers during operation of protective devices should not exceed the transient PRV rating of these cells. More complex protective systems require meeting additional co-ordinating criteria. The example of a protection system and its associated co-ordination chart described later in this discussion illustrates some of the basic principles of co-ordination for both overloads and stiff short circuits.

The magnitude and waveshape of fault and overload currents vary with the circuit configuration, the type of fault, and the size and location of circuit impedances. Fault currents under various conditions can generally be estimated by analytical means. References 1, 2, and 3 show analytical methods for calculating fault currents for generally encountered rectifier circuits.

For overloads on rectifier or inverter circuits where the current is limited to a value which the semiconductors can withstand for roughly 50 milliseconds, conventional circuit interrupting devices like circuit breakers and fuses can usually be used satisfactorily for protection. This type of overload can be expected where a sizeable filter choke in the load or a "weak" line limits the magnitude or rate of rise of current significantly. By placing the circuit breaker or fuse in the line ahead of the semiconductors, the protective device can be designed to isolate the entire circuit from the supply source whenever the line current exceeds a predetermined level which approaches the maximum rating of the semiconductors for that duration of fault.

For time intervals greater than approximately 0.001 second after application of a repetitive overload, the SCR rating for co-ordination purposes is determined by the methods discussed in Section 3.6.1. If the overload being considered is of a type that is expected only rarely (no more than 100 times in the life of the equipment), additional SCR rating for overload intervals of one second and less can be secured by use of the surge curve and I^2t rating for the specific device being considered.

The surge characteristic is expressed as the peak value of a half-sine wave of current versus the number of cycles that the semiconductor can handle this surge concurrent with its maximum voltage, current, and junction temperature ratings. In circuits that do not impose a half-sine wave of fault current on the semiconductors, the surge curve can be converted into current values that represent the particular waveshape being encountered. The surge curve for the semiconductor can be converted to different waveshapes or different frequencies in an approximate, yet conservative, manner for this time range by maintaining equivalent RMS values

of current for a specific time interval. For example, the peak half-sine wave surge current rating of the C35 SCR for 10 cycles on a 60 cps base is shown on the spec sheet to be 88 amperes. For a half-sine waveshape, the RMS value of current over the complete cycle is one-half the peak value, or 44 amperes. To convert this to average cell current in a three-phase bridge feeding an inductive load (120-degree conduction angle), divide this RMS value by $\sqrt{3}$ ($44 \div \sqrt{3} = 25.4$ amps). To determine the total load current rating for a bridge using this cell, multiply the average cell current by 3 ($25.4 \times 3 = 76.2$ amps).

13.4 PROTECTING CIRCUITS OPERATING ON STIFF POWER SYSTEMS

Conventional circuit breakers and fuses can be designed to provide adequate protection when fault currents are limited by circuit impedance to values within the semiconductor ratings up to the time when these protective devices can function. However, circuits requiring good voltage regulation or high efficiency will usually not tolerate high enough values of series impedance to limit fault currents to such low values. When a fault occurs in a circuit without current limiting impedance, current will develop in a shape similar to the dashed line in Figure 13.2. Its rate of rise is limited by the inductance inherent in even the stiffest practical systems. If the peak available current substantially exceeds the semiconductor ratings, and if it is permitted to flow in the circuit, the semiconductor would be destroyed before the current reaches this first peak. Conventional circuit breakers and fuses will not function quickly enough. Instead, so-called "current limiting" fuses which melt extremely fast at high levels of current are used. Alternately, "electronic circuit breakers" of the type discussed in Section 7.9 can be designed for this purpose.

The action of a typical current limiting fuse is indicated in Figure 13.2. Melting of the fuse occurs at point A. Depending on the fuse design and the circuit, the current may continue to rise somewhat further to point B, the peak let-thru current. Beyond this point the impedance of the arcing fuse forces the fault current down

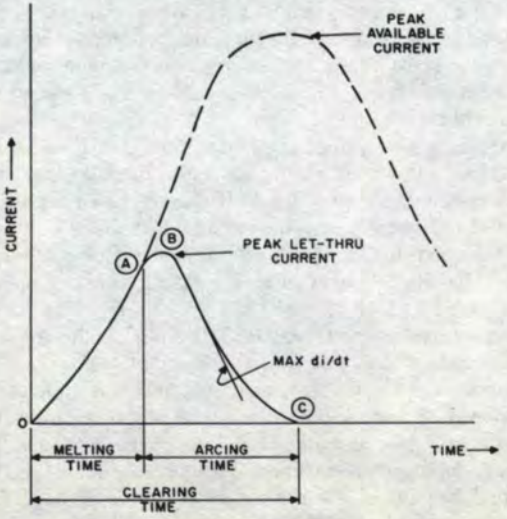


Figure 13.2 Limiting Action of Current Limiting Fuse

to zero at some point C. A satisfactory current limiting fuse will have an arcing time approximately equal to the melting time. If the fuse interrupts fault current too quickly, the high rate of change of current (di/dt) will induce levels of transient voltage in the circuit inductances that can destroy rectifier cells. For this same reason, it is not wise to use any higher voltage fuse rating than is required by the supply voltage. Surplus voltage rating of a fuse over the circuit voltage can lead to unnecessarily abrupt arc-quenching with resultant destructive voltage transients. However, the current interrupting rating of the fuse should be ample for the maximum available current to be expected.

Since the buildup of current is so rapid and since the current amplitude is so high in a circuit with low impedance, additional phases and circuit legs usually help very little in increasing the fault current capacity of a circuit because permanent damage may be done before commutation to another leg can occur. For conservative design, all fault current on stiff faults should be considered to flow through only one leg, dividing only between the parallel cells in that particular leg.

Both current limiting fuses[4,5] and semiconductors with uniform current distribution across their junctions[6,7] exhibit ability to withstand essentially constant $\int i^2dt$ below approximately one cycle (i = instantaneous current, t = time). This fortunate circumstance provides a simple tool for co-ordinating current limiting fuses and semiconductors in this difficult-to-define area below one cycle. The necessity of calculating fault currents in this region for co-ordination purposes is thereby largely eliminated. If the interrupting or clearing I^2t rating of a fuse is lower than the I^2t rating of the cell in series with it, the fuse will interrupt fault current before the cell fails regardless of current magnitude or rate of rise in the sub-cycle region.

Major fuse manufacturers now publish maximum clearing I^2t data on their

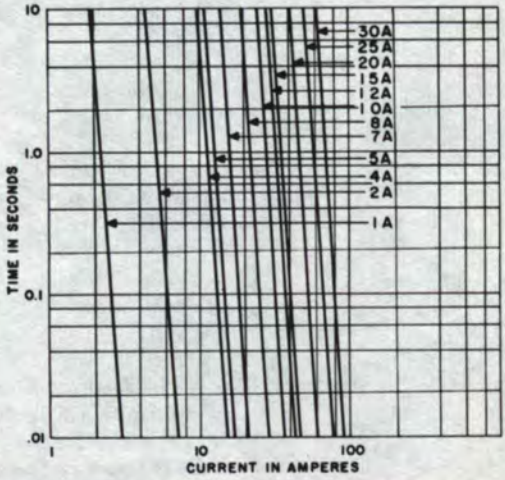


Figure 13.3 Form 101 Amp-Trap Characteristic Curves, Melting Time vs. Current, 1 to 30 Ampere Cartridge Size, 250 Volt—Type 1

current limiting fuses. However, where manufacturers do not publish I^2t ratings for their current limiting fuses, the clearing I^2t to melting can be approximated from the melting time-current characteristic of the fuse. Figure 13.3 illustrates the characteristics of a line of current limiting fuses manufactured by the Chase-

Shawmut Company, Newburyport, Massachusetts. The melting I^2t of the 30-ampere fuse, for example, can be approximated by squaring the current value at 0.01 second and multiplying it by the time ($90^2 \times .01$ second $= 81$ amp^2-seconds). If the fuse co-ordination is critical in a particular application, the manufacturing tolerance should be factored into the current or time values used to determine melting I^2t.

The arcing I^2t of satisfactory current limiting fuses will not exceed twice the melting I^2t, and total clearing I^2t will therefore not exceed three times the melting I^2t. In the above example, maximum clearing I^2t will not exceed $3 \times 81 = 243$ ampere^2-seconds for the 30-ampere Form 101 Amp-Trap fuse. It is interesting to note that Chase-Shawmut specifies 240 ampere^2-seconds for this fuse. In practice, this type of approximation should only be used when specific I^2t data is not available from the fuse manufacturer.

The minimum I^2t rating of the semiconductor cell is specified by the semiconductor manufacturer. Depending on the cell design, the I^2t rating may vary with initial junction temperature and may depend on whether or not reverse voltage is impressed on the cell following the current surge.

Several companies manufacture current limiting fuses in various voltage, current and speed ratings. Their literature indicates the following ratings:

Fuse Manufacturer	Current Limiting Fuse Designation and Rating
Low Voltage Switchgear Dept. General Electric Company Philadelphia, Pennsylvania	*Class H "CLF" Fuses* 6 to 200 Amps, 250 V DC & AC (GF6A6 to GF6A200) 6 to 200 Amps, 600 V DC & AC (GF6B6 to GF6B200) 300 to 600 Amps, 250 V AC (GF7A300 to GF7A600) 300 to 600 Amps, 600 V AC (GF7B300 to GF7B600) *Class L "CLF" Fuses* 800 to 4000 Amps, 600 V AC (GF8B800 to GF8B4000) *Class J "CLF" Fuses* 3 to 600 Amps, 600 V AC (GF8B3 to GF8B600)
Bussmann Mfg. Division McGraw-Edison Company St. Louis 7, Mo.	*Buss KAW Limitron fuses* 1—30 Amps, 130 Volts *Buss GBB Limitron Fuses* 1—10 Amps, 130 Volts 12—30 Amps, 65 Volts *Buss KAA-KAJ Limitron Fuses* 1—2000 Amps, 130 Volts (KAA, KAH) 1—800 Amps, 250 Volts (KAB) 1—800 Amps, 600 Volts (KAC, KAJ)

Chase-Shawmut Co.
347 Merrimac Street
Newburyport, Mass.

Amp-Trap Fuses, Form 101
1—10000 Amps, 130 Volts
1—5000 Amps, 250 Volts
1—2000 Amps, 600 Volts

For data on the melting time-current and I^2t characteristics of these fuses, the designer should refer to the curves and data published by the fuse manufacturer.

When a current limiting fuse in the primary of a transformer must be coordinated with a semiconductor cell in the secondary, their respective I^2t's can be compared by the following equation:

$$I^2t_{fuse} \leq \left(\frac{V_{sec.}}{V_{pri.}}\right)^2 \times I^2t_{cell}$$

where $V_{sec.}$ = rated secondary voltage of transformer.
$V_{pri.}$ = rated primary voltage of transformer.

In similar manner, the clearing I^2t of a fuse being fed by a group of N parallel semiconductor cells should be no greater than N^2 times the I^2t rating of the individual cells if all the parallel cells share current equally. If the cells are derated for parallel operation to compensate for inequalities in current sharing, the relationship between clearing I^2t of the fuse and the I^2t rating of the individual cell can be expressed as follows:

$$I^2t_f \leq I^2t_c\ [N(1-S)+S]^2$$

where I^2t_f = clearing I^2t of fuse
I^2t_c = I^2t rating of semiconductor cell
N = number of parallel rectifier cells
S = derating factor for parallel cell operation (usually 0.20)

13.5 INTERRUPTED SERVICE TYPE OF PROTECTION

By inserting the protective device in the AC lines feeding the SCR's and diode rectifiers, protection can be provided both against DC faults and semiconductor cell faults if there is no possibility of DC feed into faults of the semiconductor cells themselves. DC feed into cell faults will occur in single-way circuits when other power sources feed the same DC bus or when the load consists of CEMF types of loads such as motors, capacitors, or batteries. The following is an example of this type of AC line protection in a circuit without current limiting impedance. Upon functioning of the protective system, the circuit is interrupted and shut down.

13.6 EXAMPLE OF FAULT PROTECTION (NO CURRENT-LIMITING IMPEDANCE)

Application: —120 V RMS AC supply, 60 cps
—Single-phase bridge employing two C35H SCR's for phase control in two legs and two 1N2156 diode rectifiers in the other two legs. See Figure 13.4.
—Maximum continuous load current = 12 amperes.
—Choke input filter.
—Line impedance negligible. Peak available fault current in excess of 1000 amperes.
—Maximum ambient = 55°C free convection. Each semiconductor mounted to a 4" x 4" painted copper fin $\frac{1}{16}$" thick.

Requirements for Protective System:

—Protection system must be capable of protecting SCR's and diodes against overloads, DC shorts, and shorting of individual semiconductors. System can be shut down when any of these faults occurs.

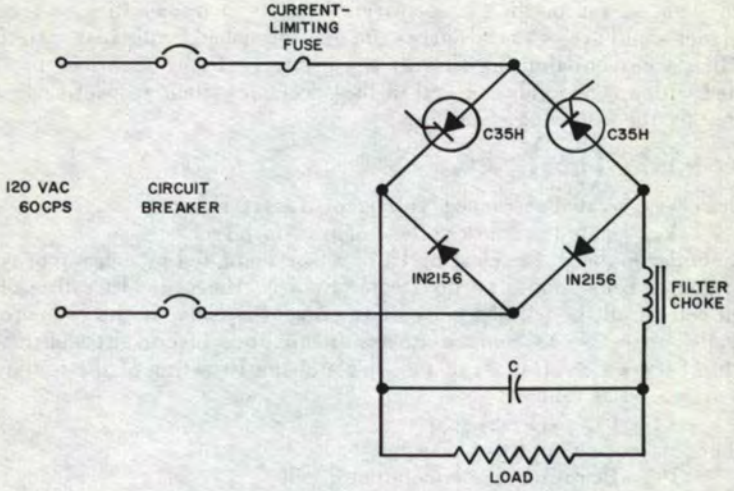


Figure 13.4 Circuit for Example of Fault Protection

Solution: —Since the current rating of the 1N2156 is higher than the C35 both at steady-state and under overload, the protection, if properly coordinated with C35, will be ample for protecting the 1N2156 also.

Using the data for a C35 on a 4″ x 4″ fin given in Figure 3.4 and the load current rating equation in Figure 3.7 (e) which applies for the continuous square wave of current experienced in a single-phase circuit with inductive load,

$$P_O = \frac{125-55}{\frac{0.0083}{0.0167}\times 5.1+\left(1-\frac{0.0083}{0.0167}\right)0.4-0.35+0.2}$$

$=27$ watts maximum peak heating allowable per SCR on steady-state basis

From the specifications for the C35, this level of heating will be developed by 18 amperes peak or 9 amperes average load current at 180 degree conduction angle with a rectangular current waveshape. Under inductive load conditions, the maximum steady-state RMS rating of the complete circuit is equal to the peak rating of each SCR = 18 amperes.

Assuming that faults and overloads will be superimposed on the steady-state equipment rating of 12 amperes, the semiconductor overload rating can be calculated from Figure 3.7 (f).

$$P_{OL} = \frac{T_J - T_A - P_{CD}R_T}{\theta_{(t)}} + P_{CD}$$

For example, for 10 seconds the SCR can dissipate the following power without its junction exceeding 125°C:

$$P_{OL} = \frac{125 - 55 - 8 \times 5.1}{2.2} + 8 = 21.3 \text{ watts/cell}$$

Average current rating per cell = 13.3 amps (from specification sheet).

Rated bridge output current = $2 \times 13.3 = 26.6$ amps RMS.

This point and others calculated by the same means are plotted on the co-ordination chart of Figure 13.5. Overload ratings achieved by this technique limit junction temperature to 125°C.

For non-recurrent types of overload as typified by accidental short circuits and failure of filter capacitors, the SCR is able to withstand considerably higher overloading as specified in the I^2t and surge current ratings. A typical point of this kind can be calculated as follows. At 0.1 second, a time which is equivalent to 6 cycles on the surge curve, the peak surge current rating of the C35 is 92 amperes.

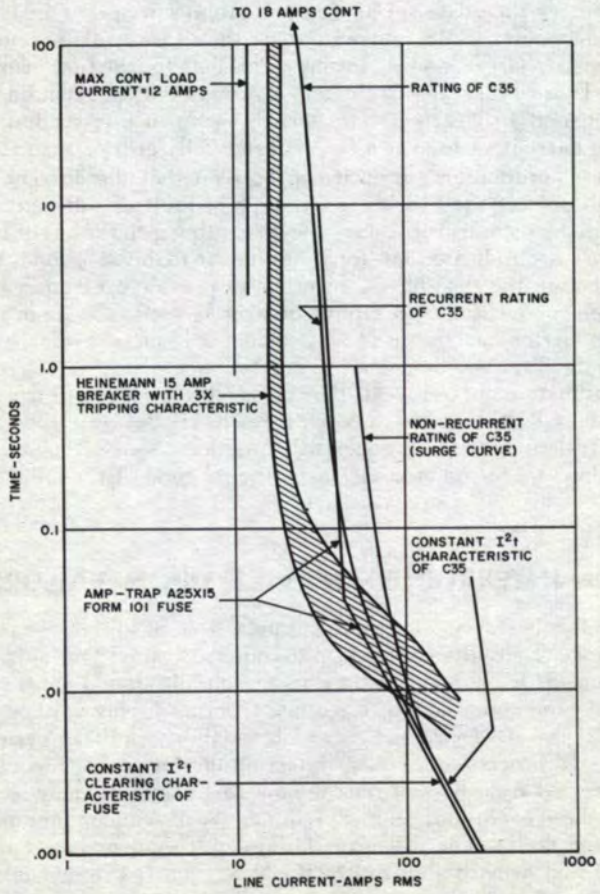


Figure 13.5 Co-ordination Curve for Example of Fault Protection of SCR's

The RMS bridge rating is $92 \div \sqrt{2} = 65$ amperes. This curve blends into ratings determined from the I^2t rating below approximately 50 milliseconds. The I^2t rating of the C35 is 75 amp^2-sec. At .001 second, the current rating of the SCR is $\sqrt{75 \text{ amp}^2\text{-sec.}/.001 \text{ sec.}} = 274$ amps. Below ½ cycle, the rating of a single SCR and the rating of the bridge are identical. Thus, at .001 second, the bridge is rated 274 amps RMS also.

To afford protection against short circuits of the load and shorted semiconductors in this type of circuit, a current limiting fuse is required. The fuse must carry the steady-state line current without melting. An Amp-Trap A25X15 Form 101 fuse rated at 15 amperes continuous current should handle the 12 amperes RMS steady-state line current satisfactorily. Melting characteristics of this fuse are shown in Figure 13.3, and are plotted directly on the co-ordination curve of Figure 13.5 since both curves are in RMS terms. Below 0.01 second, the fuse clearing characteristic can be determined on the basis of the fuse manufacturer's clearing I^2t data or on approximations from the melting time vs current curves as explained in Section 13.4. Since the manufacturer of the A25X15 fuse specifies a maximum clearing I^2t of 60 amp^2-seconds for this fuse, the data is translated into clearing current vs time data for the co-ordination curve. For instance, at 0.001 second the maximum RMS current that this fuse will permit to flow is $\sqrt{60 \text{ amp}^2\text{-seconds}/.001 \text{ second}} = 245$ amps. This data for the fuse below 0.01 second is plotted in Figure 13.5 and made very conservative by extending the straight line of the constant I^2t clearing characteristic up to its intersection with the published melting current vs time at a time substantially greater than 0.01 second.

From the co-ordination curve, it can be seen that the current limiting fuse in the line will protect the SCR's for any type of fault of sufficient magnitude to blow the fuse in 0.2 second or less since the fuse rating is to the left of the cell rating.

The curves also indicate that, for times longer than 0.2 second, the SCR's are likely to fail before the fuse blows. In order to provide protection for the SCR's for these lower current faults, a circuit breaker is used. The co-ordination chart shows the tripping characteristic of a Heinemann 15-ampere molded case circuit breaker using the Type 3X time-delay characteristic.

The co-ordination curve reveals that the circuit breaker will trip on any faults under 42 amperes RMS, but above 18 amperes RMS. Between 42 amperes and 85 amperes, the fuse and/or the breaker will function. Above 85 amperes, the fuse only should blow. Under no circumstances should good SCR's fail.

13.7 NON-INTERRUPTED SERVICE UPON FAILURE OF SCR

In the foregoing discussion and example, the SCR's are protected against overloads and short circuits of the output and also against the fault currents that occur if another SCR or diode rectifier in the circuit should short. Protection is afforded by disconnecting the entire rectifier from its supply voltage.

In some types of service such as high reliability military systems and continuous industrial processes, a service interruption due to a semiconductor failure cannot be tolerated regardless of how remote this possibility may be. To maintain service under these conditions requires redundancy of semiconductors and a means of disconnecting faulty cells whenever failure of a semiconductor occurs. It has been observed that, when failures of SCR's have occurred, they could be classified into three main categories:

1. Loss of reverse blocking ability. In rectifier circuits this generally causes a high fault current to flow.

2. Loss of forward blocking ability. In a rectifier circuit, this will generally result in loss of control of output voltage, the SCR remaining in the forward "on" state.
3. Failure to fire or switch into the forward conduction state. This will also result in loss of control of output voltage since the SCR will remain in the "off" state.

(Conditions 1 and 2 may be combined in a short-circuited device.)

Figures 13.6 and 13.7 suggest two of several possible methods of detecting and isolating defective SCR's from the circuit without interrupting the flow of controlled power to the load. Figure 13.6 illustrates a single-phase centertap phase-controlled power supply in which the SCR's in each leg of the circuit are grouped into pairs of parallel-matched cells. A low value of resistance R is connected in series with each SCR. The value of R is selected to limit fault current through good SCR's if one SCR loses its reverse blocking ability. The contacts of an isolating circuit breaker are connected in series with each pair of SCR's. The trip coil of each breaker or the coil of a pilot relay is connected across the bridge formed by the pair of SCR's and their respective series resistors. When both

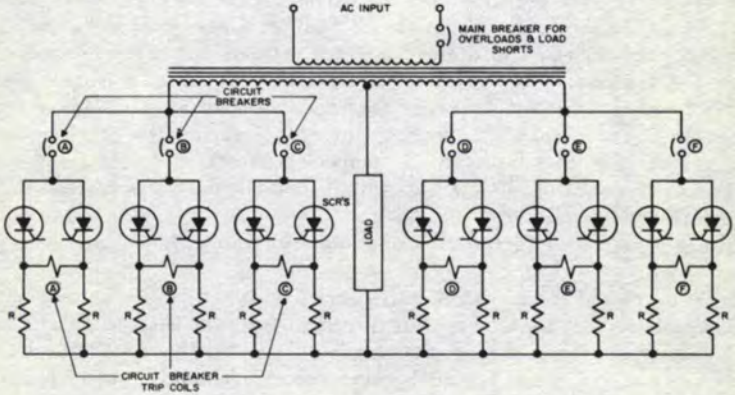


Figure 13.6 Parallel SCR Pairs for Non-Interrupted Service

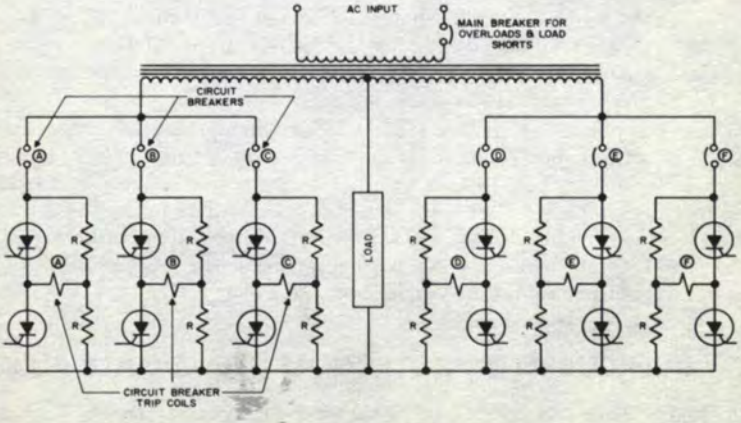


Figure 13.7 Series SCR Pairs for Non-Interrupted Service

SCR's of a pair are functioning properly and therefore identically, the instantaneous currents through the SCR's and their series resistors are essentially equal and therefore no current flows through the circuit breaker trip coil. If either SCR in a pair fails in any one or more of the three modes enumerated above, unequal currents will flow for at least part of each cycle through the SCR's. Current will flow through the trip coil associated with that SCR pair, tripping the series circuit breaker and isolating the pair from the main circuit. As long as the remaining SCR's in that leg of the circuit are capable of handling the full load current, the circuit will be capable of continuing operation indefinitely. The circuit breakers can be used to actuate an alarm or annunciator scheme to warn the equipment operator of the failure so that he can replace the faulty SCR during a scheduled maintenance shutdown of the equipment.

The circuit shown in Figure 13.7 is more economical than Figure 13.6 for circuits requiring high output voltages rather than high currents. In this circuit the SCR's are grouped in series-connected pairs for the purpose of handling higher voltages. A resistor R is connected in shunt with each SCR to assist in voltage sharing and to provide in conjunction with the pair of SCR's a bridge across which to connect the circuit breaker trip coil. When both SCR's are functioning properly, only the difference in leakage currents between the two SCR's flows through the trip coil. When either SCR in a pair malfunctions for one of the reasons cited earlier, a substantial current will flow for at least part of the cycle through the trip coil, thus opening the circuit breaker and isolating that pair of SCR's from the circuit. In order that the trip coil will reliably discriminate between the normal leakage balancing current of the SCR's and the unbalance current resulting from a faulty SCR, it may be necessary to reduce the value of each resistor R somewhat below the value otherwise adequate for forcing voltage sharing between the SCR's.

Proper functioning of the type of protection shown in Figures 13.6 and 13.7 requires that:

1. None of the circuit breakers in series with the SCR's should trip on DC overloads or faults. Separate protection in the AC or DC lines should disconnect the load from the supply voltage for this type of fault.
2. Adequate SCR and circuit breaker capacity should be provided to handle the maximum load current with one of the parallel paths removed from the circuit by operation of a breaker.
3. In isolating a pair of SCR's, the circuit breaker must cut off the current at a slow enough rate so that induced voltage (L di/dt) does not exceed the transient voltage rating of the SCR's in parallel with that pair. If they occur, excessive transient peaks may be reduced to tolerable levels by means of transient suppression techniques (Chapter 14.).

In some applications it may suffice to provide protection only against the possibility of SCR's and rectifier diodes failing by losing their reverse voltage blocking ability (shorting). In this event, the protective scheme can use current limiting fuses in simple parallel paths in a manner identical to that used for protecting diode rectifier circuits.[12] This type of protection presupposes that satisfactory operation can take place at least on a temporary basis with SCR's still in the circuit that have failed either by failure mode 2 or 3 above.

13.8 OVERCURRENT PROTECTION USING GATE BLOCKING

In many phase-controlled and inverter type circuits, the SCR's and other circuit components can be protected against overcurrent conditions by removing

the gate firing signal from the SCR's as soon as excessive current is detected in the circuit. In a phase-controlled system, this will result in fault interruption within one-half cycle after the gate signal has been interrupted since the line voltage reversal will commutate or turn-off the fault current. In an inverter type of circuit operating from DC without line commutation, the gate signal must be interrupted while the fault current is still low enough to be commutated by the circuit parameters.

Figure 13.8 illustrates a typical gate blocking circuit as applied to the phase controlled voltage regulator discussed earlier in Figure 10.1.

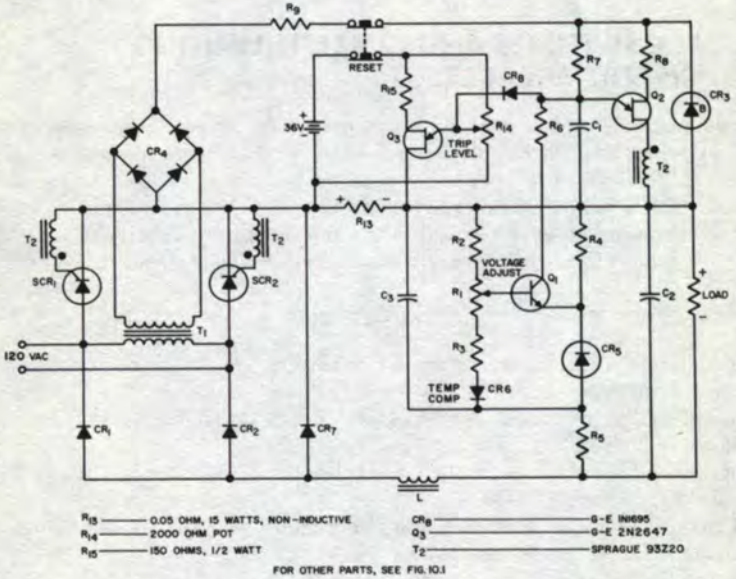


Figure 13.8 Phase Controlled Voltage Regulator with Overcurrent Trip

Under normal operation UJT Q2 develops firing pulses which are coupled to the gates of SCR1 and SCR2 through pulse transformer T2. The firing angle and therefore the average load voltage are controlled by the feedback action of Q1. It diverts charging current from C1, thereby regulating the charging rate of this capacitor and the firing angle of Q2. UJT Q3, a current sensing resistor R13, and associated components are added to the basic voltage regulator to provide the overcurrent protection feature. Q3 operates from a higher voltage DC supply than Q2 and has a higher standoff ratio than Q2. Q3 therefore fires at a higher emitter voltage than Q2. The voltage between the emitter and Base 1 of Q3 is composed of the voltage developed by the dividing action of R14 and the voltage developed by the flow of load current through the "looking" resistor R13. With no load current flowing, R14 should be adjusted so that the voltage on the emitter of Q3 is higher than the peak point voltage V_P required to fire Q2. Thus until Q3 fires, CR8 will be reverse biased and the normal regulating action of Q2 will occur.

If excessive current now flows in the load circuit, the emitter voltage of Q3 will rise with respect to Base 1 to the point where this UJT fires. Capacitor C1 will discharge through Q3 without developing a gate signal on the SCR's. The resistance between the emitter of Q3 and its positive voltage supply is low enough

that Q3 will remain in conduction and keep C1 from charging up again. Under these conditions, Q2 will deliver no firing signal to the SCR's and the load will be disconnected from the AC supply. If the "Reset" button is momentarily depressed, Q3 will return to its blocking state, and normal operation will resume provided the overcurrent condition has disappeared. If the fault still remains, Q3 will once more fire, thereby disconnecting the load from the supply, and preventing harm to the SCR's or other circuit components.

Similar gate blocking circuits for protective purposes can be devised for other types of SCR applications where the rate of rise of fault current is not excessive and where means for commutating this current are available.

13.9 SCR SWITCHES AND CURRENT-LIMITING CIRCUIT BREAKERS

SCR switches and circuit breakers may also be used for overcurrent protection systems. Several circuits that can be used for this purpose are discussed in Sections 7.2 to 7.9. For very high-speed protection of loads against overcurrent, the use of SCR's in electronic crowbar circuits like that shown in Fig. 7.10 shunts fault currents away from the load in a few microseconds. Interruption of the fault current is then performed by conventional means such as circuit breakers or fuses.

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14 Voltage Transients in SCR Circuits

In comparison with vacuum and gas tubes, semiconductor devices generally have lower voltage handling capabilities. This applies to SCR's as well as semiconductor diode rectifiers. Because of the sharp transition of their dynamic reverse resistance from a very high value to a very low value in the region of avalanche breakdown, and because of their low thermal capacity, these devices usually have little margin between the value of voltage which they can block satisfactorily in the reverse direction on a continuous basis, and the transient overvoltage which will destroy a cell by shorting in a matter of microseconds. SCR's manufactured by General Electric Co. carry a ¼ cycle nonrecurrent transient PRV rating that varies between 10 and 50% above the recurrent PRV rating, depending on the type. This additional PRV capacity is a valuable tool in designing reliable circuits.

As discussed in Section 3.8.4 the forward blocking characteristic of an SCR is self-protected by switching into the highly conductive state when the forward breakover voltage is exceeded except for those SCR's which have a peak forward voltage (PFV) rating. SCR's of this latter type that have very high values of forward breakover voltage may be damaged before anode voltage reaches the breakover voltage.

The likelihood and the severity of trouble-making voltage transients tend to be greater in SCR circuits than in simple power diode circuits because of the extremely fast switching action and the high commutating duty possible with SCR's. An understanding of the sources of transient voltages in circuits and the means of reducing them is therefore essential if optimum use of the ratings of SCR's and diode rectifiers is to be achieved.

14.1 WHERE TO EXPECT VOLTAGE TRANSIENTS

In the following discussion transients are considered to be those voltage levels which exceed the normal repetitive peak voltage applied to the SCR's. In the more common rectifier circuits operating from an AC source, the repetitive PRV applied to the semiconductors is equal to the peak line-to-line voltage feeding the circuit. In inverter circuits and other types of DC switches, the repetitive peak voltage applied to the SCR's is a function of the particular circuit and must be analyzed on an individual basis. Either or both forward and reverse voltage may change widely in normal circuit operation as load current, conduction angle, load power factor, etc., are varied.

In general, the effect of transient voltages on SCR's is similar to their effect on conventional silicon rectifiers, but it should be kept in mind that the SCR is capable of acting as a high resistance in the forward direction as well as the reverse. In some instances, this blocking action will prevent transient energy from being delivered to and dissipated in the load unless the SCR first breaks over in the forward direction.

In addition to random line disturbances such as lightning which have been recorded as high as 2600 volts on a 120-volt residential power line, transient voltages across SCR circuits may be generated by occurrences such as those described in Figures 14.1 through 14.8. The indicated diodes may be conventional rectifiers or SCR's.

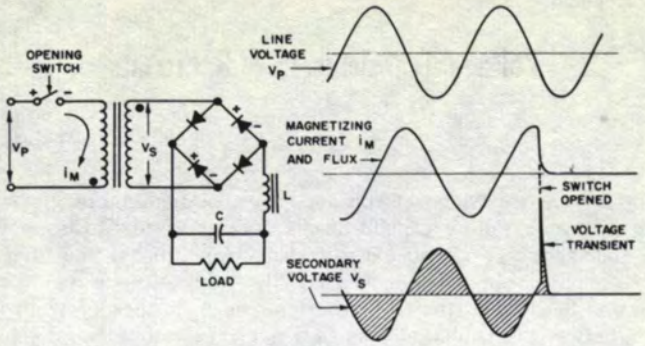

Figure 14.1 Voltage Transient Due to Interruption of Transformer Magnetizing Current

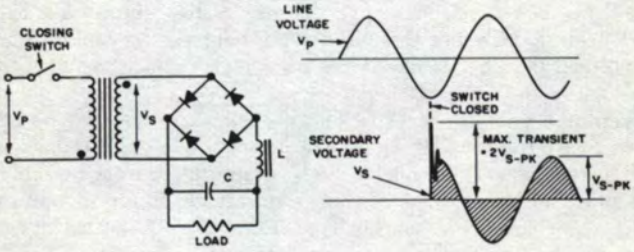

Figure 14.2 Voltage Transient Due to Energizing Transformer Primary

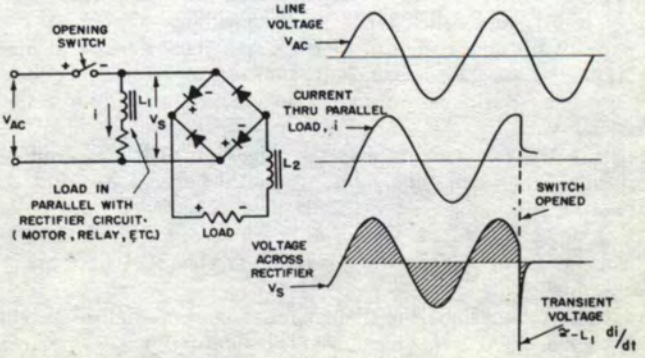

Figure 14.3 Voltage Transient Due to Switching Rectifier with Inductive Load Across Input

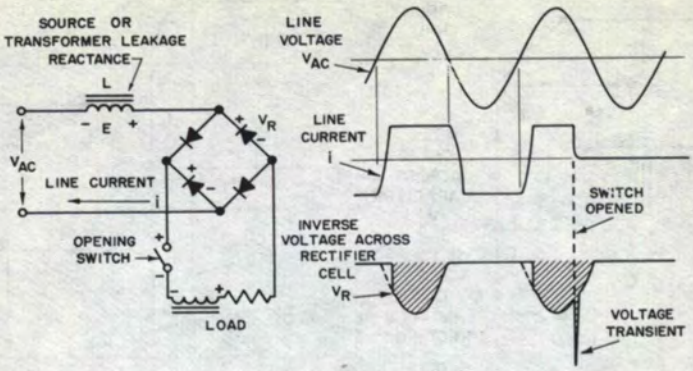

Figure 14.4 Voltage Transient Due to Load Switching

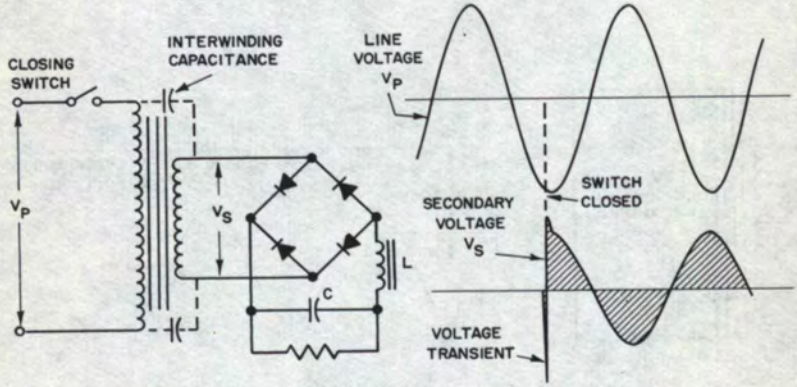

Figure 14.5 Voltage Transient Due to Energizing Step-Down Transformers

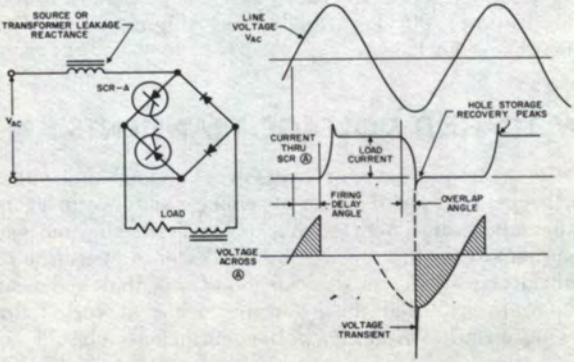

Figure 14.6 Cyclical Voltage Transients Due to Hole Storage Recovery Phenomena

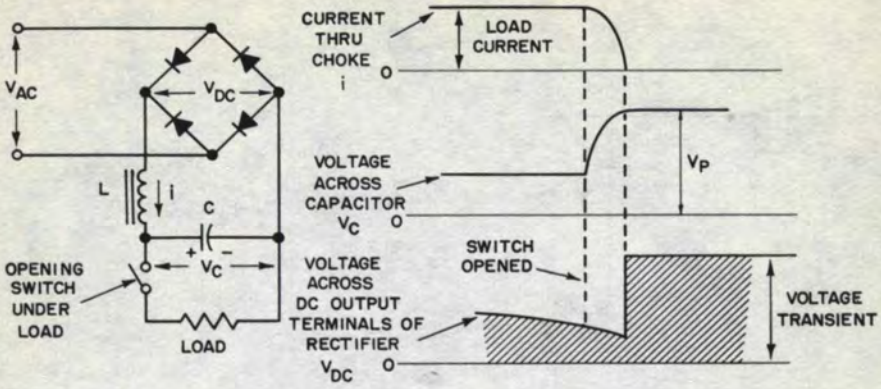

Figure 14.7 Voltage Transient Due to Dropping Load from El-Type Filter with High L/C Ratio

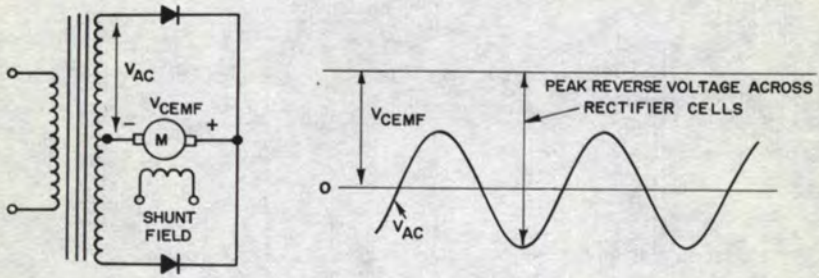

Figure 14.8 Overvoltage Due to Regenerative Load

Further details on these sources of voltage transients may be found in Reference 7 or in "Rectifier Voltage Transients: Their Generation, Detection and Reduction," Publication 200.11, available on request from General Electric Company, Auburn, New York.

14.2 HOW TO FIND VOLTAGE TRANSIENTS

Only too often the presence of excessive voltage transients in a rectifier circuit is first suspected because of a rash of semiconductor failures in the prototype equipment in the laboratory. Worse, yet, these first symptoms sometimes wait until the first equipment is shipped into the field where operating conditions may depart quite radically from the near-ideal conditions that had been successfully passed in the laboratory. When these failures occur at very light loads or immediately following circuit switching, voltage transients should be suspected as the culprit.

Since the search for, and measurement of, possible voltage transients in a circuit may destroy or at least permanently harm SCR's and diodes in the circuit,

the anode supply voltage should be reduced to about ¼ or ½ the normal level initially and then gradually increased as measurements indicate the absence or reduction of transients to levels that the semiconductors can withstand.

AC switching transients are usually worst at no load. Therefore, it may be desirable to test the circuit for this type of transient at no load with SCR's and diodes of a lower current rating substituted for the main cells in order to reduce the cost of cells that may be destroyed in the course of the test. Also, the higher blocking resistances of lower current cells will aggravate voltage transients and thus will generally make measurements and corrective measures conservative.

14.2.1 Meters

Except for very slow high energy transients, instruments with moving coils as their detecting and indicating means are almost useless in measuring transient voltages because of their high inertia and low input impedance. Of the several transient voltage problems discussed earlier, this type of meter may be useful only in measuring the amplitude of regenerative voltage transients such as those generated by a hoist motor being driven by an overhauling load.

14.2.2 Oscilloscopes

A high speed oscilloscope with long persistence screen is probably the most useful single tool for analysis of voltage transients. For significant results in detecting and measuring all the types of transients that may cause rectifier failure, the oscilloscope should have a transient response of at least 0.1 microsecond rise-time and be capable of writing rates in excess of ten million inches per second. The Tektronix 530 and 540 series meet this specification. A practical screen material is the P11 phosphor. The Hughes Memoscope, although it is handicapped by its relatively slow writing speed and rise-time, is very useful for recording the longer duration types of transients.

For looking at cyclical transients such as those due to recovery from hole storage effects as discussed in Figure 14.6, the use of a scope is straightforward. In this case, the sweep should be repetitive and synchronized with the power line. However, for nonrecurrent types of transients due to switching, more careful precautions are necessary. The scope should be equipped with a hood and for visual inspection the room should be darkened if possible and the eyes of the operator permitted to become accustomed to a low light level. For checking the amplitude of voltage transients visually, it is sometimes more effective not to use a horizontal sweep, but to use instead only the vertical deflection of the trace. Thus, the eyes can be focused on the precise part of the scope face where the transients will appear if and when they occur.

When a sweep is employed, it can be triggered by the transient itself or by some external means such as an extra contact or interlock on the circuit switch. By this latter means, the sweep can be initiated before the transient occurs and any doubt about missing an early part of the transient is eliminated.

The objectiveness of studying and measuring non-cyclical types of transients is enhanced if a photographic record is secured in addition to the fleeting image recorded in the mind by the human eye. In many cases, fast film such as Polaroid Pola-Pan Type 42 or 44 (exposure index 200 and 400, respectively) will catch traces that are not perceptible to the eye.

Circuits should be checked for possible destructive voltage transients by connecting the scope input directly across the SCR to be checked.

14.2.3 Peak Recording Instruments

Electronic peak recording instruments with a memory can be very useful in checking for transients when their occurrence is random and cannot be predicted. A simple, easy-to-build instrument of this type is described in a General Electric application note, "A Portable Transient Voltage Indicator for Semiconductor Circuits," 200.16, available upon request. A picture of this instrument is shown in Figure 14.9. This instrument is a "go-no go" type of device for indicating when a transient voltage exceeds the voltage level set on the dial. Accuracy is within 2% maximum setting for voltage pulses down to one microsecond duration. Battery operation increases flexibility of usage and provides continuous operation up to twelve days on one set of batteries. Variations of the basic unijunction-SCR circuitry of this Transient Voltage Indicator permit recording of the frequency of occurrence of voltage transients and the highest transient voltage over an extended interval. Ready-made instruments of this type can be purchased from manufacturers whose names will be furnished on request.

Figure 14.9 Transient Voltage Indicator

14.2.4 Spark Gaps

For high voltage systems, calibrated sphere spark gaps can be used to measure the crest values of transient voltages.[4,5] Current through the spark gap after it has broken down should be limited by a non-inductive resistance (at least one ohm per volt of test voltage) in series with the gap on the grounded side. Suitable overcurrent protective devices should be used to interrupt the power follow-through after the voltage surge has passed.

14.3 WHAT TO DO ABOUT VOLTAGE TRANSIENTS

One of the obvious solutions to the transient voltage problem with semiconductors is to provide additional PRV capability by using cells with higher voltage ratings or additional cells in series. This alone is usually not the most economical answer. Normally the best solution will lie in a reasonable safety factor of cell PRV (2–3 times the repetitive circuit PRV) combined with suitable steps to reduce the amplitude of the transients to this rectifier rating. In circuits using SCR's, economical protection of the SCR reverse characteristic against transients can be achieved by inserting a conventional diode rectifier in series with the SCR. Suitable shunting resistors should be used for voltage equalization. Their resistances should be in proportion to the rated PRV of the respective devices across which each is connected. Shunt capacitors may be necessary to equalize the effects of severe commutation.

The elimination or reduction of voltage transients in rectifier circuits entails in one form or another slowing down the rate of dissipation of stored circuit energy across the rectifier cells. To accomplish this, one has a number of alternatives:

a. Changing the location of the switching elements or the sequence of switching.
b. Changing the speed of current interruption by the switching elements.
c. Providing additional energy storage or dissipation means in the circuit.

An example of the first alternative is to perform switching in the transformer secondary rather than in the primary or load circuits. Since the primary must ultimately be opened, it may be possible to interlock this operation so that the rectifiers are disconnected from the transformer before the primary is opened.

A switch or fuse that does not interrupt or chop current too abruptly will in itself tend to limit transients to lower levels. This is the second alternative. This type of interrupting device will dissipate the stored circuit energy in its arc. The following list can be used as a guide in selecting switches for low recovery voltage. The list is based on laboratory measurements on samples of each type of switch on a 120-volt 60-cycle circuit. The switches are listed in the order of increasing recovery voltage.

a. Relays (lowest transients)
b. Circuit breakers
c. Snap switches (including microswitches)
d. Mercury switches
e. Vacuum switches (highest transients)

The third alternative entails any number of various schemes for storing and dissipating the circuit energy.

14.3.1 Capacitors

Capacitive filters are one of the more commonly used types of suppressors for low energy transients of the type shown in Figures 14.1 through 14.7. Filters of this type should be placed across the input lines to the rectifier circuit or across the rectifiers themselves provided proper precautions are taken to limit the peak discharge current when the SCR is triggered.

Figure 14.10 illustrates how the ripple voltage on a filter capacitor in an AC system may be reduced. By connecting the capacitor behind a double-way rectifier as shown in this illustration, a single capacitor is effective in filtering transients

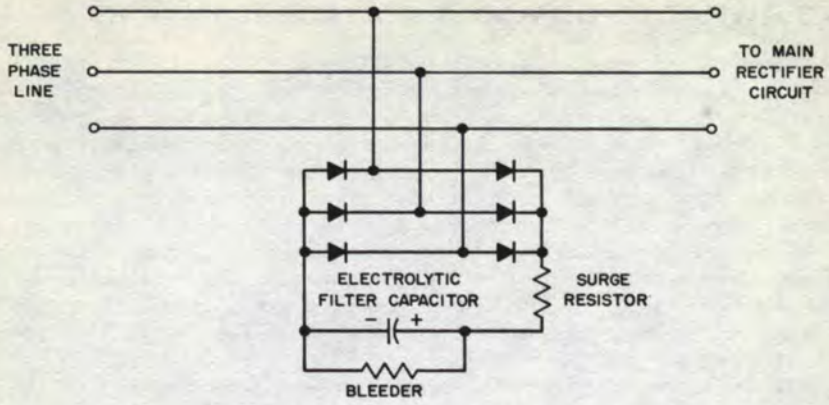

Figure 14.10 Use of Electrolytic Capacitors for Surge Suppression on AC Systems

that may occur between any of the lines in a three phase system. What would otherwise be 100% ripple voltage on the capacitor is reduced to approximately 5% and the economical energy storage capabilities of polarized electrolytic capacitors may be used to good advantage.

Filter capacitors over approximately .01 μfd may need series resistance to keep them from oscillating with distributed circuit inductance when shocked by a voltage wavefront. When capacitors are connected across the AC line this resistance should be in the order of 5 to 20 times the rated load resistance of the circuit. Final selection of resistance should be based on experimental optimization and the initial di/dt or switching current permitted by the SCR rating for the turn-on interval. Series damping resistance is also required in so-called "snubbing" circuits across SCR's for reducing hole storage recovery transients. For capacitors on the DC side of the rectifier, the series resistance should be large enough to protect the semiconductors against the inrush charging current to the capacitor when the circuit is energized initially. The cell manufacturer usually provides surge resistor selection charts for capacitor input filters of this type. The minimum resistance requirement is a function of the capacitance, the supply voltage, and the semiconductor characteristics (I^2t).

Since any inductance in series with the filter capacitor will reduce its effectiveness in suppressing transient voltages, care should be taken in selecting resistors with minimum inductance. Carbon resistors are favored over wire wound types, and capacitors with low self-inductance should be used for the same reason. Since the higher values of electrolytic capacitors may have considerable inductive reactance at high frequencies, it often is helpful to shunt this type with a high frequency type of capacitor (0.1-1.0 μfd) to handle these components of the transient.

The size of capacitor required for a particular suppression job is a function of many circuit parameters such as the load current level, the transformer characteristics, and the speed of interruption of switching. Thus it is difficult to predict with any degree of accuracy the optimum size of capacitance. As with the other means of energy storage and dissipation discussed in the following material, actual transient measurements on the prototype equipment will determine the optimum values of filter elements required.

The following equation has proved useful in selecting ample filter capacitance values for one of the most common and severe sources of transient voltages: opening the transformer primary under no load or with inductive load (Figure 14.1):

$$C = \frac{VA}{31\ f\ (V_{pk})^2}$$

where C = filter capacity in farads
VA = volt-ampere rating of transformer
f = supply frequency, cps
V_{pk} = peak transient voltage rating of each leg of the rectifier circuit

For evenly distributing the hole storage recovery voltage transient (Figure 14.6) across long series strings of SCR's and diodes, capacitors should be connected across individual cells. The required capacitor size depends on the difference in recovery time between rectifier cells. In any event, it need not exceed:

$$C = \frac{10\ I_f}{V}$$

where C = maximum capacitance to limit recovery transient within cell PRV rating, microfarads
I_f = amperes flowing through cell immediately preceding commutation
V = maximum continuous PRV rating of the cell, volts

This value is ultra-conservative and can often be reduced to a few percent of this by experimental optimization.

Capacitors across individual rectifier cells in long series strings are also used to distribute the effects of steep voltage waveforms impressed on the circuit. Because of capacitance between cells and ground, voltages with steep rates of rise would otherwise tend to "crowd" across those cells furthest from ground electrically.[3] Again, resistance in series with the individual capacitors is generally necessary to limit the peak current through the SCR when it is triggered.

14.3.2 Resistance

Ample resistive loading across individual legs of the rectifier circuit or across the AC input also provides a means for dissipating stored circuit energy without driving the voltage up to intolerable levels. Care must be taken to keep inductive effects in the resistors to a minimum so that they may dissipate high frequency components as well as lower ones. The disadvantage of the resistance loading approach is the inefficiency that it introduces to the over-all circuit since these resistors dissipate substantial energy at normal voltage levels as well as during transient occurrences.

In circuits where the rise-time of transient overvoltages is not excessive as in some regenerative types of load (Figure 14.8), a voltage sensitive relay may be used to connect a dynamic braking resistor when the DC bus voltage rises to a predetermined level, and to disconnect it when the overvoltage has subsided.

14.3.3 Thyrector Surge Voltage Suppressors

The introduction of Thyrector surge voltage suppressors by the General Electric Company has greatly reduced the transient voltage protection problem for power semiconductors. These compact non-linear resistances are essentially selenium "zener" diodes. In many applications they are far more economical and effective than the foregoing techniques of transient voltage suppression.

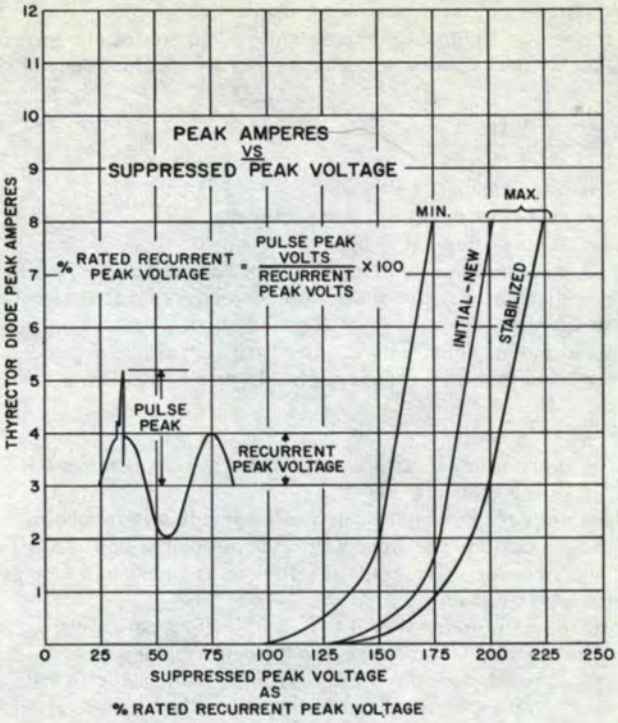

Figure 14.11 Thyrector Diode Characteristics at Ambient Temperature (6RS21 Cell) (—20°C to +100°C)

Figure 14.11 illustrates the voltage-current relationship of the one-inch-square Thyrector diode in an AC circuit. Below rated recurrent peak voltage, the Thyrector surge suppressor draws negligible current. However, as the voltage rises above this point, as would be the case under a transient condition, the Thyrector diode current increases rapidly and dissipates the transient energy. When correctly applied, Thyrector suppressors will generally clip transient voltages at 150 to 200% of the recurrent peaks. The one-inch square Thyrector diode is rated 25 volts RMS continuous. Cells are available in compact series assemblies for any multiple of this voltage. Other Thyrector diode sizes are available for suppressing various transient energy levels. Application notes and specifications are available on request.[10]

14.3.4 Controlled Avalanche As A Transient Voltage Suppressor

Controlled Avalanche characteristics in silicon rectifiers provide a very convenient means of minimizing or eliminating the effects of transient voltage in SCR circuits, often without the addition of separate surge suppressor components or substantial voltage safety factors. Introduced by General Electric in 1962, Controlled Avalanche rectifiers[9] have avalanche (zener) diode type reverse characteristics that provide built-in transient suppression.

While Controlled Avalanche silicon rectifiers have characteristics identical to conventional silicon rectifiers in the forward load current direction, special

design as well as special processing and testing insure reverse characteristics similar to those shown in Figure 14.12 for the A27 twelve ampere Controlled Avalanche rectifier. Maximum as well as minimum avalanche breakdown is rigidly specified for each voltage grade. Within its power dissipation capabilities, this type of rectifier can be operated continuously in the avalanche region, even at avalanche voltages well above 1000 volts. On a transient basis, these rectifiers can operate still higher in the avalanche region as defined by the reverse power surge curve of Figure 14.13. For instance, any A27 can dissipate 3900 watts of transient reverse energy for 10 microseconds. An A27 with an avalanche voltage of 1000 volts can therefore conduct over 3 amperes (3900 watts/1000 volts) in its reverse direction for 10 microseconds.

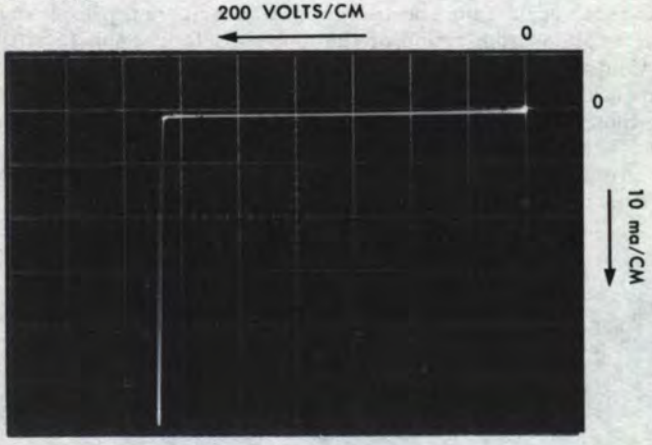

Fig. 14.12 Reverse Characteristics of A27 Controlled Avalanche Rectifier

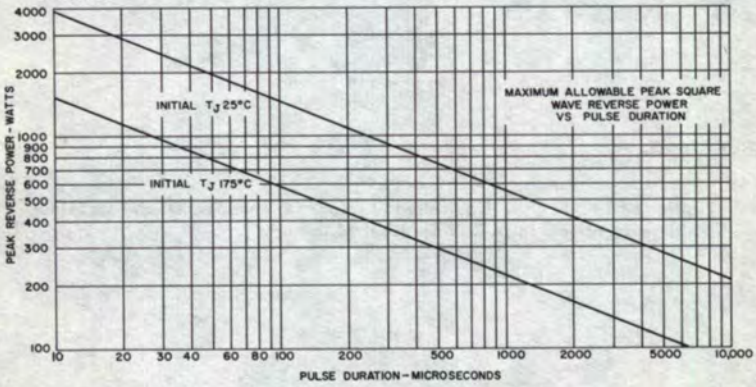

Fig. 14.13 Non-recurrent Reverse Power Surge Curve for A27 Controlled Avalanche Rectifier

Controlled Avalanche rectifier diodes are also available in several other forward current ratings extending from ½ ampere to 250 amperes continuous as indicated in Section 20. Detailed specifications are available on request.

Besides protecting themselves in the reverse direction against moderate levels of transient energy. Controlled Avalanche rectifiers can be used to protect other circuit components such as SCR's against overvoltage by virtue of their rigidly

specified maximum avalanche characteristics (Figure 14.12). For instance, the use of Controlled Avalanche rectifiers to perform the diode functions in the circuit of Figure 14.14 provides inherent suppressing action on voltage transients emanating from either the AC supply or the DC load provided the Controlled Avalanche devices have been properly selected and co-ordinated with the system and the SCR.

Controlled Avalanche rectifiers can also be connected directly across individual SCR's as transient suppressors although in many circuits each Controlled Avalanche rectifier can be used to protect more than one SCR. For example, Figure 14.15 demonstrates the use of two Controlled Avalanche rectifiers across an AC line to protect four SCR's in a non-freewheeling bridge from line voltage transients. An interesting aspect of this approach is that the Controlled Avalanche diodes will also protect the SCR's against unexpectedly high transient energy levels in excess of the normal energy dissipation rating of the diodes by failing short. In this abnormal case, the Controlled Avalanche rectifiers establish a short circuit across the AC input to the bridge, thereby blowing the line fuse and shutting down the circuit, but protecting the SCR's in the process. Controlled Avalanche rectifier diodes used as expendable overvoltage protective elements in this manner are often an economical means for protecting higher priced semiconductors, particularly where the magnitude, frequency, and energy of transient overvoltages are not known.

Low power Controlled Avalanche rectifiers can also be used as high voltage zener diodes in SCR trigger circuits to gate trigger SCR's before overvoltage reaches

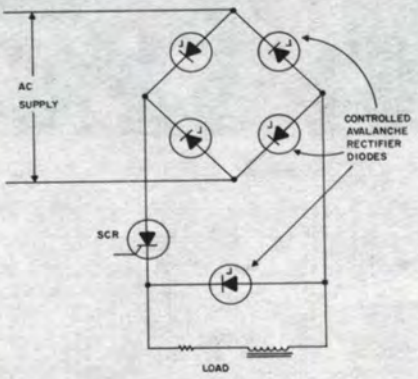

Figure 14.14 Use of Controlled Avalanche Rectifier Diodes to Limit Voltage Transients in SCR Phase Control Circuit

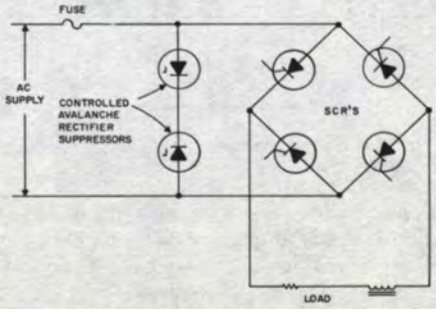

Figure 14.15 Use of Controlled Avalanche Rectifier Diodes to Protect SCR Bridge Against Line Voltage Transients

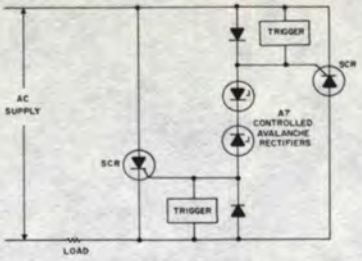

Figure 14.16 Use of Low Power Controlled Avalanche Rectifiers to Trigger SCR's on Overvoltage, Thereby Protecting the SCR's Against Excessive Reverse Voltage

damaging levels on their anodes. For example, the circuit in Figure 14.16 shows a back-to-back pair of SCR's used to phase control an AC load. Without suitable protection either SCR can be damaged in the reverse direction by excessive transient line voltage spikes if its companion SCR is not triggered in the forward direction. Addition of two Controlled Avalanche diodes selected so that their avalanche voltage occurs below the transient reverse voltage rating of the SCR's insures that neither SCR can be damaged by transient voltage of either polarity.

14.3.5 Miscellaneous Methods

Several other transient suppression means may be used to good advantage depending on the particular circumstances of the application. Spark gaps may be used in high voltage circuits provided the precautions outlined in Section 14.2.4 are maintained.[6] Silicon diodes can be used as discharge paths for the energy stored in inductive circuit elements such as generator fields and magnetic brakes. Electronic crowbar circuits of the type shown in Fig. 7.8 use the SCR to provide microsecond protection against overvoltage conditions for entire circuits.

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Interaction and Radio Frequency Interference in SCR Circuits

15.1 INTRODUCTION

Due to its inherently regenerative turning-on action, the SCR switches very rapidly. In common with other fast switching devices, the SCR tends to shock excite the supply line. Fast rates of rise of current cause voltages to be induced across the distributed inductance of the supply line; in the presence of distributed line capacitance, this causes a redistribution of charge on the supply line. Generally, the redistribution of charge will be oscillatory in nature and at a fundamental frequency determined by the parameters of the supply line. For common types of power distribution lines the fundamental frequency is usually between 250 kc and one or two megacycles per second. As such, the SCR may be considered as a generator of high frequency voltages which can give rise to radio interference or interact with other SCR circuits unless suitable steps are taken.

When acted upon by line disturbances, the SCR circuit may be considered as a receiver sensitive to high frequency voltages. Generally, these voltages act upon the anode of the device directly or they find their way into the trigger circuit. In either case an SCR may trigger spuriously and cause malfunction due to the operation of neighboring SCR circuits.

15.2 NATURE OF RADIO FREQUENCY INTERFERENCE (RFI)

Basically, two types of radio interference can be identified. One is conducted RFI and the other radiated RFI. In the former case, rf energy is transmitted along the power line and finds its way into other equipment. In the latter case, the equipment causing the interference acts as a small radio transmitter and "broadcasts" the interference which will interfere with other devices capable of "receiving" this energy (see Reference No. 1).

Another very common case related to conducted RFI, but appearing as radiated, is capacitive coupling into a conductor carrying rf energy. This latter form is particularly important where radios, including portable radios, are operated in an environment having rf carrying conductors in relatively close proximity. Residential applications are prime examples of this case.

The following military specifications set quantitative interference levels and give test procedures to which an equipment must be qualified if it is to conform to the specification:

MIL-I-6181D
MIL-I-26600 (150 kc and up) USAF
MIL-I-16910A (14 kc–1000 mc) Navy
MIL-I-11748B (14 kc–36000 mc) Army Signal Corps

15.2.1 SUPPRESSION OF RFI

RFI is an over-all systems problem, and it stands to reason that no one step by itself will necessarily eliminate or even satisfactorily attenuate it. The subject

must be approached from a systems point of view in which the location of the components, the manner in which they are mounted, the location of wiring runs, etc., must all be taken into account. This subject therefore does not lend itself to the establishing of a few simple quantitative rules to solve every conceivable situation. However, the following will give some approaches which have been found to be successful.

There are two major cases of systems circuitry. In one case an rf ground is not available at the equipment. An example of this is most residential wiring in which the neutral, even if it can be made available, is not necessarily a good rf ground.

The other case is where an rf ground is readily available. For example, a power supply may be self contained in a metal enclosure which in turn may be mounted in a metallic rack. Such a large expanse of metal can be considered an rf ground.

The basic approach, as far as the controlled rectifier is concerned, is to localize the initial high rate of rise of current to as small a section of the circuit as possible.

In this manner the effect of the SCR switching action on the distributed parameters of the supply line is minimized. With less shock excitation of the line the magnitude of the transient rf oscillations and their resultant effect (RFI) is reduced.

This can be done by appropriately placing in the circuit small inductors between which this rate of rise of current is to be localized. It is often of further help to add a small ceramic capacitor with minimum lead length to help supply charging current to the stray capacitance associated with the circuitry enclosed by the filter.

15.2.2 CONDUCTED RFI

Figure 15.1 shows an RFI suppression approach in a system *not* having an rf ground accessible.*

Figure 15.2 shows an approach in which an rf ground *is* accessible.*

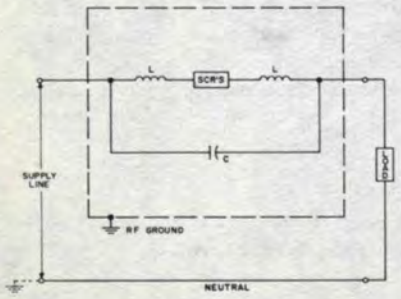

Figure 15.1 Conducted RFI Suppression With RF Ground Inaccessible

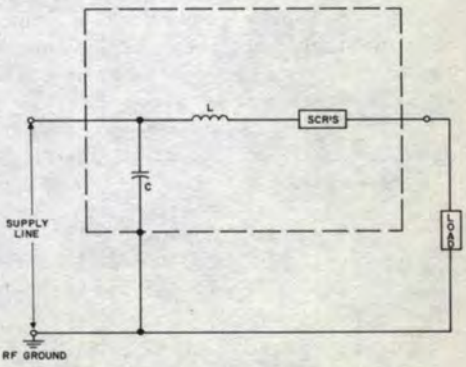

Figure 15.2 Conducted RFI Suppression With RF Ground Accessible

* These circuits were originally suggested by H. L. Gauper, Jr., of the General Electric Company.

The values of the components will depend upon the amount of suppression desired, the layout of the circuit, the nature of the supply line, the nature of the load, and generally the power level of the circuit. In a conventional 117 volt AC supply line and with a load under 1 kw the following values give a good starting point:

L = 60 μhenries (20 turns AWG 18 magnet wire on Arnold A-930157-2 molybdenum permalloy core, or 65 turns AWG magnet wire on 3 inch ¼" dia. ferrite rod)

C = 0.01 μf (ceramic disc)

It may be noted that the inductance need be in the circuit for only the few microseconds of the turn-on switching interval. For this reason the size of the inductor, even in high power circuits, will be quite small since the inductance may be allowed to saturate following the turn-on interval.

It is also of interest that the nature of operation of the SCR is relatively unimportant in connection with the generation of RFI. In other words, the same general considerations in suppressing RFI are equally valid in a phase controlled system as they are in an inverter or chopper system. It is generally found that the more conducted RFI is suppressed, the greater will be the radiated RFI. For this reason, it is not advisable to limit conducted RFI below levels required by applicable specifications.

15.2.3 RADIATED RFI

With regard to radiated RFI, the best approach to date has been electrostatic shielding. This is another good reason for confining the high rate of rise of current to as small a volume as practical. The dashed line in Figures 15.1 and 15.2 indicate the volume of the circuit that should be enclosed within the shielding. The shielding is then brought to a solid rf ground.

15.3 INTERACTION

Here the SCR system acts as a "receiver" of voltage transients generated elsewhere in the circuit. These transients act either (or both) on the SCR trigger circuit or directly on the anode of the SCR in the main power circuit. Interaction will cause the SCR system acted upon to completely or partially follow, or track, another SCR system. Also, various types of partial turn on, depending on the nature of the trigger circuit, have been known to arise. Elimination of interaction phenomena must take total system layout into consideration. Section 15.5 gives some general design practices which should be followed to minimize possible sources of interaction. Beyond good design practice in the system as well as in triggering circuits very specific steps for decoupling can be taken as outlined for UJT circuits in Section 15.4.

15.3.1 INTERACTION ACTING ON ANODE CIRCUIT

When an SCR circuit is acted upon with its gate circuit disconnected (open gate or terminated per specification bulletin) the nature of the interaction is usually attributable to a rate of rise of forward voltage (dv/dt) phenomenon. When energizing the circuit, such as by a contactor or circuit breaker, applicable dv/dt specifications for the device must be met. This subject is discussed in detail in Chapter 3. Once the circuit is energized the SCR will sometimes respond to high

frequencies superposed on the anode supply voltage. For example, a 1-megacycle oscillation having a peak amplitude of 10 volts has an initial rate of rise in the order of 60 volts per microsecond. Applicable specifications for the SCR must meet this condition or steps should be taken to attenuate the rate of rise of voltage.

Due to the nature of anode circuit interaction an SCR will rarely track another SCR circuit over the full control range of phase control. Usually, it will tend to lock in over a very limited range near the top of the applied anode voltage half cycle where the dv/dt is greatest. The best means of suppressing this type of interaction is to select an SCR with increased dv/dt withstand capability, to increase dv/dt withstand capability by means of negative gate bias, or, conversely, to reduce the rate of rise of positive anode voltage by suitable circuit means. The effect of negative gate bias on SCR dv/dt withstand capability and dv/dt suppression circuitry is discussed in Section 3.9. Often a combination of these steps yields the desired results. In addition, of course, good circuit layout and system practices should be observed as outlined in Section 15.5.

15.3.2 INTERACTION ACTING ON THE TRIGGER CIRCUIT

There are basically two cases to distinguish here:

1. The trigger circuit is acted upon from the supply line directly;
2. The trigger circuit is acted upon from the SCR gate circuit.

Both of these mechanisms may cause the trigger circuit to fire prematurely, giving rise either to spurious firing or complete or partial tracking of the SCR's in the circuit. The response of the trigger circuit to incoming transients will determine the degree of interaction, if any. There are no general rules for every type of trigger circuit. However, in the design of a trigger circuit it is well to take the possibility of interaction into account. The designer will be in the best position to assess the transient susceptibility and stability of his circuit.

When using the unijunction transistor trigger circuit there are a few relatively simple steps that can be taken to decouple these circuits against both supply voltage and SCR gate circuit transients. These methods are outlined in the following two sections.

15.4 DECOUPLING THE UJT TRIGGER CIRCUIT AGAINST SUPPLY TRANSIENTS

Depending on the nature of the particular circuit conditions, either one or a combination of the following will give effective decoupling against line voltage transients acting on the unijunction transistor trigger circuit:

1. Use of control (isolation) transformer with an RF filter across its secondary, if necessary;
2. Use of "boot strap" capacitor between base two and the emitter of the unijunction transistor;
3. Use of a Thyrector diode connected across the supply to the unijunction circuit.

The value of the "boot strap" capacitor C_1 should be chosen so that the voltage divider ratio of C_1 and C_2 in Figure 15.3(A) is approximately equal to the intrinsic standoff ratio of the UJT, or:

$$\frac{C_1}{C_1+C_2} = \eta \qquad (15.1)$$

If this condition is met, positive or negative transients on the unijunction supply voltage will not trigger the UJT.

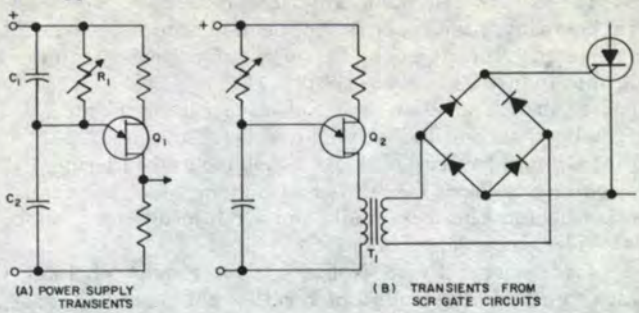

Figure 15.3 Circuits for Elimination of Erratic Firing from Voltage Transients in UJC Circuits

15.5 DECOUPLING UJT CIRCUITS AGAINST SCR GATE TRANSIENTS

Negative voltage transients appearing between the gate and cathode of the SCR's when transmitted to the UJT can cause erratic triggering. When transformer coupling is used, these transients can be eliminated by using a diode bridge in the gate circuit of the SCR as shown in Figure 15.3(B). Negative transients often arise in SCR gate circuits in forced-commutated circuits (see Chapter 5) and under certain conditions in AC phase control circuits.

15.6 GOOD DESIGN PRACTICES TO MINIMIZE SOURCES OF SCR INTERACTION

Radio frequency interference and interaction are both total system phenomena and no one step is necessarily the most effective in attaining the desired level of suppression. A combination of good system design practices, good circuit layout, good equipment layout, and, if necessary, a small amount of circuit filtering, as was outlined above, will suppress RFI to acceptable levels and eliminate various types of interaction phenomena.

When the following system considerations are met it is often unnecessary to take additional specific steps to filter trigger or anode circuits (Section 15.2) or use negative gate bias and dv/dt suppression circuitry (Section 3.7.5.):

1. Operate parallel and potentially interacting SCR circuits from a stiff (low reactance) supply line;
2. If supply line is soft (high reactance), consider using separate transformers to feed the parallel SCR branch circuits; each transformer should be rated no more than the required rating of the branch circuit load;
3. Avoid purely resistive loads operating from stiff lines—they give highest rates of current rise on switching;
4. Keep load moderately inductive—limiting rate of current rise on switching is in the direction of attenuating RFI and minimizing the possibility of interaction;
5. Keep both leads of a power circuit wiring run together—avoid loops that encircle sensitive control circuitry;
6. Arrange magnetic components so as to avoid interacting stray fields.

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Cooling the SCR

Successful application of SCR's depends to a great extent on adequate cooling of these devices. If junction temperature of an SCR rises high enough, permanent damage may occur in its characteristics and the device may fail by melting and thermal runaway. Circuits may fail before melting or thermal runaway in the SCR occurs since insufficient cooling can reduce the forward breakover voltage, increase SCR turn-off time, moving these and other SCR characteristics outside specifications sufficiently to induce circuit malfunction. For these reasons, all SCR's and diode rectifiers are designed with some type of heat transfer mechanism to dissipate internal heat losses.

16.1 LEAD-MOUNTED SCR'S

For small lead-mounted SCR's like the C5 and C8 series, cooling is maintained by radiation and convection from the surface of the case and by thermal conduction down the leads.

Several good common sense practices for minimizing the SCR temperature should be used when possible. Minimum lead length to the terminal board, socket, or printed board permits the mounting points to assist in the cooling of the SCR most efficiently. Other heat dissipating elements such as power resistors should not be connected directly to the SCR leads where avoidable. Also, high temperature devices like tubes, power transformers, and resistors should be shielded from radiating their heat directly on the SCR case. To increase heat dissipation of the standard TO-5 case, clip-on transistor radiators are available from a number of commercial vendors.

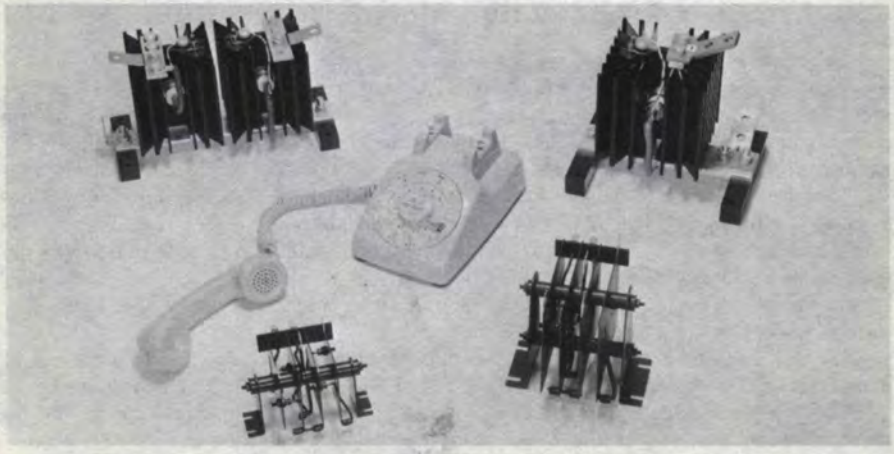


Figure 16.1 Typical General Electric Pre-wired SCR-Rectifier Stack Assemblies

Several of the General Electric SCR's in the TO-5 case are also available on a power transistor type of base for screwing to a heatsink or chassis. Directions for mounting these devices are given on the specification sheet for that type of SCR.

16.2 SCR STACK ASSEMBLIES

Higher rated SCR's are manufactured with a cooling fin in order to increase dissipation by radiation and convection. Figure 16.1 shows typical examples of General Electric natural convection cooled SCR's assembled into stack assemblies. Various fin sizes and configurations provide conservative cooling of each SCR type in the General Electric line. Literally tens of thousands of pre-wired circuit combinations are available, and associated diode rectifiers can be assembled integrally in the same stack. Detailed specifications are available on these SCR stack assemblies. They explain how these stacks can perform many useful functions in diversified applications.

16.3 MOUNTING THE STUD TYPE SCR

Because of space restrictions and other unique considerations, some applications cannot conveniently use SCR factory-assembled stacks. For these installations, the stud-mounted SCR is a particularly flexible component and has wide acceptance. This type of SCR uses a copper stud with a machine thread for making mechanical and thermal contact to a heatsink of the user's choosing. The heatsink itself may consist of a busbar, chassis, liquid cooling system, or a special cooling fin for dissipation of heat to the surrounding air.

If the heatsink is to perform an optimum cooling job, the semiconductor stud must be mounted not only in a good location on the heatsink, but also in such a manner as to achieve low thermal resistance to heat flow from the stud to the heatsink. Proper mounting is not always a straightforward simple matter. Several precautions should be considered.

16.3.1 Selection Of Heatsink Materials

Maximum cooling effectiveness calls for copper as the heatsink material because of its high thermal conductivity. However, cost considerations may dictate steel instead, and in some cases weight and ease of extrusion may bring aluminum into the picture. Two significant factors should be considered particularly for aluminum heatsinks.

Where moist or corrosive atmospheres will be expected, galvanic action between aluminum and the copper stud may lead to gradual deterioration of the joint, and an increase in thermal resistance. A good nickel or silver plate over the copper stud as provided on General Electric SCR's, combined with use of a corrosion inhibitor, such as Burndy-Penetrox A; Alcoa No. 2, or Penn-Union Cual-Aid, minimizes corrosion at this joint.

When mounting copper studs to a fin through a clearance hole by means of a nut on the backside, relaxation and metal creep may cause the mounting to gradually loosen. This condition is accelerated by temperature cycling and is dependent upon the magnitude of the time-temperature relation. As a consequence of this condition, the stud-fin contact thermal resistance will increase with time-at-temperature because of a loss of contact pressure. Tests have shown that after

1000 hours of operation, the stud-fin contact thermal resistance can increase as much as three times the initial value.

To minimize the effect of relaxation, which is common in any fastener under torque, it is recommended that a belleville spring washer be used between the nut and fin. A commercially availabe nut-belleville washer assembly, made by Shakeproof Corp., Elgin, Illinois, has been found to be satisfactory for maintaining the initial stud-fin contact thermal resistance. Tests using the ⅜, ½ and ¾ inch nut-washer assembly, Shakeproof numbers ND16470, ND16105, and ND16501 respectively, showed a 11 per cent maximum increase in the initial stud-fin contact thermal resistance after 1000 hours at 150°C.

Mounting straight threaded copper studs into a threaded hole in an aluminum fin is not recommended. Unequal temperature coefficients of expansion of aluminum and copper cause "thermal ratcheting." This tends to unscrew the copper stud from the threaded hole as the temperature cycles. The result is higher stud-fin contact thermal resistance.

Where a copper stud is screwed into a tapped hole in a copper heatsink, extreme care must be taken to assure that drilling and tapping are at right angles with the fin surface.

16.3.2 Hole And Surface Preparation For Fin Mounting

When studs with machine threads are mounted to thin flat fins through a clearance hole, optimum heat transfer depends heavily on adequate contact between the two surfaces. Care should be taken to insure a flat fin, free of ridges or high spots, particularly around the hole.

The fin surface under the semiconductor contact surface should be flat to within 0.001 inch per inch and have a surface finish of 63 micro-inches or less. If the hole is punched, the fin should be subsequently blanked. If the hole is drilled, the burr should be carefully removed. The hole size should be between 0.005 and 0.015 inch larger than the stud outside diameter. If the stud has a fillet where the thread meets the flat surface of the hex, the fin hole should be chamfered to prevent the stud from hanging up on this fillet. Before final assembly, the stud surface should be checked for removal of all burrs or peened-over corners that may have occurred during shipping and subsequent handling and that would otherwise cause reduced heat transfer across the surfaces.

Most fin surfaces have some treatment to aid radiation heat transfer and give corrosion protection. Copper fins are plated, painted, or ebnoled. Aluminum fins are generally painted or anodized. The fin surface under the semiconductor contact surface must be free of paint, anodization, or ebnol to give minimum contact thermal resistance. While plating in this area does not have to be removed, excessive oxides should be removed.

16.3.3 Mounting Torque

Good thermal contact between the semiconductor and the heatsink requires adequate pressure between these two surfaces as applied by torque on the threads of the device. However, torque beyond a certain point no longer improves the thermal contact and may mechanically stress the SCR junction and materials soldered or brazed to the stud inside the housing. Permanent damage to the device characteristics may result. For this reason, precise adherence to the manufacturer's

torque recommendations is necessary, and a torque wrench should *always* be used in mounting this type of semiconductor. Table 16.1 lists recommended mounting torques for the General Electric line of stud-mounted SCR's and diode rectifiers.

The recommended torques are for clean, dry threads. Also, on semiconductors with a 3/8-24 stud or larger, the torque is applied on the nut while holding the semiconductor stationary.

Torque wrenches, such as those made by the P. A. Sturtevant Company, should be chosen for the accurate range of torque that is to be used on a given rectifier.

16.3.4 Lubrication Of Joint

Any practical thermal joint will have trapped air pockets in the inevitable

Stud Size	Hex Size Across Flats	Typical Max. Recommended Torque (in lb.) (For exact values see spec sheets)	Effective Hex Diameter (Inches) d	Stud Contact Thermal Resistance* (°C/Watt)			
				Metal to Metal		With 0.005" Mica Insulation	
				Dry	With Penetrox	Dry	With Penetrox
10-32 NF	7/16"	15	0.46	0.75	0.60	6.5	6.0
1/4"-28	9/16"	30	0.59	0.45	0.35	4.0	3.5
1/4"-28	11/16"	30	0.72	0.30	0.25	2.5	2.2
3/8"-24	1-1/16"	100	0.91	0.15	0.10	—	—
1/2"-20	1-1/16"	150	0.91	0.10	0.09	—	—
3/4"-16	1-1/4"	300	1.20	0.06	0.05	—	—

* Values apply for studs tightened down with maximum recommended torque to reasonably smooth, flat surfaces by means of nut and clearance hole mounting. Thermal resistance values are stabilized values from studs to point on fin at diameter d.

Table 16.1 Characteristics of Standard Stud Sizes

depressions and voids between the surfaces. Since air is a relatively poor thermal conductor, the thermal transfer can be improved by applying a thin layer of Penetrox 'A,' made by the Burndy Corp., to the contact interfaces before joining. Care should be taken not to get the joint compound on the stud threads. Also, be sure there are no foreign objects in the compound, such as brush hairs. Table 16.1 indicates the improvement in thermal resistance that can be expected for typical stud sizes by use of silicone grease. Use of a tin/lead washer between stud and heatsink has also reportedly improved heat transfer and uniformity of this joint.

16.3.5 Electrical Insulation Of Stud From Heatsink

In some applications it is desirable to electrically insulate the stud from the heatsink. Hardware kits for this purpose are available for stud-mounted semiconductors with machine threads in the low and medium power ratings. These kits generally employ a .003 to .005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between the surfaces. As evidenced by the data in Table 16.1, the thermal resistance of the joint may be raised as much as ten times by use of this insulation. As in the direct metal-to-metal joint, some improvement in thermal resistance can be made by using lubricant on each side of the mica.

Tests using berillium oxide (99 per cent) for electrical insulation has shown this material to be excellent in heat transfer. Insulating a semiconductor with a ½-20 stud, using BeO (99 per cent) washers (1.00 inch OD x .52 inch ID x .125 thk) gave a stud-fin contact thermal resistance of 0.14°C/watt. Applying Penetrox 'A' to all contact surfaces decreased that thermal resistance to 0.1°C/watt.

Berillium oxide washers in large, formed sizes and small quantities are basically expensive items. However, careful consideration should be given to the over-all economics before using any other material when electrical insulation is required. Several standard washer sizes are available from companies such as National Berillium, Frenchtown, or Brush Berillium Company.

16.4 MOUNTING THE PRESS-FIT SCR

Certain sizes of SCR's such as the C22 as well as silicon rectifier diodes like the A44 are available in the so-called "press-fit" package which is designed primarily for forced insertion into a slightly undersized hole in the heatsink. When properly mounted this type of SCR has a lower thermal drop to the heatsink than the stud type mounting. Also, in high volume applications the cost of this type of mounting is generally less than that for the stud type of SCR.

16.4.1 Press-Fitting Procedure

The following simple procedures should be followed when press-fitting SCR's like the C22:

1. Heatsink materials may be copper, aluminum, or steel in order of preference. The heatsink thickness should be a minimum of ⅛ inch, the width of the knurl on the housing.
2. The hole dimensions are shown in Figure 16.2. The hole may be punched and reamed in a flat plate or extruded and sized in sheet metal. A slight chamfer on the hole should be used to guide the housing.

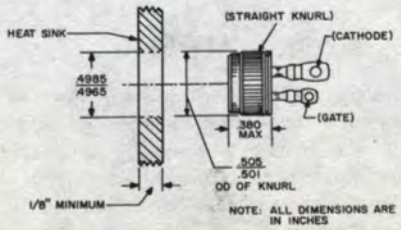


Figure 16.2 Mounting of C22 Press-fit SCR

3. To insure maximum heat transfer the entire knurl should be in contact with the heatsink. The unit must not be inserted into the heatsink past the knurl. This is to prevent the header from taking pressure off the knurl in a deep hole.
4. The insertion force must be limited to 800 pounds. This is to prevent misalignment with the hole and/or excessive unit-to-hole interference. Pressure must be uniformly applied to the face of the header as shown in Figure 16.3.

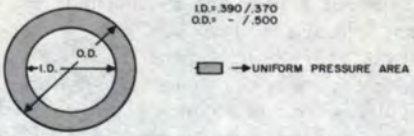


Figure 16.3 Area of Applying Pressure to C22 SCR

If the device is inserted in the above prescribed manner (using a copper heatsink), the thermal resistance, case to heatsink, will be less than 0.5°C/watt. The insertion is generally accomplished by means of a hydraulic ram. Reading the pressure and knowing the piston area, one can pre-set the maximum insertion force. Another possible insertion method which is simple to employ, but which gives no provision for measuring insertion force, is accomplished by the use of two blocks of wood and a bench vise as shown in Figure 16.4.

There are commercially available heatsinks specifically designed to accommodate press-fit devices. One such is a radial fin semiconductor cooler (NC-300-R series) manufactured by Wakefield Engineering Inc. These coolers are available in different sizes with hole accommodation for one or two press-fit units. The hole is the proper size for the C22 as well as for the A44 silicon rectifier.

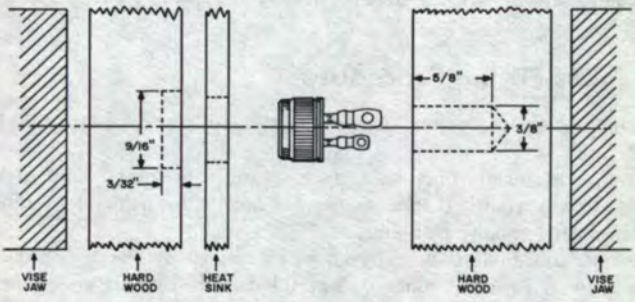


Figure 16.4 Use of Vise to Insert Press-fit SCR

16.4.2 Mounting By Other Methods

Several other mounting methods for press-fit devices are possible. Different types of mountings will demonstrate different thermal characteristics and in a good many cases the characteristics will not be readily predictable from theory. Figures 16.5(a) through (d) show mounting techniques whereby the SCR (or diode) is held by a clip and the clip is mounted on a heatsink. The size of the heatsink shown is not indicative of the size required but is intended to show only the mounting technique.

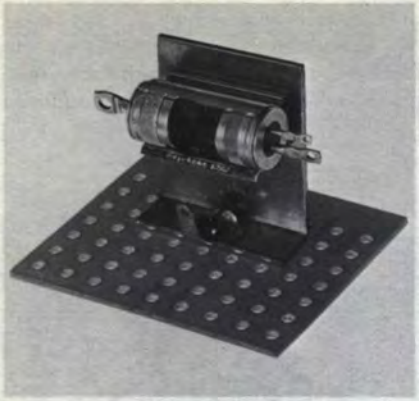


Figure 16.5(a) Augat* Clip No. 6014-46AN (Θ_{C-S}=10.1°C/watt)

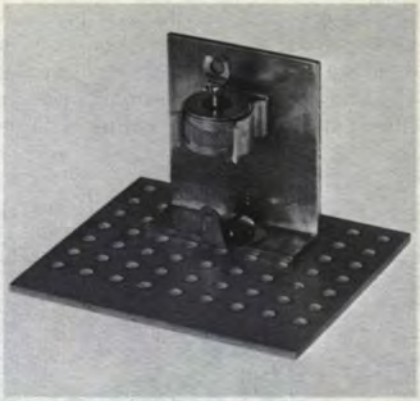


Figure 16.5(b) Augat* Clip No. 6003-39C (Θ_{C-S}=8.7°C/watt)

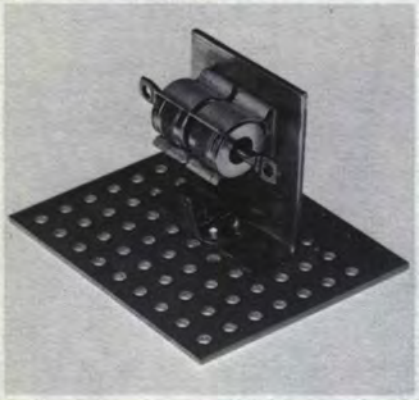


Figure 16.5(c) Augat* Clip No. 6003-24C (Θ_{C-S}=7.6°C/watt)

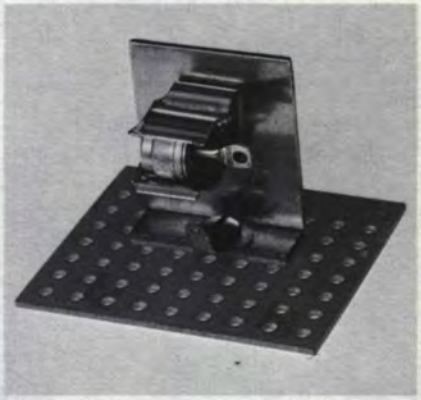


Figure 16.5(d) 30 Amp, 250 Volt Fuse Clip (Θ_{C-S}=6.4°C/watt)

Figure 16.5 Clip Mountings

Inasmuch as case-to-sink thermal resistance is at least an order of magnitude greater than in the press-fit configuration, the techniques shown in these figures have only limited possibilities for application. Cases where these types of mountings can be used are where operation is considerably below the maximum rated conditions, where the SCR is subject to intermittent or pulsed loading, or where cooling conditions (i. e. low ambient temperature, forced convection cooling, etc.) are sufficient to compensate for the high case to heatsink thermal resistance.

The mountings in Figures 16.5(a), (b), and (c) use commercially available clips and are shown in order of decreasing thermal resistance (case-to-sink). The clip in Figure 16.5(a) is nickel plated steel while those of Figures 16.5(b) and (c) are silver plated beryllium copper. As one would expect, the copper provides the better heat transfer. Figure 16.5(d) shows a mounting employing a 30 ampere, 250 volt fuse clip. Approximate values of the case-to-sink thermal resistance are given under each figure.

* Augat Inc., 33 Perry Avenue, Attleboro, Massachusetts

Figures 16.6(a), (b), and (c) show mounting techniques which exhibit better heat transfer than those previously outlined. This difference is primarily due to pressure which can be exerted on the device by tightening the mounting screw. The figures are again in order of decreasing thermal resistance. Clamps employed should have an interior radius of ¼ inch.

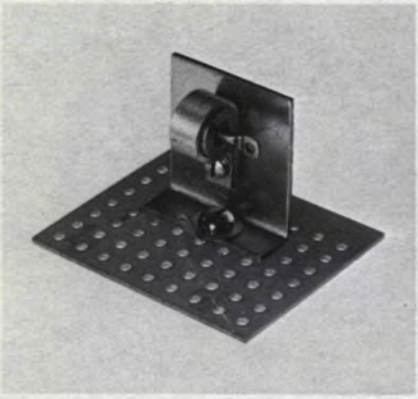


Figure 16.6(a) Mounting Employing Circular Cable Clamp (θ_{C-S}=4.0°C/watt)

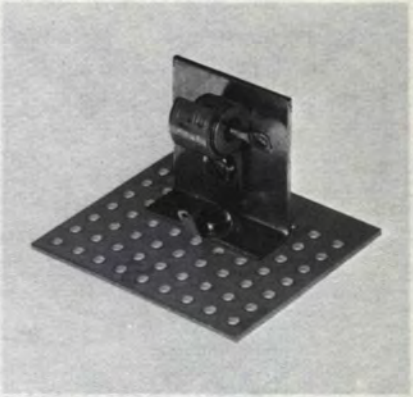


Figure 16.6(b) Single Clamp (θ_{C-S}=1.7°C/watt)

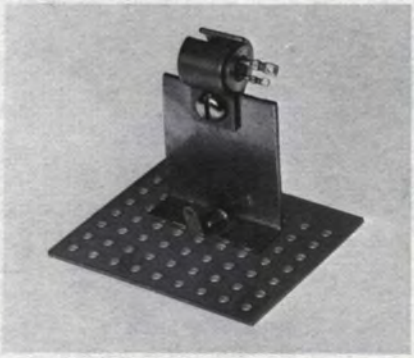


Figure 16.6(c) Dual Clamps (θ_{C-S}=0.8°C/watt)

Figure 16.6 Clamp Mountings

Figure 16.7 shows other methods of mounting the press-fit SCR.

The flexibility of the phenolic insulator prevents the application of high pressure between case and heatsink without fracturing the phenolic. It is recommended that a thin layer of silicone grease or Penetrox A compound be applied between case and heatsink. As in the case of stud mounted types this reduces thermal resistance considerably.

Figure 16.7(a) Dual Diode Mounting
(θ_{C-S}=1.2—2.2°C/watt)

Figure 16.7(b) Full Wave Bridge
Using A44 and A45 Dual Diode Sections

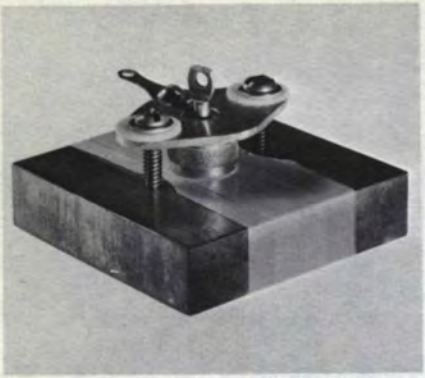
Figure 16.7 Other Press-fit Mountings

All mounting techniques outlined so far require the heatsink to be at case potential. Figure 16.8 shows approaches which can be employed where electrical insulation is required between the heatsink and the SCR. Figure 16.8(a) shows a press-fit diode mounted to, but electrically insulated from a copper heatsink. Again the size of the heatsink is for demonstration only and not indicative of the size which may be required. The insulating agent is a strip of lubricated insulating tape. The hold-down mechanism is a small copper plate which is insulated from the mounting screws with teflon washers and to which power connection can be made as shown.

Three types of insulating tape have been tested: teflon, mylar and polyethyene. Four mils of all insulations were able to withstand in excess of 1.7 kv with each mounting having an approximate thermal resistance of 1.0°C/watt/mil of thickness.

Figure 16.8(b) shows mounting using an ordinary hardware store epoxy adhesive. In order to obtain a reliable electrical insulator a small glass frit (glass powder such as Corning No. 45 Pyroceram) of 2 to 6 mil size is mixed with the epoxy resin-hardener compound. The epoxy and glass are mixed approximately one-to-one.

Two methods of mounting with epoxy are shown: one where the device is attached directly to the surface of the sink and one where the device is placed into a milled hole where heatsink thickness permits. The approximate thermal resistances (case-to-sink) are respectively 3.00 and 0.60°C/watt. Each technique requires about .05 cubic inches of epoxy-glass compound. *All surfaces must be thoroughly clean.* The compound is placed on the sink and the device is pressed down with hand pressure (approximately the same amount of effort as is required to remove a bottle cap). The pressure must be applied slowly, evenly, and firmly in order to allow the compound to run uniformly. The semi-toroidal bead which is squeezed out around the device is quite important in order to prevent arc-over between case and heatsink. It is important not to place too much pressure on the device when forming the bond inasmuch as this will crush the small glass particles and thus have a detrimental effect on the voltage capability. The curing time of the adhesive appears to be unaffected by the insertion of the glass and as such the



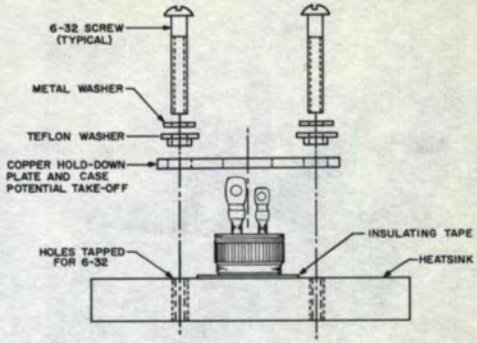
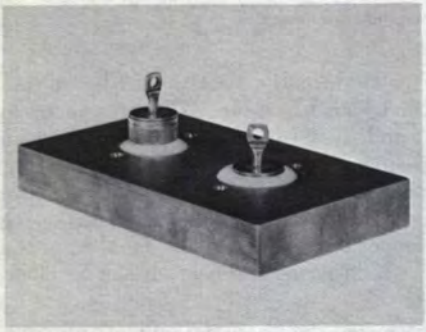
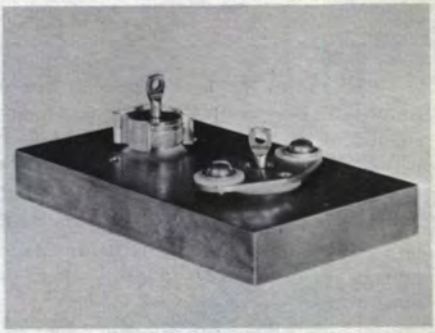


Figure 16.8(a) Tape Insulator





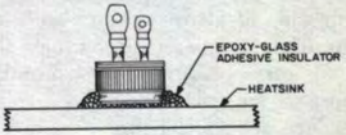


Figure 16.8(b) Epoxy and Glass Insulator

Figure 16.8 Insulated Mountings for Press-fit Rectifiers and SCR's

epoxy manufacturer's instructions can be followed in this regard. In using the mount-in-hole technique a small hole must be made in the center of the cavity, through the sink, in order to prevent air-pocketing and thus increased thermal resistance. The diameter of the milled hole should be twice the maximum frit size plus .505 inches; the practical limit on depth is about ¼ inch.

Power connections to the case can be made by using a copper cover plate similar to that employed with the tape mount. Since the device is firmly attached to the heatsink, a simple clip as shown in the photo can also be used. If it becomes necessary to make electrical connections to the case by means of a solder connection, the following precautions should be taken:

1. A 60–40 (tin-lead) solder should be used.
2. Solder temperature must be kept below 200°C.
3. The heat source should be removed as soon as the solder flows.

16.5 COOLING FIN DESIGN

The most common means of cooling stud-mounted SCR's is to mount them to a metallic cooling fin. Heat losses at the junction of the semiconductor will then flow down through the stud, into the fin, and will then be dissipated to the ambient air by radiation and either free or forced convection heat transfer. Because the mechanisms of radiation and convection are of distinctly different nature, the so-called heat transfer coefficient (h) for each effect must be calculated separately

Symbol	Definition	Dimensions
A	Surface Area of Fin	$in.^2$
c	Thermal Capacity	watt-sec/lb. °C.
h	Heat Transfer Coefficient	watts/$in.^2$°C
k	Thermal Conductivity	watts/°C-inch
L	Length of Fin (in specified direction)	inches
q	Rate of Heat Flow	watts
T	Temperature	°C
ΔT	Temperature Difference	°C
T_S	Surface Temperature of Heatsink	°C
T_A	Ambient Temperature	°C
V	Air Velocity	ft./min.
ϵ	Radiation Surface Emissivity	–
η	Fin Effectiveness	–
θ	Thermal Resistance	°C/watt

Table 16.2 Basic Thermal Units

and combined with the fin effectiveness (η) to determine the over-all heat transfer coefficient if any degree of confidence is to be placed in the analytical design. The rate of heat flow, q, from the fin to the ambient air can be expressed as follows:

$$q = hA\eta\Delta T \qquad (16.1)$$

where h = total heat transfer coefficient of the fin
A = surface area of the fin
η = fin effectiveness factor
ΔT = temperature difference between hottest point on fin and ambient

Table 16.2 lists these and other symbols used in the following discussion together with their dimensions.

A short discussion on each of the major factors in Equation 16.1 will reveal the variables on which they depend. The examples cited all apply to the same size fin and temperature conditions so that the reader can compare the relative magnitude of each of the various mechanisms of heat transfer.

It should be emphasized that while the individual equations are quite accurate when the conditions on which they are based are fulfilled in detail, the practical heatsink design will depart from the conditions to some extent because of local turbulence in the air due to mounting hardware and leads, thermal conduction down the electrical leads and the mounting for the fin, nearby radiant heat sources, chimney cooling effects caused by other heated devices above or below the cooling fins, etc. Fortunately most of these additional effects enhance rather than reduce the heat transfer. Therefore, it is common practice to disregard these fringe effects in the paper design stages except where designs are being optimized to a high degree. Even in a highly optimized design, precisely calculated values may be subjected to substantial corrections when the design is actually checked in the

prototype. The final measure of the effectiveness of the cooling fin will always be the stud temperature which should never be allowed to exceed the manufacturer's rating for a given load condition.

16.6 RADIATION

For stacked fins with surface emissivity of 0.9 or more and operating up to 200°C, the radiation coefficient (h_r) can be closely approximated by the following equation:*

$$h_r = 1.47 \times 10^{-10} \epsilon (1 - F) \left(\frac{T_S + T_A}{2} + 273 \right)^3 \frac{\text{watts}}{\text{in.}^2\text{°C}} \qquad (16.2)$$

where ϵ = surface emissivity (see Table 16.3)
F = shielding factor due to stacking ($F = 0$ for single unstacked fins)
T_S = surface temperature of cooling fin (°C)
T_A = ambient temperature (°C)

Table 16.3 indicates the wide variation in emissivity for various surface finishes. In free convection cooled applications, the radiation component of the total heat transfer is substantial, and it is therefore desirable to maximize radiation heat transfer by painting or anodizing the fin surface.

Note that oil paints regardless of color improve surface emissivity to practically an ideal level (unity).

Figure 16.9 presents Equation 16.2 in the form of a nomogram which considers the detrimental effects of stacking cooling fins. As fin spacing is reduced shielding effects become more marked, and radiation heat transfer is reduced,

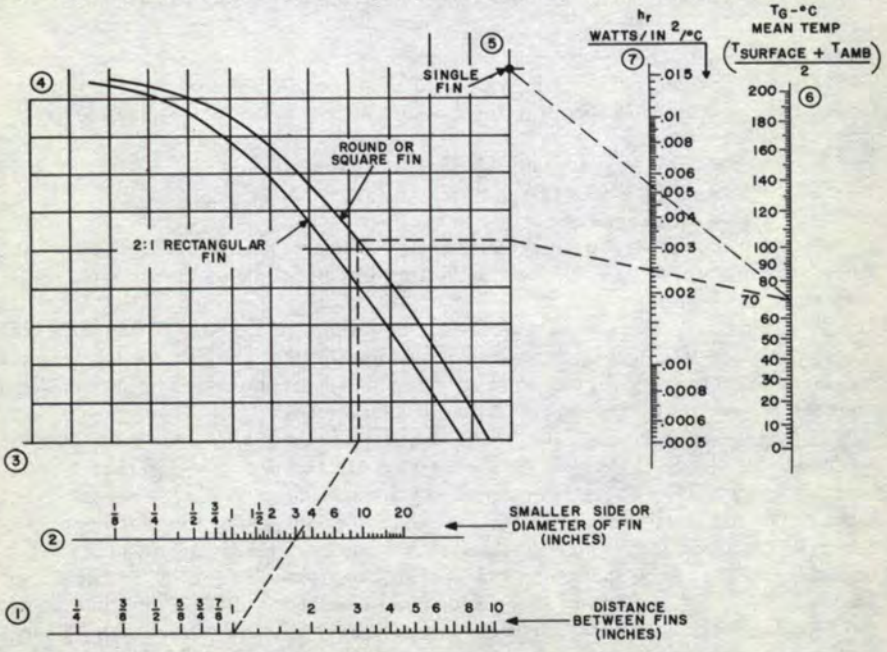


Figure 16.9 Radiation Nomogram (Emissivity=0.9)

* This equation can be derived from Equations 31-3 and 31-90 in Reference 1.

Surface	Emissivity (ε)
Anodized Aluminum	0.7–0.9
Commercial Aluminum (Polished)	0.05
Aluminum Paint	0.27–0.67
Commercial Copper (Polished)	0.07
Oxidized Copper	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85–0.91
Oil Paints (any color)	0.92–0.96
Lampblack in Shellac	0.95
Varnish	0.89–0.93

Table 16.3 Emissivities of Common Surfaces

16.6.1 Example Of Use Of Radiation Nomogram

Given: —Stack composed of 3″ x 3″ square cooling fins
—1″ spacing between fins
—ambient temperature = 40°C
—fin surface temperature = 100°C

Problem: Determine coefficient of radiation heat transfer (h_r) and total radiation heat transfer (q_r) assuming fin effectiveness = 1. (See Section 16.9)

Solution: $$T_G = \frac{T_S + T_A}{2} = \frac{100 + 40}{2} = 70°C$$

Following the dashed line sequence starting at 1 for the above conditions, h_r = .0024 w/in. ^{2}°C.

$q_r = h_r A \Delta T$ = (.0024 watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 2.6 watts per fin.

For single unstacked fins surrounded by 40°C ambient h_r = .0054 watts/in. ^{2}°C by the indicated line on the nomogram.

$q_r = h_r A \Delta T$ = (.0054) (3 x 3 x 2) (100 − 40) = 5.8 watts per fin.

16.7 FREE OR NATURAL CONVECTION

For vertical fins surrounded by air at sea level and at surface temperatures up to 800°C, the free convection heat transfer coefficient (h_c) can be approximated by the following equation which assumes laminar flow of the cooling medium:[2]

$$h_c = 0.00221\left(\frac{\Delta T}{L}\right)^{0.25} \frac{\text{watts}}{\text{in.}^{2}\text{°C}} \qquad (16.3)$$

where ΔT = temperature difference between surface and ambient air (°C)
L = vertical length of fin (inches)

This equation remains conservative for fin spacing down to approximately $\sqrt[4]{L}$ inch. Figure 16.10 presents Equation 16.3 in the form of a nomogram for convenience.

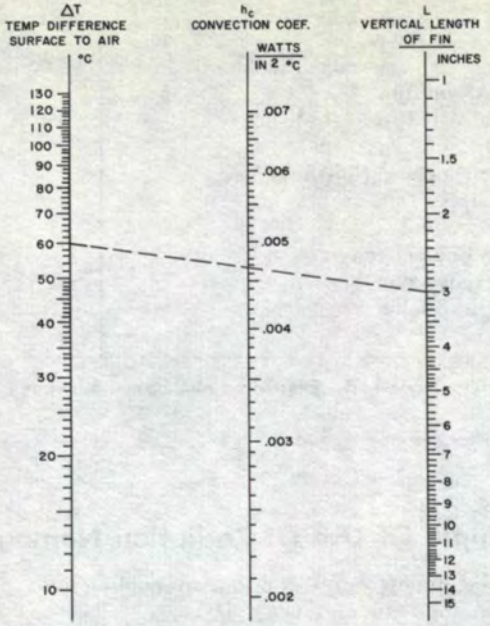


Figure 16.10 Free Convection Nomogram (Vertical Fins—Sea Level Air)

16.7.1 Example Of Use Of Free Convection Nomogram

Given: —3″ x 3″ square cooling fin
—ambient temperature = 40°C
—fin surface temperature = 100°C

Problem: Determine free convection coefficient of heat transfer (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1. (See Section 16.6).

Solution: $\Delta T = T_S - T_A = 100 - 40 = 60°C$
$L = 3$ inches
As shown by dashed line on nomogram, $h_c = .00465$ watts/in. ^{2}°C.
$q_c = h_c A \Delta T = (.00465$ w/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 5.02 watts.

Altitude derating factors for the free convection heat transfer coefficient are shown in Figure 16.11 for fins from ½ inch to 2 feet on a side.

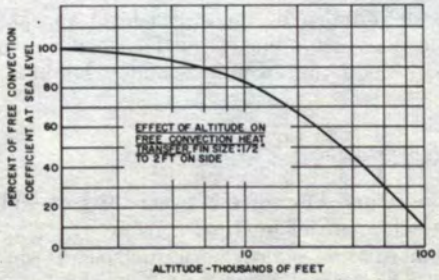


Figure 16.11 Effect of Altitude on Free Convection Heat Transfer

16.8 FORCED CONVECTION

When air is moved over cooling fins by external mechanical means such as fans or compressors, heat transfer is improved and the convection heat transfer coefficient can be approximated by the following equation:*

$$h_c = 11.2\sqrt{\frac{V}{L}} \times 10^{-4} \text{ watts/in. } ^2\text{C} \qquad (16.4)$$

where V = free stream linear cooling air velocity across fin surface (ft./min.)
L = length of fin parallel to air flow (inches)

This equation is based on laminar (non-turbulent) air flow which exists for smooth fin lengths up to $L \cong C/V$, where C is a constant given in Table 16.4 for various air temperatures. For $L > C/V$, air flow becomes turbulent and heat transfer is thereby improved. Turbulent air flow and the resultant improvement in heat transfer may be achieved for shorter L's by physical projections from the fin such as wiring and the rectifier cell itself. However, turbulence increases the power requirements of the main ventilating system. Minimum fin spacing for the above is $B\sqrt{\frac{L}{V}}$ inches where B is also a constant given in Table 16.4.

Air Temperature	B	C
25°C	3.4	37,000
55°C	3.8	45,000
85°C	4.1	52,000
125°C	4.5	63,000
150°C	4.7	70,000

Table 16.4 Laminar Flow Limitations

Figure 16.12 presents a nomogram for convenience in solving the forced convection equation, Equation 16.4 above.

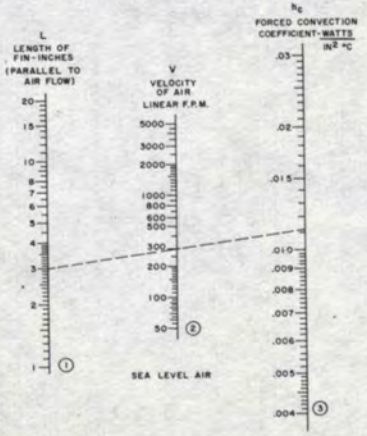


Figure 16.12 Forced Convection Nomogram

* This is accurate within 1% of Equation 7.48, Reference 2, p. 149 for air properties up to 250° C.

16.8.1 Example Of Use Of Forced Air Convection Nomogram

Given: —3″ x 3″ square cooling fin
—air velocity = 300 linear FPM
—ambient air = 40°C
—fin surface temperature = 100°C

Problem: Determine forced convection heat transfer coefficient (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1.

Solution: L = 3 inches, V = 300 LFPM
As shown on dashed line on nomogram, h_c = .011 watt/in. ^{2}°C.
$q_c = h_c A \Delta T$ = (.011 watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C)
= 11.9 watts.

16.9 FIN EFFECTIVENESS

For fins of thin material, the temperature of the fin decreases as distance from the heat source (the SCR) increases due to effects of surface cooling. Thus calculations of heat transfer, such as those above, which are based on the assumption that the fin is at a uniformly high temperature are optimistic and should be corrected for the poorer heat transfer which exists at the cooler extremities of the fin. The correction factor which is used is called fin effectiveness (η). η is defined as the ratio of the heat actually transferred by the fin, to the heat that would be transferred if the entire fin were at the temperature of the hottest point on the fin. The hottest spot, of course, is adjacent to the stud of the SCR. The effectiveness depends on the length, thickness, and shape of the fin, on the total surface heat transfer coefficient h, and on the thermal conductivity k of the fin material. As defined in Equation 16.1, the total actual heat transfer may be calculated by multiplying the fin effectiveness factor by the total surface heat transfer (determined by adding the radiation and convection heat transfer as calculated in the examples above).

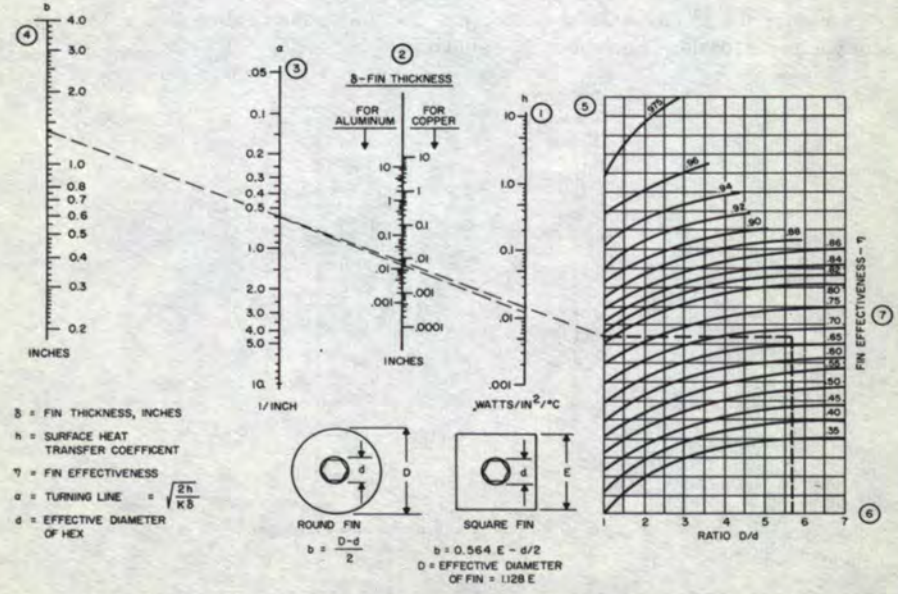


Figure 16.13 Fin Effectiveness Nomogram For Flat, Uniform Thickness Fin

Fin effectiveness can be computed by means of the nomogram shown in Figure 16.13. The typical sequence of proceeding through the nomogram is indicated by the encircled numbers adjacent to the scales.

16.9.1 Example Of Use Of Fin Effectiveness Nomogram

Given: —Stack composed of 3″ x 3″ square painted aluminum fins, each 1/64 inch thick.
—Effective stud hex diameter d = 0.59 inch.
—1 inch spacing between fins
—300 LFPM air velocity
—Fin temperature at stud = 100°C.
—Ambient air temperature = 40°C.

Problem: Determine total heat transfer of each fin.

Solution:

1st Step: Determine total heat transfer coefficient. Radiation heat transfer coefficient h_r = .0024 w/in. ^{2}°C per example in Section 16.6. Convection heat transfer coefficient h_c = .011 w/in. ^{2}°C per example in Section 16.8.
Total heat transfer coefficient = $h_r + h_c$ = .0024 + .011, h = .0134 w/in. ^{2}°C.

2nd Step: Determine fin effectiveness factor from nomogram.

$$b = 0.564E - d/2 = (0.564)\ (3) - \frac{0.59}{2} = 1.39''$$

$$D/d = \frac{1.128 \times 3}{0.59} = 5.64$$

For h = .0134 w/in. ^{2}°C and thickness δ = .0155 inch. α = 0.58 as indicated by the dashed line on the nomogram. Through b = 1.39 and α = 0.58, a line is extended to the graph where D/d = 1. Projecting horizontally on this graph to D/d = 5.64, η is found to be 0.67.

3rd Step: Determine total heat transfer.
Total heat transfer $q = hA\eta\Delta T$
q = (.0134 w/in. ^{2}°C) (18 in.^{2}) (0.67) (100 − 40°C)
= 7.2 watts per fin.

For fin materials other than copper or aluminum, use the "copper" scale on the nomogram by multiplying the actual fin thickness by the ratio of the thermal conductivity of the material being considered to the thermal conductivity of copper. Thus, for a 1/8 inch *steel* fin, enter axis 2 on the *copper* scale at 0.125 inch x 1.16/9.77 = 0.015 inch. Thermal conductivities of several commonly used fin materials are given in Table 16.5.

Material	Density (lbs/in.^{3})	Heat Capacity (c) (watt-sec./lb. °C)	Thermal Conductivity (k) (watts/in. °C)
Aluminum	0.098	407	5.23
Brass (70 Cu, 30 Zn)	0.30	179	2.70
Copper	0.32	175	9.77
Steel	0.28	204	1.16

Table 16.5 Thermal Properties of Heatsink Materials

In general, it will be found that fin thickness should vary approximately as the square of the fin length in order to maintain constant fin effectiveness. Also, a multi-finned assembly will generally have superior fin effectiveness and will make better use of material and weight than a single flat fin.

16.9.2 Typical Example Of Complete Fin Design

Given: —Four C35 SCR's with 9/16″ hex and 1/4″–28 thread are operated in a single-phase bridge at 10 amperes DC maximum each. The specifications for this rectifier indicate that at this current level each SCR will develop 16 watts of heat losses at its junction and that for satisfactory service at this current level, the stud temperature should be maintained below 92°C. The maximum ambient temperature is 40°C and free convection conditions apply.

Problem: Design a stack of fins to adequately cool the four SCR's in this bridge circuit.

Solution:

1st Step: Determine maximum allowable fin temperature at radius of stud hex. From Chart 16.1, the thermal resistance from stud to fin for a joint with lubricant is 0.35°C/watt maximum. The maximum fin temperature therefore must not exceed 92°C — (0.35°C/watt x 16 watts) = 86°C.

2nd Step: Estimate required fin designs based on space available: 6″ x 6″ painted vertical fins at one inch spacing. Material .08 inch thick steel. Assume all cell losses are dissipated by fin.

3rd Step: Determine surface heat transfer coefficient and fin effectiveness of estimated fin design:

Radiation (from Nomogram in Figure 16.9)

$$T_G = \frac{86 + 40}{2} = 63°C \qquad h_r = .00145 \text{w/in.}^2\text{°C}$$

Free Convection (from Nomogram in Figure 16.10)

$$\Delta T = 86 - 40 = 46°C \qquad \frac{h_c = .0037 \text{w/in.}^2\text{°C}}{h_{total} = .0052 \text{w/in.}^2\text{°C}}$$

Fin Effectiveness (from Nomogram in Figure 16.13)

$D = 1.128E = 1.128 \times 6 = 6.768$

$d = 0.59$ from Table 16.1

$$b = 0.564E - d/2 = 0.564 \times 6 - \frac{0.59}{2} = 3.089$$

$$D/d = \frac{6.768}{0.59} = 11.5; \quad \delta \text{ Cu} = (.08)\frac{1.16}{9.77} = .0095 \text{ in.}$$

Using these parameters in the nomogram, $\eta = 55\%$

4th Step: Determine total heat transfer for estimated fin.

$q = hA\eta\Delta T$

= (.0052) (6 x 6 in.^{2}) (2 sides) (0.55) (86 – 40°C)

= 9.7 watts

5th Step: Determine error in approximation. Re-estimate fin requirements, and recalculate total heat transfer. In this example, the capabilities of the initial fin design fell considerably below the requirements of 16 watts. To sufficiently increase the heat transfer, a ¼″ thick copper fin would be needed. Alternately a thinner fin of larger area could be used.

16.10 MEASUREMENT OF STUD TEMPERATURE

Heatsink design should be checked in the prototype equipment. A 10 or 12 mil thermocouple wire should be used. A copper-constantan thermocouple junction is suggested. The thermocouple junction should be carefully soldered to the center of the flat surface on the stud hex as indicated in Figure 16.14. The temperature at this point closely approximates the temperature of the stud immediately below

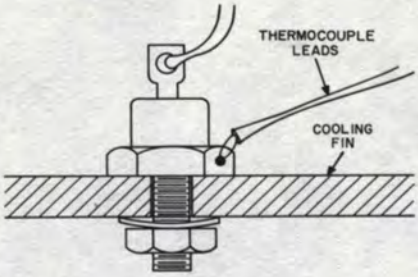


Figure 16.14 Preferred Location for Mounting Thermocouple for Stud Temperature Measurements

the rectifier junction, which is inaccessible once the cell is mounted to a fin. The point of measurement on the stud should be shielded from any forced air which might cause localized cooling, and the leads should be kept out of any flow of cooling air since they can provide a heat flow path which will lower the temperature at the thermocouple junction.

Unless carefully calibrated leads and instruments are available, a thermocouple bridge rather than a pyrometer should be employed. Care should be taken to keep the thermocouple leads out of electric fields that might induce error voltages in the leads.

As an alternative to using a thermocouple, temperature indicating waxes and paints bearing such trademarks as "Thermocolors" (manufactured by Curtiss-Wright Research Corporation) and "Tempilaq" (manufactured by Tempil Corporation, New York City) can be used to indicate whether the stud exceeds a specific level of temperature. Careful attention should be given to the manufacturer's instructions for using this type of temperature indicator to prevent mis-application and errors. Temperature indicating paints and waxes are particularly useful in high electrical fields where substantial errors may occur in electrical measurement techniques or where the fin is inaccessible for thermocouple leads during the test, such as on the rotor of a rotating machine. Care must be taken in applying paints so their presence does not materially affect the emissivity of the surface.

Use of the foregoing procedures to produce a well-engineered cooling fin design for SCR's can pay big dividends in reliable operation, low material costs, and minimum space and weight requirements.

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SCR Reliability

17.1 INTRODUCTION

Prior to the introduction of the Silicon Controlled Rectifier (SCR), the inherent long life capability of solid state devices had already been demonstrated through the field experience of semiconductor diodes and transistors. The desirability of a solid state power switching device was enhanced by the fact that equivalent reliability of such a device represented an even more dramatic improvement in size, weight, efficiency and reliability over superseded technologies than was the case with signal semiconductor devices.

At the time the first commercial SCR was being developed, there was a growing awareness of the need for the establishment of more formalized reliability criteria in the missile and aerospace fields, and means for enforcing these criteria. It was possible to anticipate a high degree of receptivity in these industries for an SCR with design and development criteria which would assure a high degree of device reliability under the broad range of stresses in the anticipated applications. It was apparent that the initially higher cost of a broadly applicable device, optimized for reliability in its initial design, would be justified through improved performance of aerospace systems.

Approximately two years from the time it became the first commercially available SCR, the General Electric C35 was qualified to the first military SCR specification. At about this time, a specification was finalized which made this same device one of the qualified components in the much publicized Minuteman high reliability missile program.

With continuous early production of the SCR being supported by the requirements of the military and aerospace industries, it became possible, through continuing development of improved processes and techniques, to actually augment reliability while effecting considerable reductions in device cost. Related evaluation programs have contributed to the subsequent capability of providing even further cost advantages through improved ability to define and optimize for reliability for more narrowly defined application conditions. The producers of commercial, industrial, and consumer equipment, ever mindful of the importance of reliability to cost and reputation, are taking increasing advantage of the benefits derived from early support of and investment in the SCR by the military and aerospace industries, and by the General Electric Company. High volume applications of the SCR in such diverse products as missiles, industrial controls, and household appliances are now common and are increasing at a rapid rate.

The General Electric Company has since applied its reliability criteria in the design and production of other Silicon Controlled Rectifiers which have expanded the availibility of device configurations and ratings according to the increasingly varied applications requirements of industry. At this writing, the General Electric Company offers approximately twenty different series of SCR's ranging in rating from one ampere rms to four hundred and seventy amperes rms, and up to eleven hundred volts. Also offered are specially developed high reliability device specifications for the convenience and advantage of aerospace and related industries. These specifications are discussed separately in section 17.6.2 of this chapter.

17.2 FACTORS INFLUENCING ACHIEVEMENT OF RELIABILITY

There are a variety of factors which, in combination, influence the actual reliability of completed SCR's in the end application.

17.2.1 Design For Reliability

DESIGN FOR RELIABILITY may be subdivided into the three categories of thermal, mechanical, and surface, all of which contribute significantly to the inherent reliability capability of the finished product.

THERMAL—Junction temperature of the SCR represents the basic limitation to rating and capability. Thermal design is concerned not only with the temperature capability of the device, but with its heat transfer characteristics and their stability, as well.

The degradation of internal connections or interfaces under normal use conditions can result in significantly increased internal dissipation and can also cause an increase in thermal impedance between junction and case. The complete package, both internally and externally, must be capable of withstanding the rate and degree of temperature excursions required by the end application if reliability is to be achieved. For this reason, use is made of materials with matched coefficients of expansion which are joined with solders scientifically selected to reduce the likelihood of metal fatigue.[1]

MECHANICAL—As with other devices, the SCR must be capable of withstanding the normal mechanical stresses encountered in production handling, shipping, and installation. It must also be capable of meeting the requirements of the mechanical environment to which it will be exposed in the end application.

Design for mechanical reliability includes the use of rigid assemblies of low mass, low moments of inertia, and the elimination of mechanical resonances in the normal ranges of vibration and shock excitation. Mechanical ruggedness of glass to metal seals is also necessary to assure integrity of hermetic seals during the useful life of the device.

INTERNAL SURFACE PROTECTION—This aspect is of sufficient importance to merit separate consideration in that inadequate isolation of the semiconductor element from undesirable atmospheres would result in excessive electrical degradation due to changes in surface characteristics caused by such atmospheres. Although the stability of surface characteristics may be improved through chemical neutralization or through treatment to reduce surface voltage gradients,[2] an effective hermetic seal is necessary for the assurance of long term reliability.

17.2.2 Rating For Reliability

The establishment of a realistic relationship between significant design criteria and published maximum ratings is important, if the possibility is to be avoided of inadvertently allowing the device to be applied beyond its design capability. All General Electric devices are subjected to detailed analyses of power dissipation characteristics. This information, together with a knowledge of the thermal transfer characteristics, allows accurate computation of the peak junction temperatures achieved under operating conditions (see chapter 3). Using a digital computer, a set of rating calculations for one type of General Electric SCR involves approximately eighteen thousand mathematical operations by the superposition method.[3]

The result is the assurance that the design junction temperature capability will not be exceeded when the SCR is operated within its published ratings.

17.2.3 Production For Reliability

The complete manufacturing process must be carefully designed and controlled if all design criteria, including reliability, are to be maintained in volume production. Certain aspects of the process allow a greater degree of opportunity than others, to optimize for the achievement of reliability criteria.

MATERIALS—Complete and properly detailed material specifications are an obvious basic necessity. Also important, however, are adequate means for thorough evaluation of the materials both prior to and, as in the case of gases, during their use. The necessary facilities are extensive and often quite sophisticated. They provide the ability to perform electrical, mechanical, physical, chemical, and environmental evaluations.

WORKMANSHIP—Rigid test and inspection standards throughout the process provide an effective means for monitoring controls. The human element is ever present, even in the most automated of processes, and rigid standards of workmanship help to instill a sense of urgency in the operators for the maintenance of the necessary degree of control.

TOOLS—The tooling and equipment used in the processing and fabrication of the semiconductor device can make an increased contribution to reliability of the completed device if their design is optimized for ease of set-up, easy maintainability, repeatability, and simplicity of operation to minimize or eliminate operator judgement.

TEST AND INSPECTION—The design and efficient implementation of in-process inspections and device testing provides for positive monitoring of the effectiveness of controls, with a minimum time lag for the institution of immediate corrective action when the need is indicated. The testing may include electrical tests in both the sub-assembly and completed stages, as well as environmental and electrical stressing of the completed devices.

17.2.4 Application For Reliability

Device application, although beyond the control of the device manufacturer, nevertheless plays a significant part in system reliability performance. Even excluding circuitry approaches to reliability, such as circuit selection and redundancy, several application aspects can be directly related to the individual device.

DERATING—Those mechanisms which might result in eventual device failure when the device is operated within ratings, can be expected to react with time according to the degree of the applied stress to which the particular mechanism is sensitive. Significant abrupt changes in parameter characteristics are generally of a catastrophic nature and occur either upon mechanical failure or after a gradual degradation which has progressed sufficiently such that junction temperature, under operating conditions, is in excess of design limits.

Tests performed on various devices have served to demonstrate the relative effects of stress derating on those particular devices. Figure 17.1 illustrates an analysis of such a test performed on a General Electric rectifier diode. It is presented in the form of relative failure rate improvement curves, or acceleration factors, based upon the derating of temperature, voltage, and current.[4] These curves are the result of a matrix test wherein a number of rectifier diodes were divided into

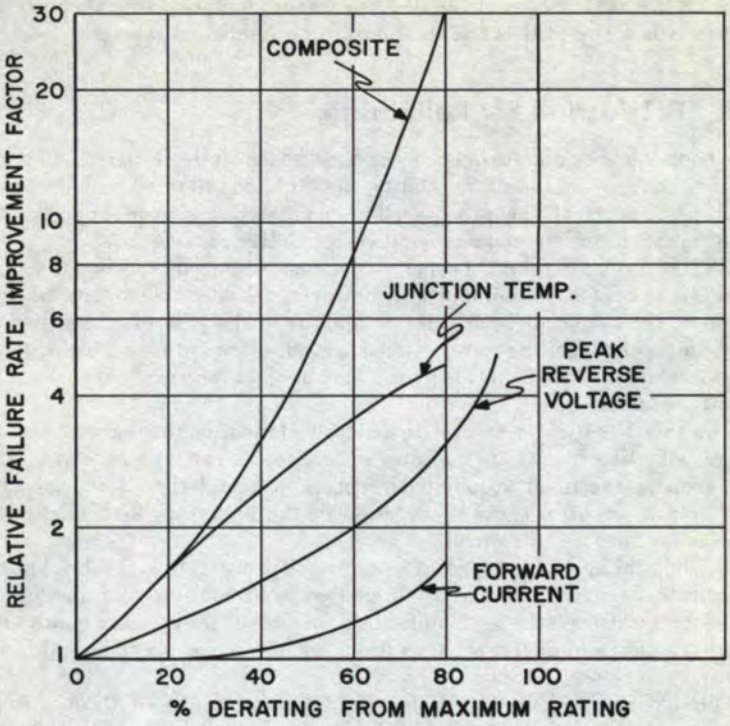


Figure 17.1 Failure Rate Improvement Vs. Derating

groups, each group of which was subjected to a different set of stress conditions for a long period of time. Extensive testing of a similar nature is presently being conducted on the General Electric C35 series of SCR.

A decrease in failure rate is effected by derating through the slowing of the processes that might eventually result in device failure. Some mechanisms, under some derated conditions, might never result in failure during the life of the system in which the device is applied.

DEFINITION OF FAILURE—Excessive drift allowances in circuit design can lead to excessive power dissipation and a resultant decrease in system reliability due to increased temperatures. On the other hand, designing to overly restrictive parameter limits can result in an unnecessarily increased failure rate. Similarly, the use of restrictive definitions of failure in failure rate measurement tests can increase failure rate artificially as a result of purely analytical failures.

As described above, the degradation that can occur in a few devices might do so at a sufficiently slow rate that significant failure rate improvement results simply from the relaxation of the definition of failure. Some failures, with realistic limits applied, might never exist as failures during the useful life of the system.

Equally important is the existence of known mechanisms which can allow only a limited parameter drift in operation. Such mechanisms generally involve the entrapment of ionizable materials within the hermetic seal.[5] When ionized, these materials can cause an electrical change in the geometry of the semiconductor element. Because the availability of ionizable material is limited in a properly sealed device, so also is the amount of electrical change it can cause.

17.3 FAILURE MECHANISMS

Failure mechanisms, as alluded to above, are those chemical and physical processes which result in eventual device failure. The kinds of mechanisms that have been observed in the semiconductor classification of component device are shown in the table of figure 17.2. Also shown in the table are those kinds of stresses to which each mechanism is likely to respond.[6]

If more than a few such failure mechanisms are, to any significant degree, prevalent in a given device type from a given process, it would not be reasonable to expect to achieve the degrees of reliability that have been demonstrated by many semiconductors. The dominant mechanisms to which a device type may be susceptible will vary according to the peculiarities of the design and fabrication process of that device.

FAILURE MECHANISM \ STRESS	MECHANICAL				TEMPERATURE			ELECTRICAL				MISCELLANEOUS			
	STATIC FORCE	SHOCK	VIBRATION	PRESSURE (FLUID)	STATIC	SHOCK	CYCLING	VOLTAGE	CURRENT	POWER (CONTINUOUS)	POWER (CYCLED)	CORROSION	ABRASION	HUMIDITY	RADIATION
STRUCTURAL FLAWS – WEAK PARTS	•	•	•	•	•	•	•			•	•				
– WEAK CONNECTIONS	•	•	•	•	•	•	•			•	•				
– LOOSE PARTICLES		•	•				•				•				
– THERMAL FATIGUE						•	•				•				
ENCAPSULATION FLAWS				•		•	•			•		•	•	•	
INTERNAL CONTAMINANTS – ENTRAPPED FOREIGN GASES					•		•								
– OUTGASSING					•		•								
– ENTRAPPED IONIZABLE CONTAMINANTS					•			•							
– BASE MINORITY CARRIER TRAPPING					•				•						
– IONIC CONDUCTION					•		•	•	•	•					
– CORROSION					•			•	•	•					
MATERIAL ELECTRICAL FLAWS – JUNCTION IMPERFECTION								•	•	•					
METAL DIFFUSION					•					•					
SUSCEPTABILITY TO RADIATION															•

Figure 17.2 Failure Mechanisms and Associated Stresses

17.3.1 Structural Flaws

STRUCTURAL FLAWS are generally considered to be the result of weak parts, discrepancies in fabrication, or inadequate mechanical design. Various in-process tests performed on the device, such as forward voltage drop at high current density levels and thermal resistance measurement, provide effective means for the monitoring of controls against such flaws. These tests also provide a means for the elimination of the occasional possible discrepant device.

The modes of failure generally associated with the mechanical flaw category of failure mechanism for an SCR are excessive forward voltage drop, failure to turn on when properly triggered, and open circuit between the anode and cathode terminals. Because these types of failure mechanism are relatively rare, the incidence of these modes of failure is low.

17.3.2 Encapsulation Flaws

ENCAPSULATION FLAWS are deficiencies in the hermetic seal that will allow undesirable atmospheric impurities to reach the semiconductor element. Foreign atmospheres, such as oxygen and moisture, can react in such a way as to permanently alter the surface characteristics of the silicon metal.

A change in surface conductivity is evidenced by gradual increase of the forward and reverse blocking current characteristics. Because the SCR is a current actuated device, it will lose its capacity to block rated voltage if blocking current degrades beyond some critical point. This type of mechanism may eventually result in catastrophic failure. The rate of degradation is dependent mostly on the size of the leak and the level of stress, particularly temperature, that is applied.

A variety of leak detection methods are commonly used. The applicability of each method is related to the construction of the device and the order of magnitude of the leak rate to be detected. Examples of methods in current use are:

PRESSURE DYE—Penetrant dye under pressure. Rejection criteria are visual. Useful for devices encapsulated in transparent glass.

PRESSURE BOMB—Water with a small percentage of wetting agent, such as liquid detergent or alcohol, under pressure. Usefulness is limited if internal surfaces are coated or treated, or if detection of very low leak rate is desired.

BUBBLE TEST—Immersion in heated liquid such as glycerine or clear ethylene glycol. Rejection criteria are visual. This method is effective for detection of gross leaks.

HELIUM—Exposure to helium under pressure. Rejection criteria are based on measurement of the rate of helium flow into and then out of the device.

RADIFLO*—Exposure to radioactive tracer gas under pressure. Rejection criteria based on count of radioactivity within the device.

17.3.3 Internal Contaminants

The inclusion of a source of ionizable material inside the sealed package can result in failure mechanisms similar to those resulting from encapsulation flaws if the inclusion is gross. It can also result in apparently similar mechanisms except that the amount of electrical change that occurs is limited.

The mechanism need not be a permanent change in the surface characteristics of the silicon, but can be an electrical change in base width near the silicon surface due to the formation of inversion layers.[7] This condition is often reversible, with recovery accomplished through the removal of electrical bias and the introduction of elevated temperature.

Because the SCR is a bistable, rather than a linear device, concern for this category of failure mechanism arises only if forward blocking current can increase to the point where forward blocking capability is impaired. The probability of occurrence is extremely low except for the possible case of the small junction area, highly sensitive devices. Even here, the mechanism is often negated through negative gate or resistor biasing in the circuit.

17.3.4 Material Electrical Flaws

This category of failure mechanism involves, basically, imperfections in junction formation. Discrepancies of this nature are not generally experienced with

* Manufactured by the Consolidated Electrodynamics Corp., Analytic and Control Division, Pasadena, California.

SCR's because of their relatively thick base widths and because the blocking junctions are formed by the diffusion process, which allows consistent control of both depth and uniformity of junction.

17.3.5 Metal Diffusion

Of the possible failure mechanisms observed in semiconductors, metal diffusion is the least significant. Though diffusion will occur over a long period of time when two metals are in intimate contact at very high temperatures, the rate at which it progresses is too slow to have tangible effects during the useful life of the device or the system in which it is applied.

17.3.6 Nuclear Radiation

The only true means for determining the actual tolerance of any device to the effects of nuclear radiation is through actual radiation exposure testing of that device. Approximate levels of SCR tolerance, however, have been determined through various tests performed on the General Electric C35 (2N685 series). Critical levels have been shown to be 10^{14} nvt for fast neutron bombardment and 5×10^{5} R/sec for gamma radiation.

Fast neutron bombardment of the silicon results in permanent damage to the crystal lattice, reducing minority carrier lifetime. Significant effects that appear between 10^{13} nvt and 10^{14} nvt are increased gate current to trigger and, to a lesser degree, increased holding current, on voltage, and forward breakdown voltage.[8]

Although gamma radiation may also produce permanent effects on the SCR, it is expected that failure in the typical radiation environment would result first from fast neutron bombardment. Gamma radiation, however, produces high energy electrons by photoelectric and compton processes which create a leakage current during irradiation. High pulse levels of irradiation can have the transient effect of triggering the SCR on. At 10^{6} R/sec, there is a fifty percent chance that the General Electric C35 SCR will be triggered on.[9]

17.4 RELIABILITY MEASUREMENT

Statistics, which are the basis of reliability measurement, are a distinct technical field by themselves, and any attempt to describe the statistics used to derive the measurements must be beyond the scope of this chapter.

Reliability, as commonly defined, is the probability that a device or system will perform its intended function for a given period of time under a specified set of conditions. Reliability may be thought of in terms of life expectancy, and is not technically the same as quality, a term often used interchangeably. The latter is rather a measure of the degree to which design and production criteria are met, and thus represents but one aspect of reliability.

The ultimate concern is, of course, how well the over-all system performs. The reliability measurement of a system is often applied as Mean Time Between Failures (MTBF), in order to evaluate anticipated down time and maintenance costs and to help establish optimum preventive maintenance schedules. The implementation of a system MTBF design goal is a complex process of properly weighting the various contributing elements and applying the necessary control to each aspect. Although it is sometimes assumed that system reliability is but the sum of the reliabilities of the component parts in the system, studies of actual field histories have indicated

that no more than thirty percent of field failures have been directly attributable to failure of defective component devices.[10] Other assignable causes for system failure include misapplication, handling, workmanship, installation and maintenance as relate to the system. It may be concluded that while the elimination of all defective components would only partially eliminate system failures, it is nevertheless desirable to establish an optimum control over component reliability.

17.4.1 Sampling Plans

Various test sampling plans are used to evaluate the acceptablity of homogeneous component lots. The two most commonly used are the AQL (Acceptable Quality Level) sampling per MIL-STD-105 and the lambda-LTPD (Lot Tolerance Percent Defective) sampling per MIL-S-19500.

AQL—The AQL sampling plan is designed to control the acceptance of device lots based on an allowable proportion of devices with undesirable characteristics being included in the lot. The sample size is therefore a function of the size of the lot, and the accuracy with which the sample truly represents the lot is determined by the design of the specific sampling procedure used.

The operating characteristic curve for a typical sampling plan is shown in figure 17.3, which describes the probability of accepting a lot according to the proportion of defectives that could be included in that lot. It may be noted that there is both a risk that a lot with a lower proportion of defectives than allowable will be rejected (producer's risk), and a risk that a lot with a greater proportion of rejects than is allowable will be accepted (consumer's risk). As the ratio of sample size to lot size is increased, the slope of the operating curve becomes steeper, decreasing the differences between the probabilities of acceptance and rejection for a given proportion of defectives.

Certainty of acceptance or rejection for a given proportion of defectives can only be accomplished if the lot is specially tested on a one hundred percent basis. Doing so, however, obviously defeats the purpose for which the sampling plan was developed. The ratio of sample size to lot size actually used must be determined as a function of economics founded on a comparison of the effect on initial device cost versus the effect on incoming test and rework costs.

LAMBDA—As used in MIL-S-19500, lambda is the same as LTPD when associated with a one thousand hour test period. The unit of measure is failure rate in percent per thousand hours. The sampling plan for lambda at the ninety percent confidence level is given as Table IV of MIL-S-19500C, and is shown below as figure 17.4. The statistical derivation of this sampling plan takes into consideration the resolution with which the sample represents the population from which it is drawn and the general pattern of behaviour with time of the devices under observation.

The relationship between sample size and lot size differs considerably from the AQL sampling plan discussed above. In the lambda sampling plan, the sample size does not change in accordance with the lot size, but only according to the lambda to be measured, the number of rejects to be allowed, and the degree of confidence desired. Although the sample size does not change in the lambda sampling plan, certain assumptions are made in regard to lot size.

Where the sample size equals the lot size, the obvious result is one hundred percent confidence. As the size of the lot is increased from which a given sample size is drawn, the degree of confidence is decreased. However, above the point at which the lot size is approximately five times the sample size, changes in the degree of confidence become insignificant. Calculations of failure rate, using the lambda

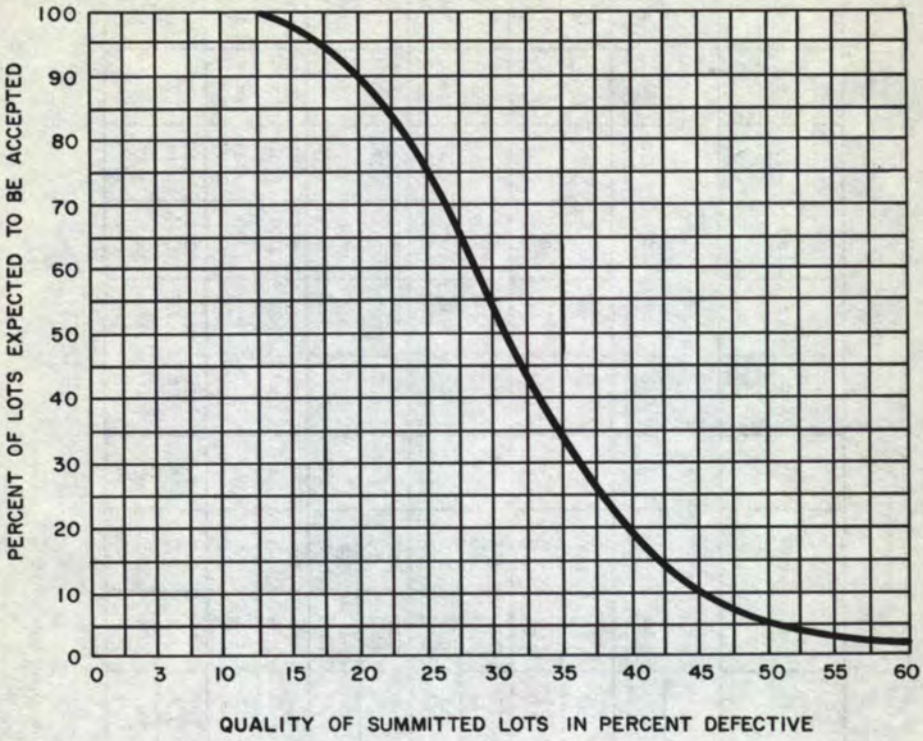


Figure 17.3 Typical Operating Characteristic Curve

sampling plan, are therefore performed on the assumption that the size of the lot from which the samples under observation were drawn, is infinite in number.[11]

If, in the lambda sampling plan, the sample size for a specific failure rate is increased without increasing the allowable number of rejects, the degree of confidence in the accuracy with which the sample represents an infinite homogeneous population is increased. The table of figure 17.4 provides for measuring maximum failure rates at a ninety percent confidence.

It may be seen, from figure 17.4 that if two rejects occur during a one thousand hour life test of one thousand and sixty-five devices, there is a ninety percent probability that no more than one half of one percent of an infinite homogeneous population represented by the sample tested would fail to the same limits, if tested for the same period of time under the same conditions. It is significant to also observe from figure 17.4 the limitation placed on the ability to measure actual failure rate by the statistics of the sampling plan.

According to the method by which the lambda sampling was derived, it is approximately correct to extrapolate an order of magnitude of failure rate for an order of magnitude of sample size at the zero acceptance number. On this basis, a minimum sample of approximately two hundred and thirty thousand devices would have to be tested for a thousand hours, with no failures observed, to show a maximum failure rate of 0.001% per thousand hours at a ninety percent confidence level.

Minimum size of sample to be tested to assure, with a 90 percent confidence, a Lot Tolerance Percent Defective or λ no greater than the LTPD specified. The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

Rejection Number	Acceptance Number	Maximum Percent Defective (LTPD) or λ (1)	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.1
			Minimum Sample Sizes													
1	0		11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	770 (0.007)	1152 (0.005)	2303 (0.002)
2	1		18 (2.0)	25 (1.4)	38 (.94)	55 (.65)	77 (.46)	129 (.28)	195 (.18)	258 (.14)	390 (.09)	555 (.06)	778 (.045)	1298 (.027)	1946 (.018)	3891 (.009)
3	2		25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (.78)	176 (.47)	266 (.31)	354 (.23)	533 (.15)	759 (.11)	1065 (.080)	1777 (.046)	2662 (.031)	5323 (.015)
4	3		32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (.62)	333 (.41)	444 (.31)	668 (.20)	953 (.14)	1337 (.10)	2228 (.061)	3341 (.041)	6681 (.018)
5	4		38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (.75)	398 (.50)	531 (.37)	798 (.25)	1140 (.17)	1599 (.12)	2667 (.074)	3997 (.049)	7994 (.025)
6	5		45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (.85)	462 (.57)	617 (.42)	927 (.28)	1323 (.20)	1855 (.14)	3099 (.084)	4638 (.056)	9275 (.028)
7	6		51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (.94)	528 (.62)	700 (.47)	1054 (.31)	1503 (.22)	2107 (.155)	3515 (.093)	5267 (.062)	10533 (.031)
8	7		57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (.67)	783 (.51)	1178 (.34)	1680 (.24)	2355 (.17)	3931 (.101)	5886 (.067)	11771 (.034)
9	8		63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (.72)	864 (.54)	1300 (.36)	1854 (.25)	2599 (.18)	4334 (.108)	6498 (.072)	12995 (.036)
10	9		69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (.77)	945 (.58)	1421 (.38)	2027 (.27)	2842 (.19)	4739 (.114)	7103 (.077)	14206 (.038)
11	10		75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (.80)	1025 (.60)	1541 (.40)	2199 (.28)	3082 (.20)	5147 (.120)	7704 (.08)	15407 (.04)

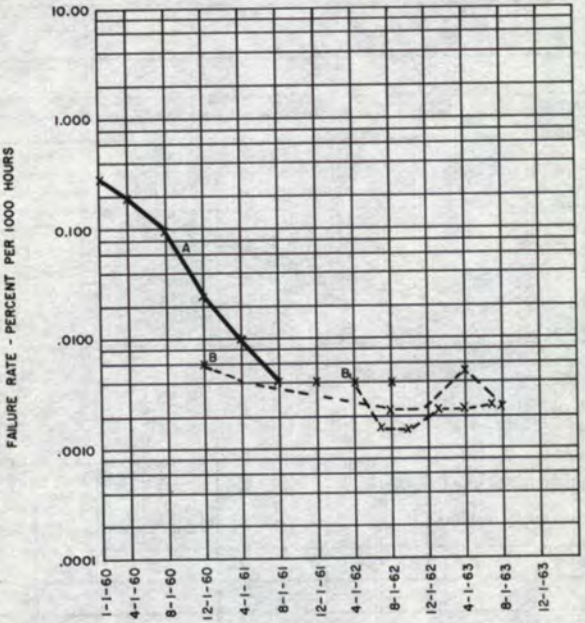
(1) The life test failure rate lambda (λ) shall be defined as the LTPD per 1000 hours.

Figure 17.4 Lambda Sampling Plan at 90% Confidence

17.4.2 Failure Rate Analyses

Reliability demands placed on the SCR by the military and aerospace industries have been as stringent as for rectifier diodes; SCR requirements tend in fact to be even more stringent because of the greater number of parameters to be controlled. Test results and field experience, however, have shown the SCR to be capable of meeting the same reliability criteria as rectifier diodes.

The General Electric C35B (2N685) SCR was assigned the same failure rate objective of 0.004% per thousand hours at sixty percent confidence by the Minuteman program as was assigned to the medium current rectifier diodes. Figure 17.5 is a failure rate chart showing the achievement and maintenance of the objective failure rates in accordance with the program requirements. This chart also illustrates the use of acceleration factors. While the failure rate measurement tests were operated at maximum device rating, application is restricted to derated conditions. A factor of one hundred is applied to the actual maximum failure rate calculation to reflect the reduction of failures as a result of the derating.



Curve A—Maximum allowable failure rate for operation at optimum conditions per Minuteman specifications:
Reverse voltage = 160 PRV
Forward current = 4 Adc
T_C = 40°C

Curve B—Failure rate based on Degradation Rate Test—Group B, at 60% confidence level. Acceleration factor assumed to be 100.

Curve B_1—Failure rate based on Reliability Figure of Merit data, at 60% confidence level, from which the latest twelve months average is calculated every three months. Acceleration factor assumed to be 100.

Figure 17.5 Failure Rate Chart—C35B (2N685)

If the devices were to be tested under actual use conditions, and the use of acceleration factors eliminated, the periodic failure rate measurement tests would require that samples of more than fifty thousand devices be tested for a thousand hours, with only one reject allowed in each case.

Extensive testing of a single device type to one specification, as is the case with Minuteman, is not common. It is, more often than not, necessary to project maximum failure rates on the basis of a more limited number of observations. These projections necessarily include a degree of engineering judgement which is based on a knowledge of the device design and construction and on field experience.

The most common source for significant test information is developed in the qualifying of device lots to military specifications. Although sample sizes tend to be limited, reasonable significance can often be achieved by the combining of voltage grades of the same device, and by viewing test results cumulatively. Figure 17.6 shows failure rate as calculated for the C10D (2N1777A) from a sample tested to the intermittent operating conditions of MIL-S-19500/168. Figure 17.7 is a similar calculation for combined quantities of C10D(2N177A) and C10C (2N1776A) tested during the same period of time.

LIFE TEST CONDITIONS			
$T_A = 118° \pm 5°C$	$I_F = 3.0$ amps	Intermittent Life	50 min. on 10 min. off

PARAMETER READING CONDITIONS AND LIMITS					
Parameter Measured	Test Conditions	Acceptance Limits		Post Test End Points	
		Minimum	Maximum	Minimum	Maximum
I_{RO}	Rated V_{ROM}	....	1.ma	....	2 ma
I_{FO}	Rated V_{FOM}	....	1.ma	....	2 ma
I_{GT} V_{GT}	V_{FOM} = 6Vdc	....	15.ma 2.Vdc	....	15 ma 2 Vdc

Hours on Test	Number of Devices	Number of Defectives	Reason for Defectives	Reading of Defectives	Post Test End Point Failure Rate	
					60% Confidence Level	90% Confidence Level
0	62	0	....	....	....	....
250	62	0	....	....	....	....
500	62	0	....	....	....	....
1000	62	0	....	....	1.45	3.62

Figure 17.6 Reliability Figure of Merit—C10D Per Mil-S-19500/168

Hours on Test	Number of Devices	Number of Defectives	Reason for Defectives	Reading of Defectives	Post Test End Point Failure Rate	
					60% Confidence Level	90% Confidence Level
0	122	0	....	....	....	....
250	122	0	....	....	....	....
500	122	0	....	....	....	....
1000	122	0	....	....	0.75	1.88

Figure 17.7 Reliability Figure of Merit—C10C and C10D Per Mil-S-19500/168

The above referenced maximum failure rate calculations are based on operation of the devices at maximum rated conditions, and include no acceleration factors. Except for unusual requirements, the actual failure rates as calculated indicate a high enough degree of reliability to meet the needs of industry in general. It must be remembered, however, that failure rates as calculated above do not always present the actual failure rate of the device, but rather a failure rate level which the device does not exceed. The level shown is derived as a function of the number of devices observed; true failure rate could conceivably be lower by orders of magnitude.

17.5 PARAMETER DISTRIBUTIONS VERSUS TIME

While previous discussions in this chapter have related to the probability and nature of an individual SCR failure, there is also interest in the behaviour with time of the general population of devices. In Figure 17.6, the calculated failure rate was given for a quantity of C10D(2N1777A) SCR's life tested to MIL-S-19500/168. The actual variables readings of the major parameters for the same devices during the same tests are plotted against time as percentile distributions in Figure 17.8.

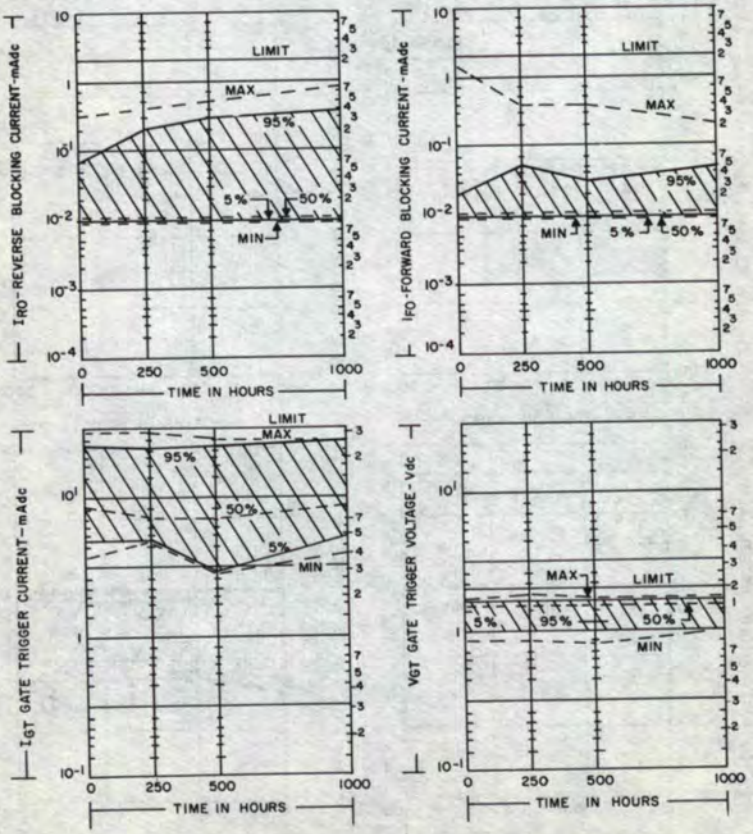


Figure 17.8 Parameter Distributions—C10D Operating Life Per Mil-S-19500/168

In observations of this nature, it is important to recognize the limitations of instrumentation, particularly when comparisons are made of measurements taken over widely spaced intervals of time. Variations in readings are normally expected to be observable from equipment to equipment and from operator to operator. Variations with the same equipment over a period of time are normal even with strict adherence to regularly scheduled programs of calibration.

All major SCR characteristics are variable with temperature, introducing a further significant possibility for instrumentation error, the minimizing of which imposes stringent requirements on test circuitry. Independently of ambient temperature variances, the low thermal mass of the junction can result in significant temperature variations depending upon the amplitude and duration of pulses of test power applied. The low levels of static characteristics that have been achieved with the large junction areas common to the SCR provide appreciable amplification of instrumentation errors.

Figure 17.9 shows percentile distributions of the major parameters for ten samples of the General Electric C35B(2N685) during a three thousand hour intermittent operating life test to the conditions of MIL-S-19500/108. Figure 17.10 shows percentile distributions of the same parameters for a different sample of 25 devices during a three thousand hour elevated temperature storage life test per the conditions of the same specification.

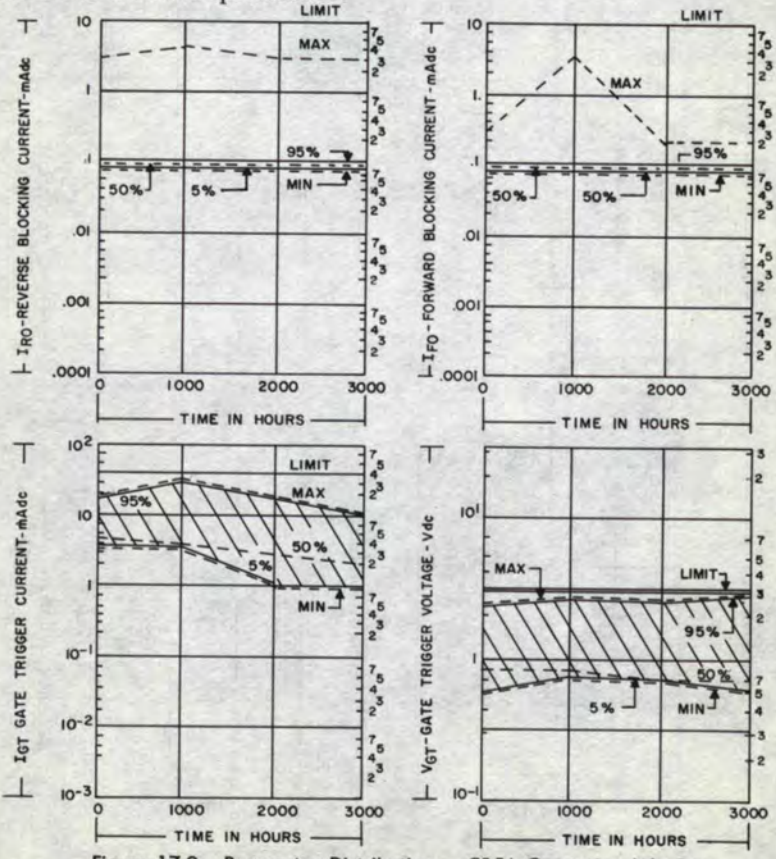


Figure 17.9 Parameter Distributions—C35A Operating Life Per Mil-S-19500/108

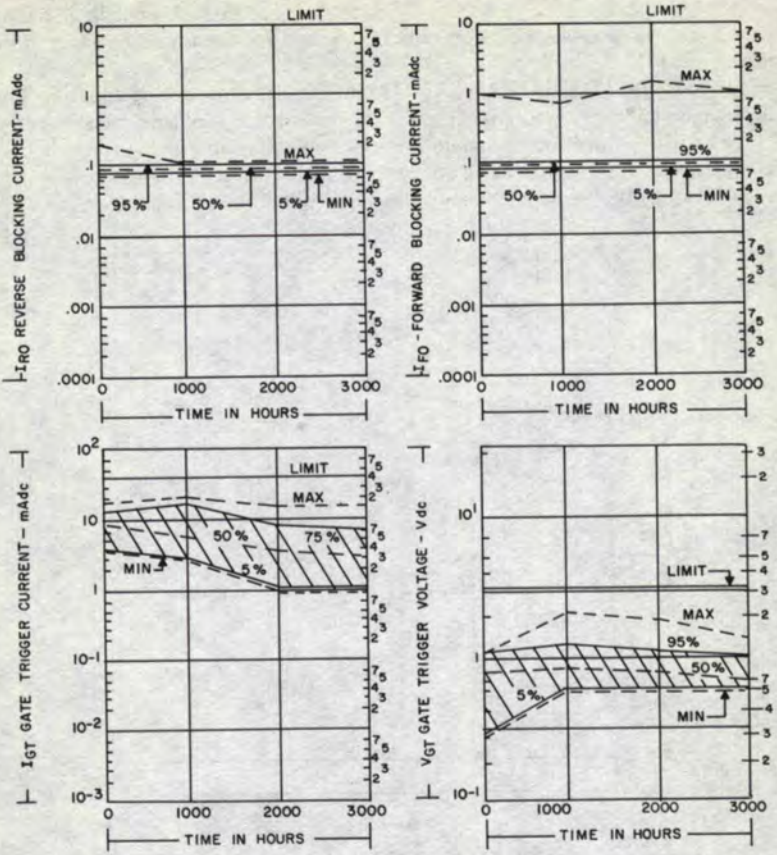


Figure 17.10 Parameter Distributions—C35A Storage Life Per Mil-S-19500/108

Observations over a still longer period of time were made possible through initiation, in 1960, of a test using some of the first commercially produced SCR's. The conditions imposed were random, roughly simulating the conditions such devices might be exposed to over a long period of time in a derated application. Temperature cycling, storage at various ambient temperatures, and sporadic short term operation at low current levels essentially constituted the test conditions.

Forty-nine devices were started into the test cycle, of which three became early failures. One of the failures resulted from a mechanical imperfection, the cause for which was subsequently eliminated through design improvement. The other two were analyzed to be the result of leaks in the hermetic seal. Refinements in housing fabrication and final sealing techniques plus the development of improved sensitivity leak detection methods have since provided effective control over the occurrence of this type of defect.

Observations of the forty-six devices that remained on test indicate that the most significant characteristic being monitored was forward blocking current. Though it is difficult to evaluate the degree of instrumentation error present, it is reasonable to assume that some actual change in blocking current was experienced

with several of the devices. Figures 17.11a and 17.11b show percentile distributions of forward and reverse blocking currents to twelve thousand, five hundred hours of test time.

Figues 17.11c, 17.11d, 17.11e, 17.11f and 17.11g show percentile distributions of gate trigger current, gate trigger voltage, on voltage, holding current, and forward breakdown voltage of the same devices over the same test interval. Because of the sensitivity of these tests to measurement error, actual variances with time are considered to be below the resolution of available instrumentation.

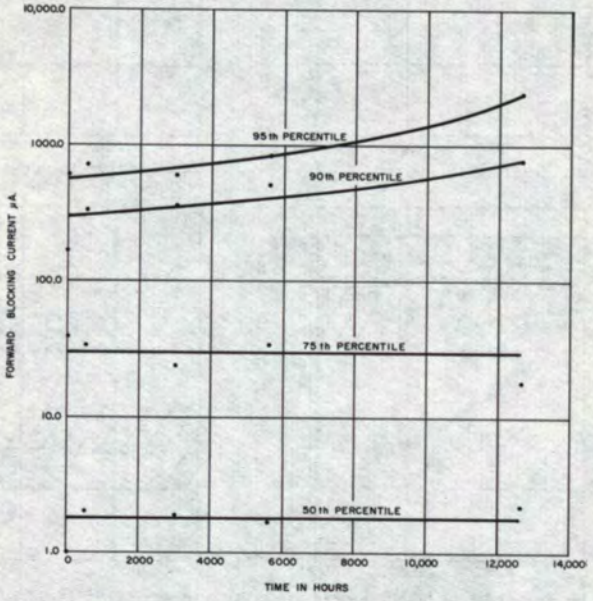


Figure 17.11a Forward Blocking Current (I_{fo}) Versus Time—C35

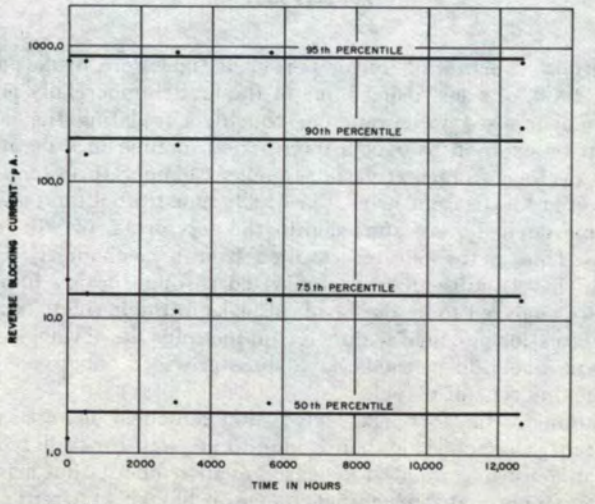


Figure 17.11b Reverse Blocking Current (I_{ro}) Versus Time—C35

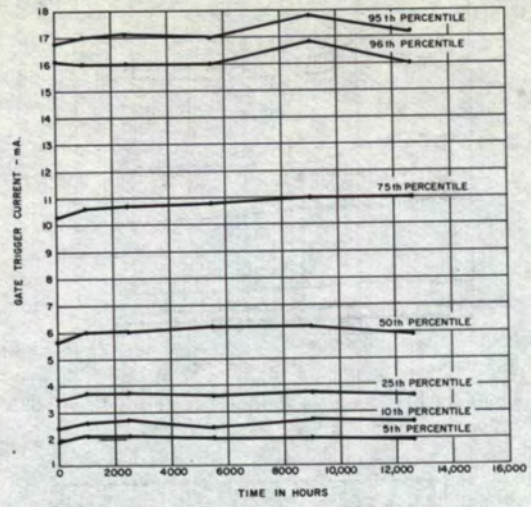


Figure 17.11c Gate Trigger Current (I_{gt}) Versus Time—C35

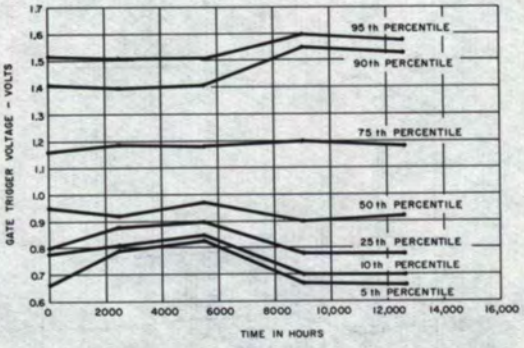


Figure 17.11d Gate Trigger Voltage (V_{gt}) Versus Time—C35

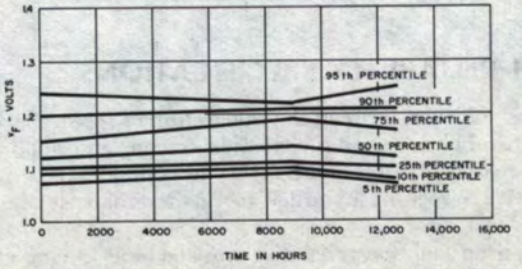


Figure 17.11e Instantaneous on Voltage Versus Time—C35

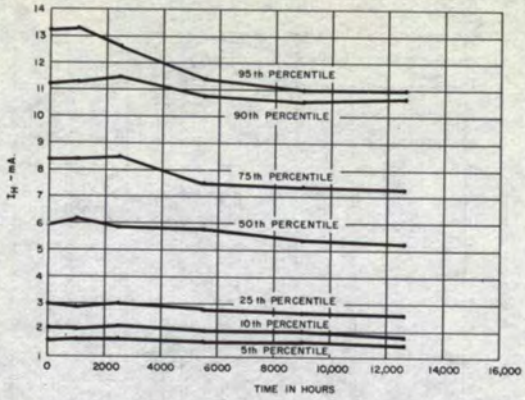


Figure 17.11f Holding Current (I_h) Versus Time—C35

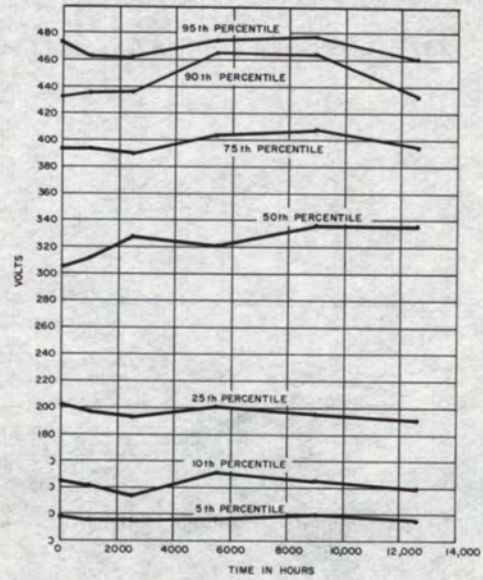


Figure 17.11g Forward Breakover Voltage $(V_{BR})_{FO}$ Versus Time—Combined Sample of C35F and C35A

17.6 HIGH RELIABILITY SPECIFICATIONS

Reliability is achieved through the integration of research, design, production, quality control, evaluation, rating, selective screen, and application. In unusual applications, increased expense and delivery lead time may be justified for special additional selective screening in order to further increase the reliability of the standard device.

It has often been said that reliability must be built in, and cannot be tested in. It is thereby concluded that if the device were as good as it should be, no selective

screening would be necessary. In actuality, the perfect device has not been designed, nor are purchased parts and materials necessarily perfect. The people used to assemble, process, and test devices, while good, are also not necessarily perfect. In a worst case of tolerance extremes, it is possible to produce a small number of discrepant devices. Any test that excludes such a device must be considered to improve the reliability of the population from which that device was removed. A high reliability device specification includes provisions for screen testing as well as failure rate measurement testing.

17.6.1 Selective Screen Tests

A variety of selective screens have been used for different SCR types depending upon characteristics, construction, failure mechanisms, and history of the particular type. Several kinds of common screen tests are listed below:

TEMPERATURE CYCLING—wide range of temperature excursions, usually from maximum to minimum rated storage temperatures.

ELEVATED TEMPERATURE STORAGE—extended exposure to high temperature, usually maximum rated storage temperature or above.

ELECTRICAL PARAMETER SCREENING—elimination of the ends of long tailed distributions to provide ample safety margins within specification limits

LEAK DETECTION—elimination of encapsulation flaws.

BLOCKING BURN-IN—sixty cycle sine wave or rated peak voltage with junction at rated temperature.

17.6.2 Failure Rate Measurement Tests

When time and economics allow, a high reliability specification will include sample life testing of the completed devices, usually under accelerated conditions. Even though these tests may be quite extensive as a result of the statistics of the sampling procedure, their performance in no way changes the reliability of the lots they represent. They are informational only.

When reliability measurement tests are performed, they provide the device manufacturer the opportunity to further evaluate the efficiency of selective screen tests. From the results of comparative evaluations of screening losses versus life test behaviour plus the analyses of the occasional freak failures, the device manufacturer may be able to develop improved or special screening techniques for specific failure mechanisms.

17.6.3 Standard High Reliability Specifications

The General Electric Company has produced and made available standard high reliability specifications for a number of devices. These specifications provide an optimum integration of the essential fundamentals necessary to the achievement of high reliability. Two SCR specifications available at this writing are the C11DR700 (spec. #670.9) which is similar to the C11D(2N1777), and the C35DR700 (spec. #670.8) which is similar to the C35D(2N688).

The specification for each type consists of two parts: a general specification that includes the general requirements with detailed presentations of the measurements and test procedures (spec. #670.6); and a detailed part drawing, as referenced above, specifying parameter limits with associated measurement conditions which pertain to the various tests in the general specification.

Fundamental philosophies included in the specifications are:
1—No requirement or assumption is included that cannot be measured or tested. This applies particularly to acceleration factors. If application stress level, failure definition, and mission time information is supplied, it will be possible for the General Electric Company to estimate a maximum failure rate based on information from various test sources. Since this information is in the form of a complex equation, it is programmed on a computer to provide reliability estimates at actual operating conditions on a custom basis.
2—The proposed JEDEC high reliability format has been followed insofar as possible.
3—The Lambda-LTPD sampling plan developed by JEDEC for MIL-S19500C has been used.
4—It was recognized that failure modes and mechanisms, and the selective screening tests for their removal, vary not only from one device type to another, but from one manufacturer to another. The complete details of the selective screening tests, though included in internal process instructions, are therefore not included on the detailed part specifications. The purpose of the omission is to facilitate implementation of improved screening techniques as they become available.

The screening techniques used are those which give the highest level of failure rate acceleration without introducing new failure mechanisms that would not be encountered during normal use of the devices.

Universal acceptance of standard specifications as described above could be expected to provide major advantages to the users of high reliability parts, including:
1—LOWER FAILURE RATES. More efficient utilization of resources, in terms of both facilities and personnel, could allow more concentrated and effective effort in the areas of product improvement through failure analyses, failure mode and mechanism studies, and screening versus life test evaluations. It could also give better direction to efforts to improve process control, quality control, and design.
2—AVAILABILITY. By its very nature, processing to high reliability specifications is time consuming. By anticipating combined requirements to a known specifications, a manufacturer can complete extensive testing on a programmed basis, with the resulting advantage of reduced delivery cycles.
3—LOWER COST. The standardization of test methods and equipment can contribute to the reduction of costs involved in one hundred percent screening tests. The expense of extensive failure rate measurement testing can be prorated over a larger number of devices than may be required by an individual user at any one time.

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Test Circuits for SCR's

18.1 INTRODUCTION

When it is anticipated that SCR's will be used for production purposes, it is essential that some basic equipment be made available for testing the characteristics of SCR's in the factory. The test circuits in this chapter are intended to serve this purpose and several others, namely:

1. Incoming inspection of SCR's.
2. Troubleshooting SCR circuits.
3. Preventive maintenance.
4. Comparison of SCR's of different types and manufacture.
5. Development of better understanding of SCR characteristics.

18.2 INSTRUMENTATION

The current waveform into, and the current and voltage waveforms out of an SCR circuit may be distorted, due either to the nature of the circuit, e.g., a phase control circuit, or to non-linearities in the SCR itself, e.g., its logarithmic forward voltage drop-current relationship. The selection of proper instrumentation for use in SCR evaluation is therefore of prime importance, if accurate measurement is to be made.

Conventional diode rectifiers and SCR's are rated in terms of *average forward current*, average current being defined as that value of unidirectional current indicated by a DC-reading ammeter placed in series with the diode or SCR. The average value of a waveform should not be confused with its *RMS value*, which is a measure of the heating (I^2R) effect of the waveform in a linear resistance. The ratio of RMS value to average value of any waveform is called its *Form Factor* (F), and F is a function of the ripple content of the wave. For pure (rippleless) DC, $F = 1$, and F increases as the ripple content increases. Thus, the Form Factor of a full wave rectified sine wave is 1.11, but rises to 1.57 for a half wave rectified sine wave.

The type of metering used in a particular SCR circuit will depend on the input voltage to the SCR. If the input is AC, input voltage should be measured in terms of its RMS value. Note that the commonly available types of "RMS reading" meters (VOM's, most VTVM's) only read RMS correctly when the waveform is a pure undistorted sine wave (rectifier-moving coil instruments actually *measure* average current, but are *calibrated* to read RMS as long as $F = 1.11$). There are three types of meter that do measure true RMS, independently of waveshape: the iron vane, dynamometer, and thermocouple type instruments. The dynamometer meter is accurate and reasonable in cost, the thermocouple meter is very accurate but delicate, while the iron vane type, although low in cost, has a limited frequency capability. A typical "chopped" sine wave, as produced by SCR phase control, contains a high percentage of harmonics which may be beyond the frequency range of an iron vane meter. The output "DC" voltage and current of an SCR circuit as well as the current through individual SCR's can be measured with conventional moving-coil instruments. Ripple voltage is best measured with an oscilloscope, or

with an RMS voltmeter in series with a capacitor having low impedance to the ripple compared with the voltmeter. Peak-to-peak voltage is normally read directly from an oscilloscope trace, or with a meter designed to read peak-to-peak values (RCA Senior Voltohmyst WV98C for instance).

18.3 TEST CIRCUITS FOR FORWARD BREAKOVER VOLTAGE, REVERSE VOLTAGE, AND GATE CHARACTERISTICS

18.3.1 $V_{BR(FO)}$, V_{ROM} (rep) and Gate Test Set for all SCR's, Except TO-5 Types

Figure 18.1 illustrates a circuit for testing the forward and reverse blocking characteristics and the gate triggering characteristics of all G-E low, medium, and high current SCR's except the very low current SCR's, LASCR's, and GTO's in the TO-5 package.

This circuit consists of a variable voltage current-limited power supply that develops a half sine wave voltage across the SCR to minimize junction heating.

Instrumentation consists of suitable meters to indicate voltage and current values. An oscilloscope with separate horizontal and vertical inputs can be added to provide a visual display of the forward and reverse voltage-current characteristics. Test procedures are as follows:

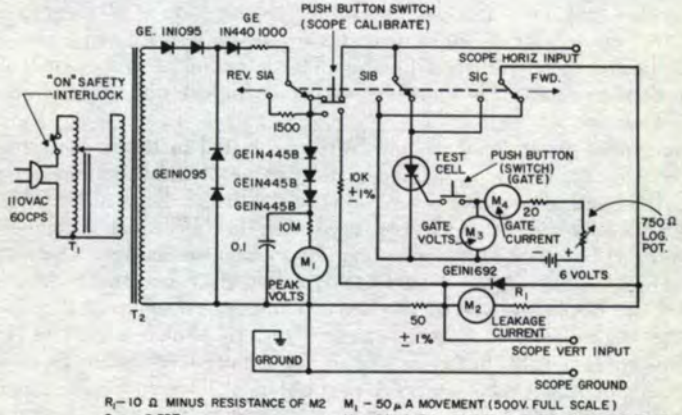


Figure 18.1 Test Set For Measuring $V_{(BR)FO}$, V_{ROM}(rep), and Gate Triggering Characteristics (Except SCR's, LASCR's, and GTO's in the TO-5 Package)

18.3.1.1 Scope Calibration

Horizontal deflection on the scope represents the anode voltage on the SCR. Gain should be adjusted to correlate with the reading on meter M_1. Vertical deflection on the scope is developed by the voltage across the 50Ω resistor, and thus represents anode current. With the "Scope Calibrate" button depressed, peak current in milliamperes through the 50Ω resistor is 0.1 times the reading on meter M_2. Vertical gain should be adjusted for 1 or 10 ma per inch.

18.3.1.2. $V_{BR(FO)}$ Measurement

Switch S_1 to "Forward" position. Raise voltage by means of adjustable transformer T_1. Read $V_{(BR)FO}$ on meter M_1 just prior to breakover as indicated by abrupt rise in reading on M_2 and drop in reading on M_1. Prior to breakover, meter M_2 will read full cycle average leakage current. The scope will trace a plot of the forward voltage/current relationship.

18.3.1.3 I_{GT}, V_{GT} Triggering Measurements

With switch S_1 in the "Forward" position and M_1 at desired level of anode voltage, depress "Gate" button and gradually raise gate current M_4 by adjusting the 750 ohm potentiometer. Read I_{GT} on meter M_4 and V_{GT} on meter M_3 just prior to breakover. To return the SCR to its forward blocking state, reduce gate current.

18.3.1.4 V_{ROM} (rep) and Reverse Leakage Current Measurement

Switch S_1 to "Reverse" position. Raise M_1 to the V_{ROM} (rep) rating of the SCR. Read full cycle average reverse leakage current I_{RO} (AV) on M_2, or peak leakage current on the scope display.

18.3.2 $V_{BR(FX)}$, V_{ROM}(rep) and I_{GT} Test Set for TO-5 Packaged SCR's, LASCR's, and GTO's.

The circuit of Figure 18.2 is suitable for measuring the forward and reverse blocking voltages, and gate triggering characteristics of all controlled rectifiers, light-activated controlled rectifiers and gate turn-off switches in the TO-5 package. Because the leakage currents of these devices are so low, forward and reverse voltage measurements must be made at very low frequency, to minimize errors due to stray capacitance in the test set.

The 2 cps half sine wave supply can be obtained by amplifying and rectifying the output of a low frequency signal generator to 500 volts peak. Test procedure is as follows:

18.3.2.1 Test Oscilloscope Calibration

With switches S_3 and S_2 both in position (1) adjust R_{19} to give a peak voltage reading of 0.5 volts $\pm 5\%$ peak at terminal V; adjust R_{20} to give 1.0 volt $\pm 5\%$ peak at terminal H. A very high impedance voltmeter must be used to set these figures. The test oscilloscope should now be adjusted for 10 centimeter horizontal and 5 centimeter vertical deflection when connected to H and V.

18.3.2.2 $V_{BR(FR)}$ Measurement

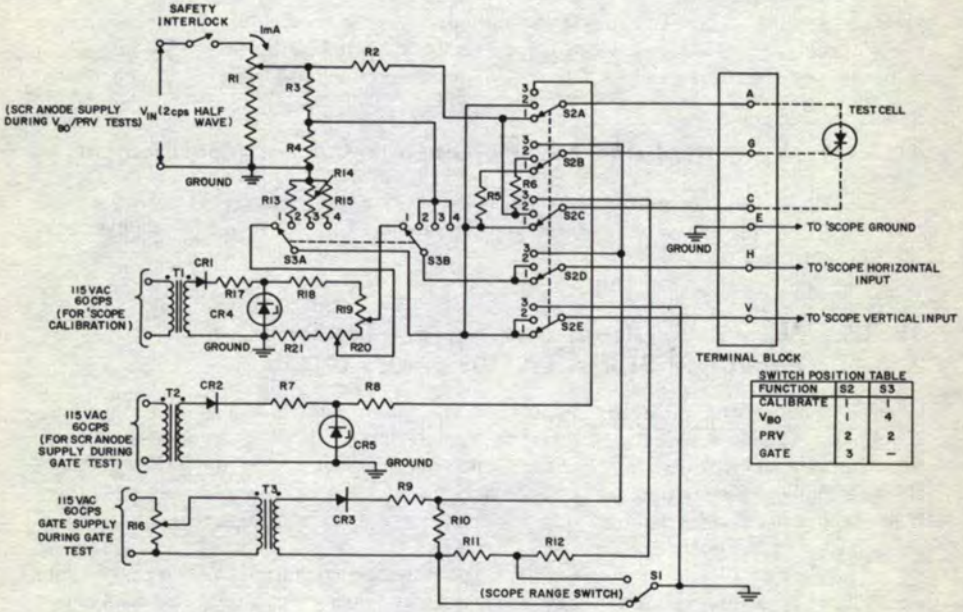
With V_{IN} applied leave S_2 at position (1) and rotate S_3 to (4). Adjust R_1 until cell $V_{BR(FR)}$ is indicated by a sudden increase in forward current. Read off voltage and forward leakage current direct from E-1 display on oscilloscope.

18.3.2.3 V_{ROM}(rep) and Reverse Characteristic

With S_2 at (2) and S_3 at (2) adjust R_1 until oscilloscope trace indicates that rated voltage is being applied to the cell. Read off reverse leakage current at this value of reverse voltage.

18.3.2.4 Gate Characteristic and Cell Triggering Point

V_{IN} is not required for this part of the test. Both anode voltage and gate signals are supplied by self-contained power supplies. Select position (3) on S_2. Increase gate voltage by turning up R_{16} until unit triggers. The oscilloscope now displays the SCR gate characteristic; gate voltage and current to trigger are indicated by a sudden discontinuity in the gate E-I trace.



All resistors 10% unless otherwise specified
R_1 —100K 5 watt carbon potentiometer
R_2 —47K 1 watt
R_3 —1M 1% ½ watt
R_4 —2K 1% ½ watt
R_5, R_6 —Depends on device under test. Equals R_{GK} on Spec. Sheet
R_7 —100 ohm 5 watt
R_8 —600 ohm 1 watt
R_9 —1K 1 watt
R_{10}—100 ohm 1% 1 watt
R_{11}—1800 ohm 1% ½ watt
R_{12}—200 ohm 1% ½ watt
R_{13}—10K 1% ½ watt
R_{14}—2K 1% ½ watt
R_{15}—1K 1% ½ watt
R_{16}—5K 2 watt potentiometer
R_{17}—390 ohm 1% ½ watt
R_{18}—15K 1% ½ watt
R_{19}—Potentiometer 5K ½ watt
R_{20}—Potentiometer 100 ohm ½ watt
R_{21}—390 ohm ½ watt
CR_1, CR_2, CR_3—Rectifier G-E 1N91 (3 required)
CR_4—Zener Diode 22 volt 1 watt
CR_5—Zener Diode G-E 4JZ4X6.2B
T_1, T_2, T_3—Transformer UTC No. FT10 (3 required)
S_1—Switch, SPDT, 110 volt Rotary, Break before make
S_2—Switch, 5P3T, 1000 volt Rotary, Break before make
S_3—Switch, DP4T, 110 volt Rotary, Break before make

Figure 18.2 Test Set for TO-5 Package SCR, GTO and LASCR

18.4 DC FORWARD AND REVERSE LEAKAGE (BLOCKING) CURRENT

The circuit of Figure 18.3 provides a simple and inexpensive means for checking the instantaneous leakage characteristics of SCR's (or rectifiers). Pushbutton S_2 should not be omitted, as it prevents continuous power from being applied to the cell and reduces the possibility of thermal runaway occurring.

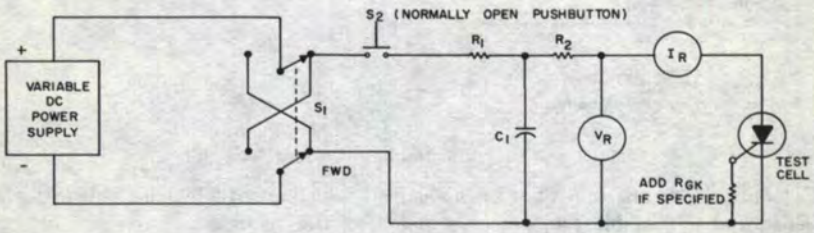
$$(R_1+R_2) = \frac{V_{BR(FO)}}{5\times(\text{Max Fwd Leakage Spec})}$$

or

$$(R_1+R_2) = \frac{V_{ROM}(rep)}{5\times(\text{Max Reverse Leakage Spec})}$$

and

$$R_1 = R_2$$
$$C_1 = 1\mu f \text{ (non-polarized)}$$



$$(R_1 + R_2) = \frac{V_{BR\,(FO)}}{5 \times (\text{MAX. FWD LEAKAGE SPEC})}$$

OR

$$(R_1 + R_2) = \frac{V_{ROM\,(REP)}}{5 \times (\text{MAX REVERSE LEAKAGE SPEC})}$$

AND $R_1 = R_2$

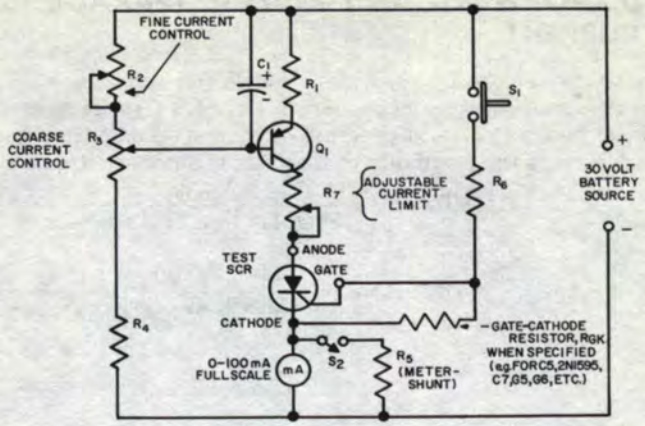
$C_1 = 1\mu f$ (NON-POLARIZED)

Figure 18.3 DC Leakage Current Test

18.5 MEASUREMENT OF HOLDING CURRENT

A simple series circuit consisting of battery, potentiometer, ammeter and test SCR is unsuitable for the measurement of SCR holding current since *smooth* reduction in cell current is not possible with such an arrangement. It has been found that noise and transients generated by a potentiometer as its resistance is increased are sufficient to turn the SCR off at an indicated DC current much higher than its true holding current. The circuit of Figure 18.4 utilizes a transistor as a constant current source to overcome this limitation. This circuit should not be used to measure the holding current of Gate Turn-Off Switches—see end of this section.

R_3 should be set initially so that fairly high current will flow through the test SCR when S_1 is closed. Current is then progressively reduced, at first using R_3, and finally with R_2 as cell current drops towards its specified holding value. S_2 switches a shunt across the meter to give 1000 ma full scale deflection if required.



R_1—10 ohm 10 watt
R_2—10 ohm 25 watt potentiometer
R_3—50 ohm 10 watt
R_4—100 ohm 10 watt
R_5—Shunt for 1000 ma full scale (select to suit meter)
R_6—220 ohm, 1 watt
R_7—50 ohm 25 watt
Q_1—2N174 or equivalent
C_1—100 μf 25 VDC
S_1—Normally open push button
S_2—SPST

Figure 18.4 SCR Holding Current Test Set

Holding current can also be measured satisfactorily by substituting a *fixed* resistor and a variable DC power supply for the transistor current source and fixed power supply of Figure 18.4. Variable DC can be obtained directly from a commercial power supply or alternatively from a variable transformer supplying a simple rectifier bridge-filter arrangement. Holding current may vary slightly with supply voltage. This type of test is recommended for measurement of Gate Turn-Off Switch holding current.

18.6 AVERAGE FORWARD VOLTAGE ($V_{F\,AVG}$) TEST SET

The circuit of Figure 18.5 can be used to test the forward voltage drop of the SCR in the conducting state. In this test, the SCR is subjected to a DC current as read by meter M_1, and the voltage drop across the SCR is measured by meter M_2. To make the measurement, close S_1 with T_1 in a position approximately midway between the end positions. Adjust T_1 to the level of current desired on M_1. Read M_2 by depressing S_2. These readings should be less than the maximum values specified on the forward characteristic curves in the specification bulletin for the particular device. A current level somewhere near the continuous duty current rating of the SCR is recommended. If the SCR is not attached to a heatsink for this measurement, the readings should be completed within two or three seconds to prevent overheating of the cell. The foregoing tests can be conducted at any ambient temperature within the operating range provided that the ratings at the stud temperature are not exceeded.

Special oscilloscopes such as the Tektronix Type 575A which are designed to trace transistor characteristic curves may be used for checking the triggering characteristics and holding current requirements of SCR's. The power supply in the Tektronix 575A limits maximum anode voltage to 400 volts positive or negative.

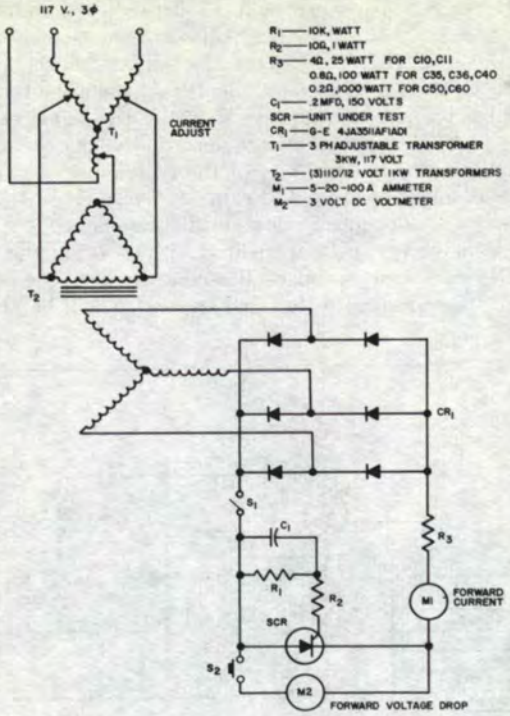


Figure 18.5 Forward Voltage Drop Test Set

18.7 TURN-OFF TIME TEST CIRCUIT

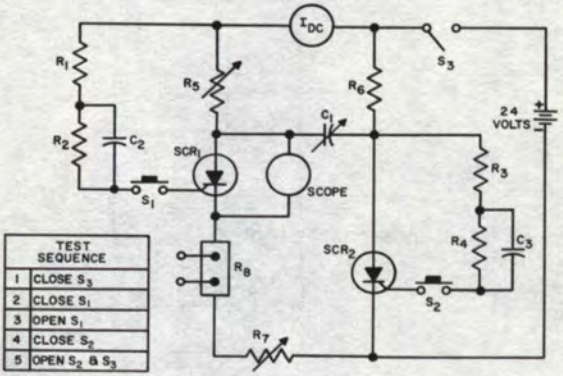
As discussed in Chapter 5, the turn-off time depends on a number of circuit parameters. Thus, a turn-off time specification inherently must include the precise value of these circuit parameters to be meaningful. Accordingly, specifications for General Electric SCR's with guaranteed turn-off limits list the applicable circuit parameters and show the test circuit which will apply these parameters to the SCR. For this information, the reader is referred to the specification bulletin for the SCR under consideration (e.g., C9, C12, C40, C55).

For general turn-off time test work, the type of circuit shown in Figure 18.6 can be used for low, medium, and high current SCR's by proper manipulation of the circuit constants. Forward load current is adjustable by R_5 from approximately ½ ampere to 70 amperes and the length of time SCR_1 is reverse biased during the turn-off cycle can be adjusted by manipulating R_5 and C_1. The peak reverse current during the recovery period can be adjusted by R_7 and this current can be viewed on a scope by monitoring the voltage across a non-inductive shunt R_8. If one is interested in only one particular load current range, there is of course no necessity in providing the complete range of resistors and capacitors specified in Figure 18.6.

This test circuit subjects the SCR to current and voltage waveforms similar to those found in a parallel inverter circuit. Closing S_1 and S_3 fires SCR_1, the unit under test, so that load current flows through R_5 and the ammeter. In less than a second C_1 charges through R_6 to the voltage being developed across R_5 by load

current flow. If S_2 is now closed, SCR_2 turns on. This applies C_1 across SCR_1 so that the current through SCR_1 is reversed. C_1 furnishes a short pulse of reverse recovery current through SCR_1 until this SCR recovers its reverse blocking ability. After this initial pulse of current, C_1 continues its discharge through SCR_2, the battery, and R_5 at a rate dependent on the time constant of R_5C_1. After a time interval, t_1, in Figure 18.7, somewhat less than the R_5C_1 time constant, the anode to cathode voltage of SCR_1 passes through zero and starts building up in the forward direction. If the turn-off time, t_{off}, of the SCR is less than t_1, it will remain turned off and the ammeter reading will return to zero. If not, the SCR will turn back on and current will continue to flow until S_3 is opened.

The turn-off interval t_1 can be measured by observing the anode to cathode voltage across SCR_1 on a high speed oscilloscope such as the Tektronix 545A or equivalent. A waveshape similar to that in Figure 18.7 will be observed.



TEST SEQUENCE	
1	CLOSE S_3
2	CLOSE S_1
3	OPEN S_1
4	CLOSE S_2
5	OPEN S_2 & S_3

R_1, R_3 — 100 OHMS, 1 WATT
R_2, R_4 — 1 MEG, 1 WATT
R_5 — VARIABLE RESISTOR, 0.25Ω, 2.5KW TO 50Ω, 15 WATT
R_6 — 1000Ω, 2 WATT
R_7 — 0.1Ω, 500W TO 1Ω, 10 WATT
R_8 — NON-INDUCTIVE SHUNT (IF USED)
C_1 — 0.1–100μfd PAPER CAPACITORS, 150 VOLTS
C_2, C_3 — 0.5μfd – 200 VOLT PAPER CAPACITORS
SCR_1 — TEST CONTROLLED RECTIFIER
SCR_2 — C 22F

Figure 18.6 Turn-Off Time (t_{off}) Test

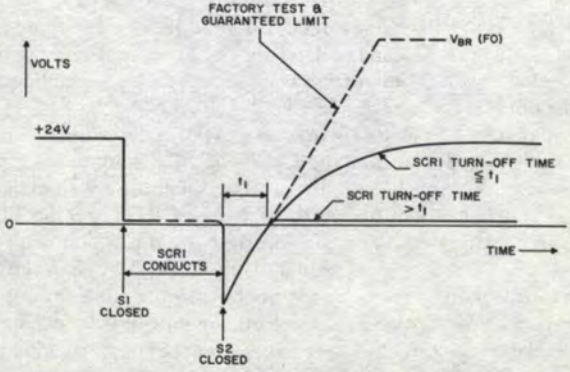


Figure 18.7 Voltage Across SCR_1 During Turn-Off Time Test

Satisfactory operation of this circuit requires careful attention to detail. The DC source must have good regulation if C_1 is to develop ample commutation voltage

for turning off SCR_1. In order to minimize circuit inductance, power leads should be heavy copper braid when testing medium and high current SCR's and lead lengths should be held to an absolute minimum.

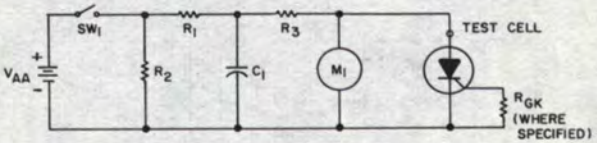
Turn-off time testing in the General Electric factory is performed with a fixed rate of rise of reapplied forward voltage as indicated by the dashed line in Figure 18.7. This is a more severe test on the SCR than the exponential curve and it requires considerably more elaborate test equipment than in Figure 17.6. For those who wish to test under these conditions, information on the factory test circuit will be provided upon request. (Ref. 1)

18.8 dv/dt TEST

The forward blocking capability of an SCR, GTO or LAS is sensitive to the rate at which the forward blocking voltage is applied. If the rate of rise exceeds a critical value, switch-on will occur, even though the applied voltage is less than the *static* breakover voltage of the device. For energization of a device from rest with an exponentially rising voltage waveform, the numerical value of dv/dt is computed as follows:

$$dv/dt = \frac{\text{Applied Forward Voltage}}{\text{Exponential Time Constant}} \times .63$$

Where this parameter appears on the device specification sheet, it enables the circuit designer to design filters to prevent false triggering. Figure 18.8 illustrates a simple circuit to check the dv/dt capabilities of p-n-p-n devices.



V_{AA} = ANODE VOLTAGE SUPPLY, VARIABLE
SW_1 = MERCURY WETTED RELAY
R_1 = NON-INDUCTIVE RESISTOR
R_2 = DISCHARGE RESISTOR
R_3 = CURRENT LIMITING RESISTOR
R_{GK} = GATE TO CATHODE RESISTOR (WHERE SPECIFIED e.g. C5, C7, G5, G6, L8, L9 etc.)
C_1 = CAPACITOR
M_1 = DC VOLTMETER OR OSCILLOSCOPE

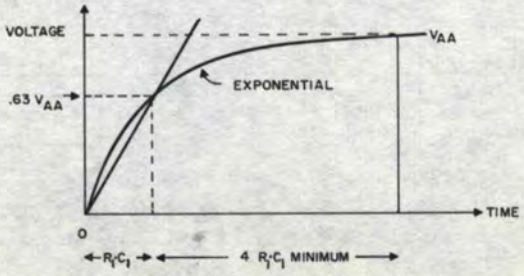


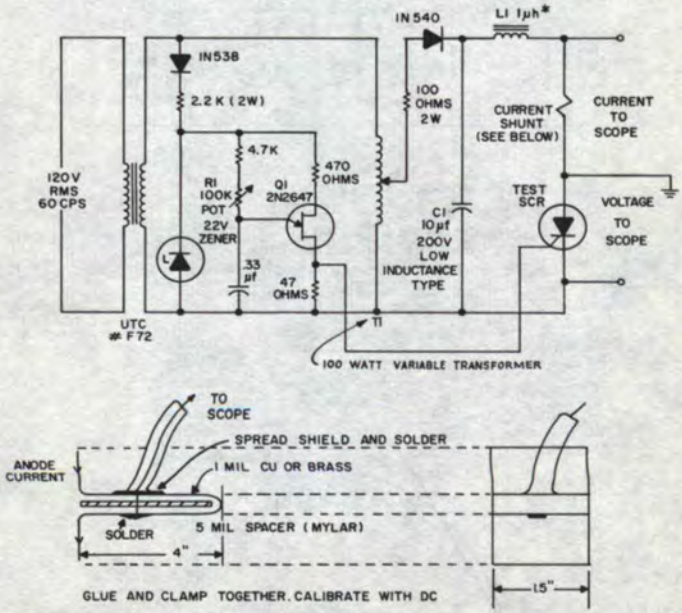
Figure 18.8 dv/dt Test Set

The switch SW_1, if it is not of the mercury wetted type, must have a closure time (including bounce) of not more than .1 R_1 C_1. R_3 is a current limiting resistor to prevent damage to the device under test in the event of dv/dt triggering.

With the gate open-circuited, or with the specified bias conditions operable, an exponential voltage waveform is applied across the test cell each time SW_1 closes. The test is a GO-NO GO test performed by increasing the supply voltage until the device under test switches on, or until the specified voltage limit value is reached without switching. The exponential waveform may be observed by connecting an oscilloscope directly across the test cell.

18.9 di/dt TESTING

The circuit of Figure 18.9 may be used to gauge the ability of an SCR to switch high current loads satisfactorily. This is known as its "di/dt" capability. When an SCR is gate triggered, it turns on initially only in the region nearest the gate contact, and the turned-on portion then spreads laterally to encompass the entire pellet area. Until the whole pellet is in conduction, any load current through the SCR concentrates in the turned-on portion, effectively limiting the maximum current-carrying ability of the SCR for the first microsecond or so after triggering. Since the forward voltage drop of an SCR is proportional to current density, it is possible to compare the switching characteristics of a batch of devices by measuring their individual forward voltage drops at a standard current level and time interval subsequent to triggering. In the circuit as shown, the UJT (Q_1) oscillator frequency is set by means of R_1 so that the test SCR triggers sometime after the peak of the 60 cps input sine wave. Transformer T_1 is then adjusted until the peak



* L_1 includes stray inductance of main discharge loop (C_1, L_1 and test SCR). The discharge loop leads should be as short and heavy as possible to minimize losses.

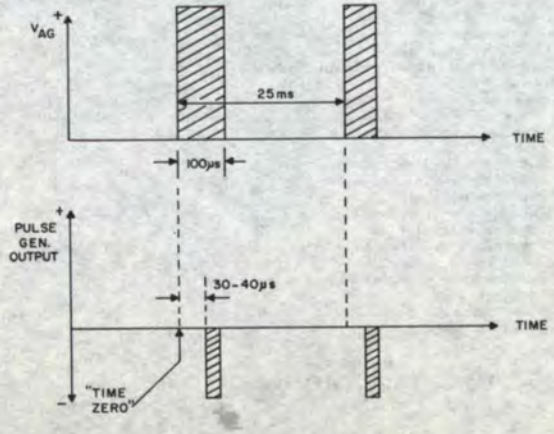
Figure 18.9 di/dt Test Circuit

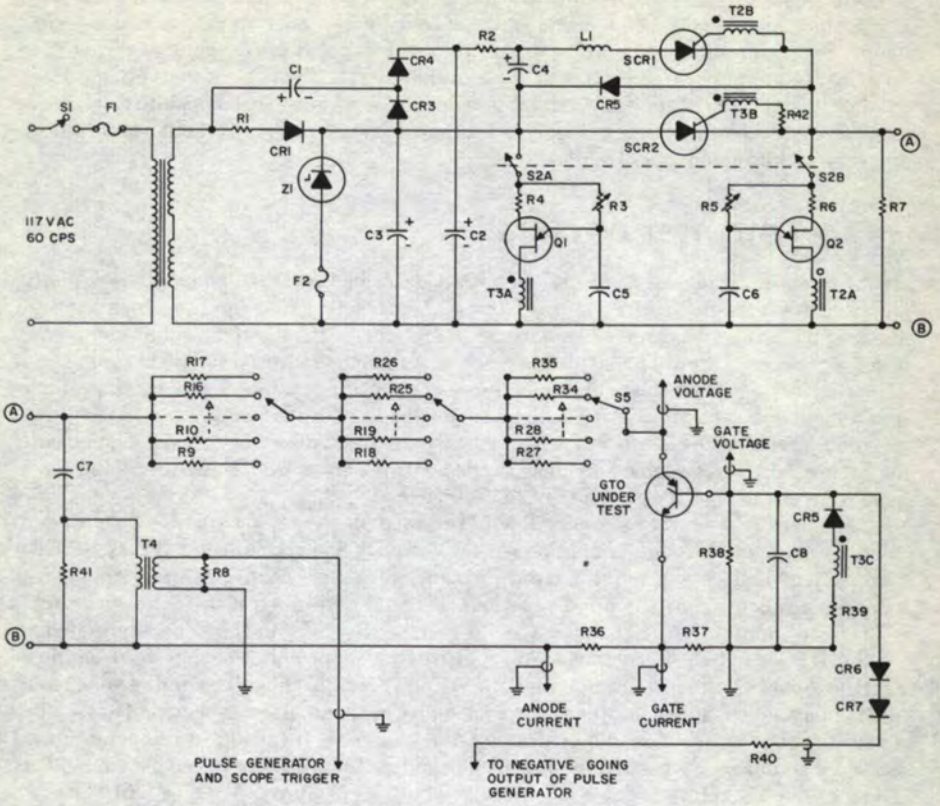
magnitude of the 10 microsecond wide half sine wave resonant discharge current pulse that ensues is 150 amperes, as measured by the current probe and oscilloscope. By taking measurements at the peak of the current pulse, voltage errors due to stray inductance in the circuit are eliminated. The SCR forward voltage drop at the 150 ampere standard current is a measure of its di/dt capability. Care is needed in the connections of the voltage and current probes to avoid errors due to stray pickup from ground loops.

18.10 GTO TEST CIRCUITS

Standard SCR test gear, of the type described in this chapter, is equally suitable for measuring the majority of GTO characteristics, such as forward and reverse blocking voltage, leakage current, gate trigger parameters, holding current, etc. In general, the only piece of special test equipment required for GTO evaluation will be a turn-off gain test set. Since most GTO's are capable of conducting much higher currents on a pulse basis than their steady state DC dissipation will allow, turn-off gain measurements must usually be performed on a pulse basis. The circuit of Figure 18.10 is suitable for checking levels up to and well above the 2 amperes peak current capability of the G5 & G6 devices.

Capacitor C_3 serves as a very low impedance anode supply for the GTO under test. C_3 is charged to and is clamped at 30 volts DC via transformer T_1, diode CR_1 and zener diode Z_1. Each time unijunction transistor Q_1 fires it triggers SCR_1, which connects C_3 to the anode of the GTO under test. Q_1 also triggers the test GTO into conduction. Capacitor C_7 and resistor R_{41} differentiate the leading edge of the GTO anode voltage waveform, and this pulse provides a time-zero marker for the turn-off pulse generator and the display oscilloscope. The pulse generator time delay is set so that 30–40 microseconds elapses after time-zero before the turn-off pulse starts. This allows time for the charge distribution in the conducting GTO to stabilize. Gate current magnitude and pulse width required to turn-off a given anode current can be read directly from the oscilloscope trace. All turn-off gain testing at the factory is done with a standard 10 microsecond wide turn-off pulse. The anode current level is set by means of resistors R_9–R_{35}. Unijunction transistor Q_2 is set to fire 100 microseconds after Q_1 has fired. Q_2 triggers SCR_2 and SCR_2 in turn commutates SCR_1. With SCR_1 "off," anode voltage is removed from the test GTO. This prevents overheating of the GTO at high peak current levels, should it fail to turn-off when the negative gate pulse is applied. Over-all repetition interval is set by means of R_3 to be not less than 25 milliseconds.





S_1—SPST toggle switch
S_2—DPST toggle switch
S_3, S_4, S_5—Ten position 1 pole rotary heavy duty shorting switch
Q_1, Q_2—G.E. 2N2647 unijunction transistor
SCR_1, SCR_2—G.E. C20B SCR
T_1—UTC No. FT10 or equivalent transformer
T_2, T_3—UTC No. H51 pulse transformer
Z_1—Zener diode (2 G.E. 1N1775 in series)
C_1, C_2—10 μf 200 V capacitor
C_3—10,000 μf 40 V capacitor
C_4—1 μf 200 V capacitor
C_5—1 μf 200 V capacitor
C_6—.1 μf 200 V capacitor
C_7—.01 μf 200 V capacitor
C_8—.025 μf 200 V capacitor
CR_1—CR_4—G.E. 1N538 Rectifier diode
CR_5—CR_7—G.E. 1N4150 Fast recovery signal diode
F_1—Fuse ½ ampere
F_2—Fuse ½ amperes
L_1—10 μH choke
R_1—1 ohm 2 watt carbon resistor
R_2—3.3 k 1 watt carbon resistor
R_3—50 k 1 watt carbon pot (locking)
R_4, R_6—470 ohm 1 watt carbon resistor
R_5—5 k 1 watt carbon pot (locking)
R_7, R_{40}, R_{39}, R_{42}—100 ohm 2 watt carbon resistor
R_8—470 ohm 2 watt carbon resistor
R_9-R_{17}—100 ohm 5 watt Sprague Koolohm 453E resistor
R_{18}-R_{26}—10 ohm 5 watt Sprague Koolohm 453E resistor
R_{27}-R_{35}—1 ohm 5 watt Sprague Koolohm 453E resistor
R_{36}—1 ohm 5 watt carbon resistor
R_{37}—IRC 15 watt pulse probe 10 ohm
R_{38}, R_{41}—1 k 1 watt carbon resistor

Figure 18.10 GTO Turn-Off Gain Tester

18.11 COMMERCIAL SCR TEST EQUIPMENT

There are several manufacturers who offer ready-made SCR test gear for use by OEM's and others. These manufacturers should be contacted directly for details of their respective equipments. A partial listing of such manufacturers follow.

Baird-Atomic Inc.
33 University Road
Cambridge 38, Mass.

Owen Laboratories Inc.
55 Beacon Place
Pasadena, Calif.

Power-Radiation Inc.
Box 616
Suffern, N. Y.

Seco Electronics Inc.
1201 S. Clover Dr.
Minneapolis 20, Minn.

Solitron Devices, Inc.
Norwood, N. J.

18.12 IEEE TEST STANDARDS

The Semiconductor Components Committee of the IEEE is presently preparing a Standard for Semiconductor Controlled Rectifiers. At this writing (Fall 1963) no Standard has been issued.

REFERENCE

1. "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers," R. F. Dyer and G. K. Houghton, AIEE CP 61–301.
2. "Portable SCR and Silicon Rectifier Tester," Application Note 201.3, available from General Electric Co., Auburn, N. Y.

Selecting The Proper SCR

A glance at the SCR specifications in Chapter 20 shows that the designer has available to him a variety of SCR's of different current and voltage ratings (from a few hundred milliamperes to over 400 amperes and up to 900 volts). Also, he has special SCR's with guaranteed turn-off times for certain applications such as inverters, as well as SCR's that can be triggered by light, and turned off by suitable gate signals.

To apply the SCR correctly, none of its ratings should be exceeded. By the same token it would be uneconomical to apply the device too conservatively. Since SCR ratings and characteristics, as is customary for semiconductors, are specified as maximum or minimum values (worst case), the designer must determine which of the parameters specified are limiting to his particular application. In this manner he is not penalized by application practices that may have been established in other industries. Each parameter is given at its limit, allowing the designer to determine for himself which one is limiting.

The limiting parameter in most applications is usually one like average or RMS current, non-recurrent surge current, operating temperature, turn-off time, or voltage, not to mention environmental or mechanical requirements. The chart introducing Chapter 20 can conveniently be used to check some of the important parameters against available SCR's.

The following is a check list of the steps that should be taken or considered in selecting the proper SCR.

1. *Determine Circuit Requirements on SCR*

   Voltage across and current through the SCR must be determined in terms of circuit input and output requirements. Figure 19.1 shows these for some common SCR circuits.

   Note: Check *voltage transients* (Chapter 14.)

   Check current carrying capability required if *current waveform is irregular* (Chapter 3).

2. *Select Proper SCR*

   Refer to introductory chart and detailed specifications in Chapter 20. Use voltage and current requirements as determined in step (1).

3. *Determine Proper Heatsink*

   a. *Check* maximum allowable ambient temperature if a *lead mounted* SCR was selected.

   b. *Select* proper size *heatsink* from *fin curves* given on specification bulletin for *stud-mounted* SCR's.

   c. *Determine* proper size *heatsink* from *Chapter 16* if *fin curves* are *not given* for a *stud-mounted* SCR.

4. *Design Triggering Circuit*

   See *Chapter 4* for SCR triggering requirements and design criteria. Also, there are commercially available packaged triggering circuits of both the magnetic and unijunction type triggering.

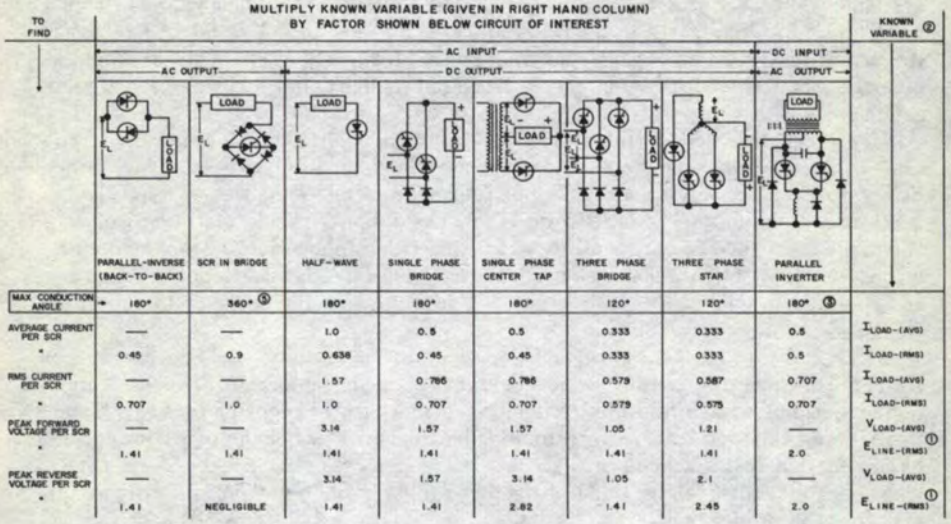
5. *Design Fault Protection*

   Protect SCR's and associated semiconductor components against short-circuit and other fault conditions if required; see Chapter 13. In some ap-

plications economic factors and industry practice may preclude or not require protective circuitry coordination.

Beyond these elementary steps there are often other considerations meriting special attention:

1. Series and parallel operation—Chapter 6.
2. Radio interference and interaction—Chapter 15.
3. Frequency response—Chapters 3 and 5.



① PER TRANSFORMER LEG WHERE TRANSFORMER IS SHOWN.
② WITH NO TRIGGERING ANGLE DELAY
③ ASSUMED PERFECT SQUARE-WAVE OUTPUT.
④ MINIMUM REQUIRED CELL CAPABILITY. ACTUAL VALUE SELECTED MUST BE DETERMINED BY CIRCUIT DESIGNER ON BASIS OF KNOWN AND POTENTIAL VOLTAGE TRANSIENTS.
⑤ WHERE THIS 360° "FULL WAVE" CONDUCTION ANGLE IS NOT GIVEN ON SPECIFICATION BULLETIN USE 180° CONDUCTION ANGLE STUD TEMPERATURE CURVE AND INCREASE CURRENT AS FOLLOWS (CURVES AVAILABLE UPON REQUEST):

SCR TYPE	APPROX. INCREASE
C11	50%
C20	50%
C35	30%
C45	30%
C45	30%
C50	30%
C60	30%
C80	40%

⑥ VALUES PERTAIN TO RESISTIVE LOADING.

Figure 19.1 Circuit Constants for Common SCR Circuits

General Electric Semiconductor Specifications

The following pages list condensed specifications of the General Electric line of Silicon Controlled Rectifiers (SCR's), rectifiers, and zener diodes at the time of publication of this Manual. Also shown are abbreviated specifications for the Unijunction Transistors used in SCR trigger circuits. For the latest detailed specification information, please request the specification bulletin for the particular type of interest.

For a definition of the terms used in the specifications that follow please refer to Chapter 2.

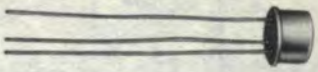
The following chart is offered as an index to the G-E line of SCR's:

SCR SPECIFICATION INDEX

G.E. Type No.	JEDEC Type No.	Devel. Type No.	Max. Avg. Single Phase Current $I_{F(AV)}$	Max. RMS Current If	Operating Junction Temp. °C		Max I_{GT} Required to Trigger +25°C	Guaranteed Turn-off Time**, t_{off} u sec	V_{ROM} (rep) and $V_{(BR)F}$ Up to	Housing Design	Outline No.	Complete Specification Sheet No.	Condensed Specs. on Page
					Max	Min							
C5	2N2322-2329	ZJ203	1.0	1.6	125	−65	200 ua		400	Single End Lead Mounted	1	150.10	330
C7	2N2344-2348		1.0	1.6	100	−65	20 ua		200	Single End Lead Mounted	1	150.11	332
—	2N1595-1599 (Similar to C5, major difference I_{GT})						10 ma		400	Single End Lead Mounted	1	150.15	
C8	2N1929-1935	ZJ209	2.0	2.7	125	−65	15 ma		300	Double End Lead Mounted	2	150.12	334
C9	Fast Turnoff Type		2.0	2.7	125	−65	15 ma	12	300	Double End Lead Mounted	2		336
C10	2N1770A-1777A	ZJ54A	4.7	7.0	150	−65	15 ma		400	7/16 " Hex Stud	3	150.20	338
C11	2N1770-1778 2N2619	ZJ54L	4.7	7.0	125	−65	15 ma		600	7/16 " Hex Stud	3	150.21	340
C12	Fast Turn-off Type		4.7	7.0	125	−65	15 ma	12	400	7/16 " Hex Stud	3	150.25	342
C20 & C22		ZJ226	4.7	7.4	100	−25	25 ma		400	½ " Knurl	4	150.30	344
C30 & C32		ZJ230	12	18	100	−40	50 ma		400	½ " Knurl	4		346
C35	2N681-692*	ZJ39A	16	25	125	−65	40 ma		800	9/16 " Hex Stud	5	160.20	348
C36	2N1842-1850	ZJ39L	10	16	100	−40	80 ma		800	9/16 " Hex Stud	5	160.21	350
C38			23	35	150	−65	40 ma		500	9/16 " Hex Stud	5	160.30	352
C40	Fast Turn-off Type		16	25	125	−65	40 ma	12	500	9/16 " Hex Stud	5	160.25	354
C45 & C46		ZJ246	35	55	125	−45	70 ma		900	1 1/16 " Hex Stud	6 & 7	170.17	356
C50	2N1909-1916	ZJ50L	70	110	125	−40	70 ma		900	1 1/16 " Hex Stud	7	170.20	358
C52	2N1792-1798		70	110	125	−40	70 ma		900	1 1/16 " Hex Stud	6	170.1	
										Flag Cathode			
C55 & C56	Fast Turn-off Type		70	110	125	−40	70 ma	20	300	1 1/16 " Hex Stud	7 & 6	170.21	360
C60 & C61	2N2023-2030	ZJ50B	70	110	150	−65	70 ma		400	1 1/16 " Hex Stud	7	170.26	362
C150		ZJ260	70	110	125	−40	125 ma		1100	1 1/16 " Hex Stud	7		364
C80	2N2542-2548	ZJ204	150	235	125	−40	100 ma		700	1 1/4" Hex Stud	8	170.50	366
C85	Fast Turn-off Type		150	235	125	−40	100 ma	25	700	1 1/4" Hex Stud	8	(See C80 Spec)	
6RW71			300	470	125	−40	150 ma		600	1 5/8" Hex Stud	9	170.60	368
L8 & L9	Light Activated	ZJ227	1.0	1.6	100	−65	220 ua		200	Single End Lead Mounted	1	190.10	370
G5 & G6	Gate Turn-off	ZJ224	.25	1.4	100	−65	10 (G5) 20 (G6)		400	Single End Lead Mounted	1	150.60	372

*USN Specifications 2N681-688 Mil-S-19500-108 available.
**Under specified test conditions.
†No $V_{(BR)F}$ specified above 125°C.

C5U—C5D, C511 (Diamond Base*) Series



High Sensitivity Low Current SCR
1.6 Amperes RMS Max.
Outline Drawing No. 1

The C5 Silicon Controlled Rectifier is an all diffused three junction semiconductor device for use in low power switching and control applications.

This series conforms to the JEDEC TO-5 package outline.

- All diffused
- High gate sensitivity
- Single ended package ideal for printed circuit applications
- Designed to meet MIL-S-19500/276 (Navy)
- Low holding current
- Broad voltage range

TYPE†	PEAK FORWARD BLOCKING VOLTAGE, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ OHMS	WORKING AND REPETITIVE PEAK REVERSE VOLTAGE V_{ROM} (wkg) and V_{ROM} (rep) $T_J = 65°C$ to $+125°C$	NON-REPETITIVE PEAK REVERSE VOLTAGE, V_{ROM} (non-rep) (<5 Millisec.) $T_J = -65°C$ to $+125°C$
C5U (2N2322)	25V	25V	40V
C5F (2N2323)	50V	50V	75V
C5A (2N2324)	100V	100V	150V
C5G (2N2325)	150V	150V	225V
C5B (2N2326)	200V	200V	300V
C5H (2N2327)	250V	250V	350V
C5C (2N2328)	300V	300V	400V
C5D (2N2329)	400V	400V	500V

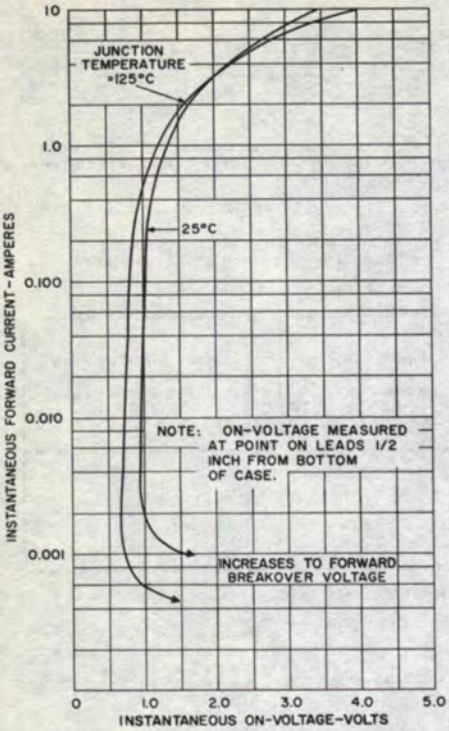
MAXIMUM ALLOWABLE RATINGS

Peak Forward Voltage, PFV . . . . . 500 Volts
RMS Forward Current, On-state . . . . . 1.6 Amperes
Average Forward Current, On-state . . . . . Depends on conduction angle (see charts 2 and 3)
Peak One-Cycle Surge Forward Current (Non-repetitive)
I_{FM} (surge) . . . . . 15 Amperes
I^2t (for fusing) . . . . . 0.5 Ampere² seconds (for times > 1.5 milliseconds)
Peak Gate Power, PGM . . . . . 0.1 Watt
Average Gate Power, PG (AV) . . . . . 0.01 Watt
Peak Gate Current, I_{GFM} . . . . . 0.1 Ampere
Peak Gate Voltage, Forward & Reverse, V_{GFM} & V_{GRM} . . 6 Volts
Storage Temperature, T_{stg} . . . . . −65°C to +150°C
Operating Temperature, T_J . . . . . −65°C to +125°C
Peak non-recurrent surge forward current during turn-on time interval (current rise time = 5.0 sec minimum) . . . . . 40 Amperes

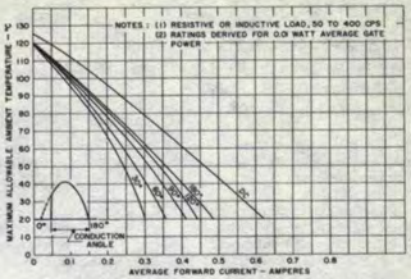
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Reverse or Forward Blocking Current	I_{RX} or I_{FX}	. . . . .	2.0	10.0	μAdc	$V_{RX} = V_{FX}$ = Rated V_{ROM} (rep) Value, T_J 25°C, R_{GK} = 1000 Ohms
		. . . . .	40	100	μAdc	T_J = 125°C, R_{GK} = 1000 Ohms
Gate Trigger Current†	I_{GT}	. . . . .	10.0	200	μAdc	T_J = 25°C, V_{FX} = 6Vdc, R_L = 100 Ohms
		. . . . .	20.0	350	μAdc	T_J = −65°C, V_{FX} = 6Vdc, R_L = 100 Ohms
Holding Current	I_{HX}	. . . . .	1.0	2.0	mAdc	R_{GK} = 1000 Ohms T_J = 25°C, R_L = 10K
		. . . . .	1.5	3.0	mAdc	T_J = −65°C, R_L = 10K
		0.15	0.4	. . . . .	mAdc	T_J = 125°C, R_L = 50K
Circuit-commutated Turn-off Time	T_{off}	. . . . .	40	. . . . .	μsec	T_J = 125°C, I_{FM} = 1.0A, I_R (Recovery) = 1.0A, Reapplied V_{FXM} = Rated V_{FXM} Value, Rate of Rise of Reapplied V_{FXM} = 20 Volts per μsec, R_{GK} = 100 Ohms

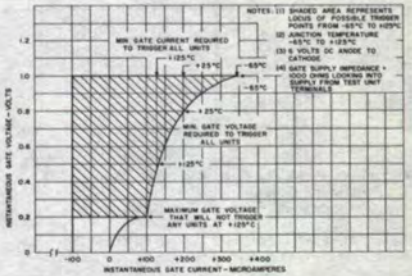
*The C511 is identical to the C5 series except that its base is soldered to a diamond base flange. See full specification sheet.
†For a gate trigger current of 20 μa maximum at T_J = 25°C and 75 μa maximum at −65°C (R_{GK} = 2000 ohms), specify the 2N2322A-2N2328A series.



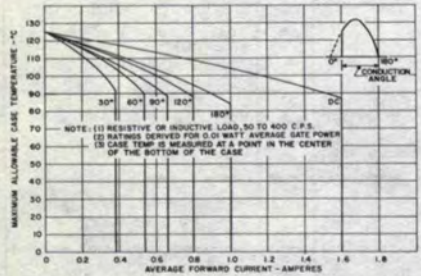
1. Maximum Forward Characteristics—On-State



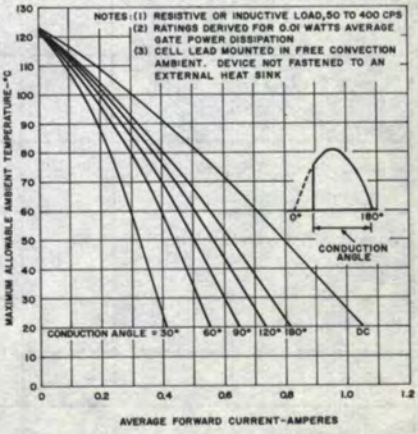
3. Maximum Allowable Ambient Temperature For Sinusoidal Current Waveform



4. Gate Triggering Characteristics For C5 (2N2322-29) Only



2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



5. Maximum Allowable Ambient Temperature For Half Wave Rectified Sine Wave Of Current (Diamond Base)

C7U–C7B

(TYPE 2N2344–2N2348)
Very High Sensitivity Low Current SCR
1.6 Amperes RMS Max.
Outline Drawing No. 1

The C7 Silicon Controlled Rectifier is an all diffused three junction semiconductor device for use in low power switching and control applications. The C7 features maximum gate sensitivity and high external gate-cathode shunting resistance.

This series conforms to the JEDEC TO-5 package outline.

- All welded construction
- Glass to metal seals
- Low holding current
- All diffused
- Extremely high gate sensitivity (I_{GF} =20 μa)
- Single-ended package ideal for printed circuit applications

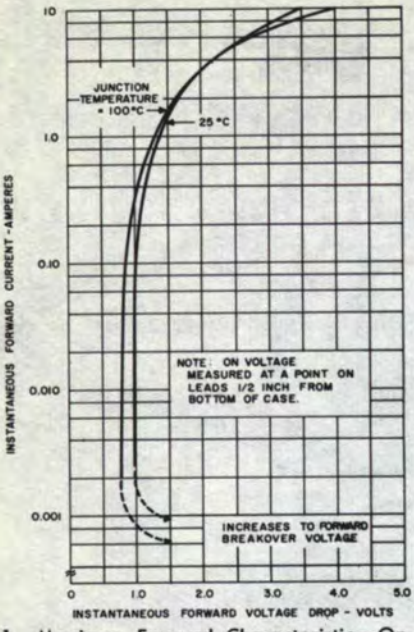
Type	Minimum Forward Breakover Voltage *$V_{(BR)FR}$ T_J = −65°C to +100°C R_{GK} =40,000 ohms	Repetitive Peak Reverse Voltage V_{ROM} (rep) T_J = −65°C to +100°C	Non-repetitive Peak Reverse Voltage V_{ROM} (non-rep) (<5 Millisec.) T_J = −65°C to +100°C
C7U (2N2344)	25V	25V	40V
C7F (2N2345)	50V	50V	75V
C7A (2N2346)	100V	100V	150V
C7G (2N2347)	150V	150V	225V
C7B (2N2348)	200V	200V	300V

MAXIMUM ALLOWABLE RATINGS (ALL TYPES)

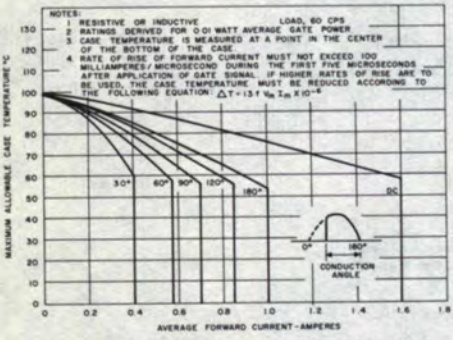
Repetitive Peak Forward Blocking Voltage (PFV)	300 Volts
RMS Forward Current	1.6 Amperes
Average Forward Current, On-state, $I_{F(AV)}$	Depends on conduction angle (see charts 2 and 3)
Peak One Cycle Forward Surge Current, (non-repetitive) I_{FM} (surge)	15 Amperes
Peak Gate Power, P_{GM}	0.1 Watt
Average Gate Power $P_{G(AV)}$	0.01 Watt
Peak Gate Current I_{GFM}	0.1 Ampere
Peak Gate Voltage, Forward & Reverse, V_{GFM} & V_{GRM}	6 Volts
Storage Temperature, T_{stg}	−65°C to +125°C
Operating Temperature, T_J	−65°C to +100°C

CHARACTERISTICS

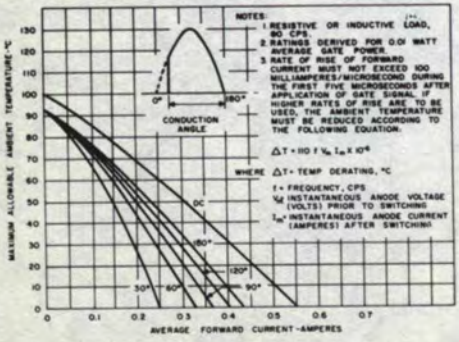
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Reverse Blocking Current	I_{RX}	....	40	100	μA	V_{RX} =Rated V_{ROM} (rep) T_J =100°C R_{GK} =40,000 ohms
Forward Blocking Current	I_{FX}	....	40	100	μA	V_{FX} =Rated V_{FOM}, T_J =100°C R_{GK} =40,000 ohms
Gate Current to Trigger	I_{GT}	....	5	20	μAdc	V_{FX} = +6 Vdc, T_J =25°C R_L =100 ohms Max.
Gate Supply Current to Trigger	I_{GS}	....	10	40	μAdc	V_{FR} = +6 Vdc, T_J =25°C R_L =100 ohms Max. R_{GK} =40,000 ohms
Holding Current	I_{HX}	....	0.2	1.0	ma	R_{GK} =40,000 ohms, T_J =25°C
Turn-on Time	t_d+t_r	....	1.4	....	μsec.	I_F =1 amp, T_J =25°C
Turn-off Time	t_o	....	20	....	μsec.	i_F =1 amp, i_R =1 amp dv/dt =20v/μsec. R_{GK} =100 ohms, T_J =100°C (See Application Notes)



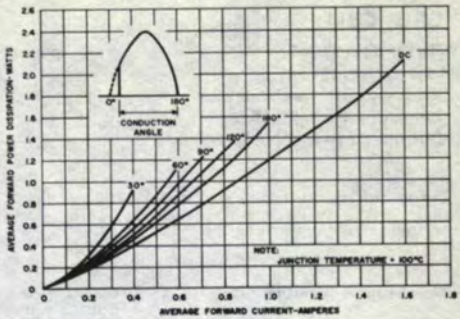
1. Maximum Forward Characteristic—On-State



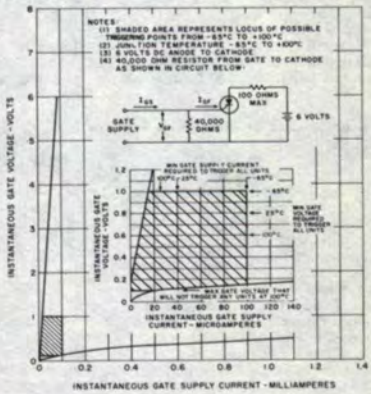
2. Maximum Allowable Case Temperature



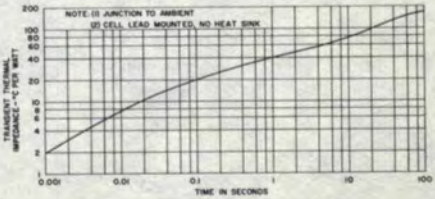
3. Maximum Allowable Ambient Temperature



4. Forward Power Dissipation



5. Gate Trigger Characteristics



6. Maximum Transient Thermal Impedance

C8U–C8D

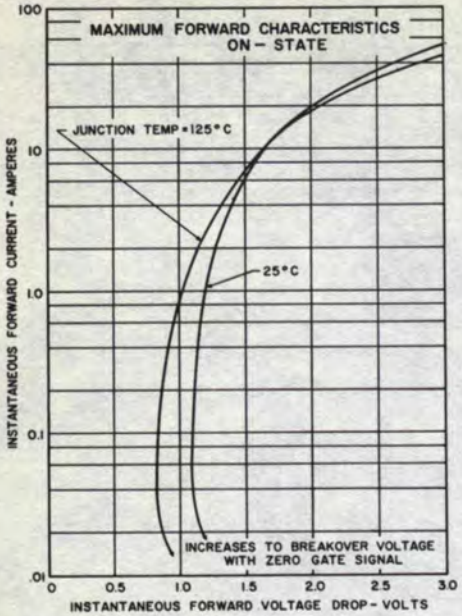
(TYPE 2N1929–2N1935)
Low Current
Silicon Controlled Rectifier
2.7 Amperes RMS Max.
Outline Drawing No. 2

The unique double-ended mechanical design of the 2N1929-1935 permits point-to-point wiring flexibility in circuit layout design. A prime feature of these devices is that high current loads are carried without the use of any external heat sink.

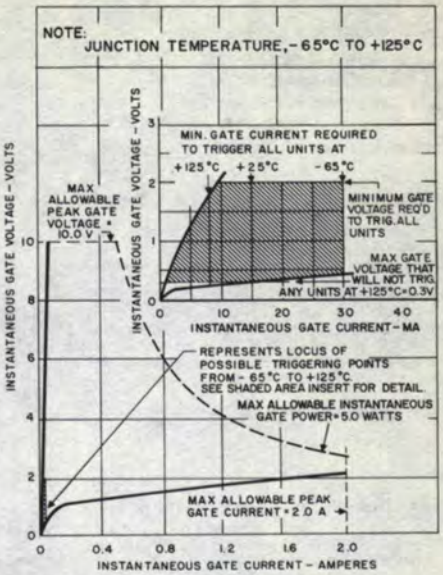
Maximum Allowable Ratings	(Resistive or Inductive Load, 50-400 cps) (C8U) 2N1929	(C8F) 2N1930	(C8A) 2N1931	(C8G) 2N1932	(C8B) 2N1933	(C8H) 2N1934	(C8C) 2N1935
Non-repetitive Peak Reverse, Voltage, V_{ROM} (non-rep)* (<5 millisec.)	35	75	150	225	300	350	400 volts
Repetitive Peak Reverse Voltage V_{ROM} (Rep)*	25	50	100	150	200	250	300 volts
Repetitive Peak Forward Blocking Voltage (PFV)	480 volts						
Average Forward Current $I_{F(AV)}$	Depends on Conduction Angle (See Charts 2 & 4)						
Peak One Cycle Non-recurrent Surge Current I_{FM} (surge)	30 amperes (See Chart 5)						
Peak Gate Power, P_{GM}	5 watts						
Average Gate Power $P_{G(AV)}$	0.1 watt						
Peak Gate Current I_{GFM}	2.0 amperes						
Peak Gate Voltage (Forward and Reverse) V_{GFM} & V_{GRM}	10 volts						
Operating Junction Temperature, T_J	−65°C to +125°C						
Storage Temperature, T_{stg}	−65°C to +150°C						

Characteristics at Maximum Ratings (125°C Junction Temperature)	2N1929	2N1930	2N1931	2N1932	2N1933	2N1934	2N1935
Minimum Forward Break-over Voltage $V_{(BR)FX}$	25	50	100	150	200	250	300 volts
Maximum Reverse $I_{RO(AV)}$ or Forward $I_{FO(AV)}$ Blocking Current	4.0	4.0	2.0	1.5	1.1	1.0	0.9 ma d-c
Maximum On-Voltage V_{FM}	1.1 volts (at 1.1 amps DC)						
Gate Triggering Characteristic (See Chart 3)							
Maximum Thermal Resistance θ_{J-A} (See Chart 6)	90°C/watt						
Maximum Holding Current (I_H)	20 ma at 25°C Junction Temp.						
Typical Holding Current (I_H)	8 ma at 25°C Junction Temp.						

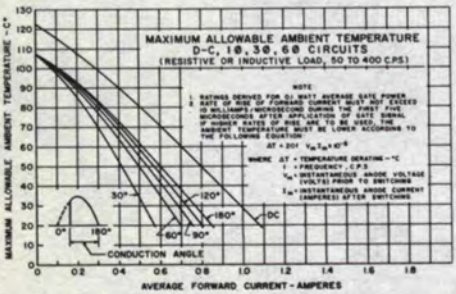
* V_{ROM} ratings apply for zero or negative gate voltage only.



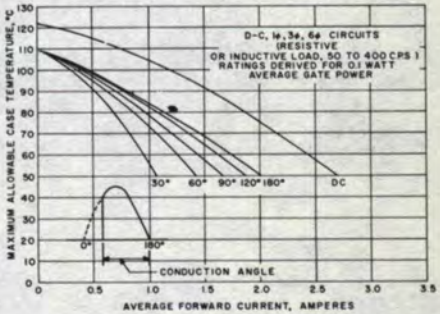
1. Maximum Forward Characteristics



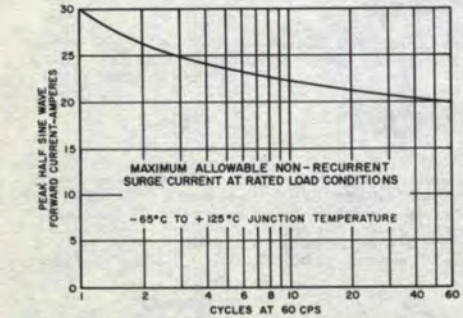
3. Gate Trigger Characteristics



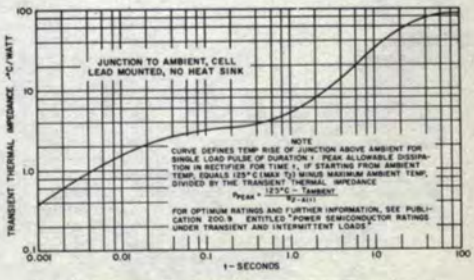
2. Maximum Forward Current vs. Ambient Temperature



4. Maximum Allowable Case Temperature



5. Maximum Allowable Non-Recurrent Surge Current at Rated Load Conditions



6. Maximum Transient Thermal Impedance

C9 Series

Fast Turn-off Type
Silicon Controlled Rectifier
12 μsec Turn-off Time
2.7 Amperes RMS Max.
Outline Drawing No. 2

Features:
- Specially Designed for Inverter, Pulse Modulator, Chopper Frequency Changer, Cycloconverter, and other High Frequency Applications
- Insured Turn-off Time† of Less than 12 μsec
- Same Top Features of General Electric's Proven Dependable C8 (Type 2N1929-1935).
- Broad Voltage Range—Up to 300 volts

† Turn-off time is defined as the time interval required for the silicon controlled rectifier to regain its forward blocking state after forward current conduction. This time is measured from the point where the forward current reaches zero to the time of reapplication of forward voltage. For additional information refer to Chapter 5. The C9 is specially selected from the C8 Series (Type 2N1929-1935). Ratings and characteristics (with the following additions) apply as described for the C8 Series (Type 2N1929-1935) specifications.

Maximum Allowable Ratings (Note 1)

	C9U	C9F	C9A	C9G	C9B	C9H	C9C
Repetitive Peak Reverse Voltage V_{ROM} (rep)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	5 amperes						
Junction Temperature Range, T_J	−65°C to +125°C						
Maximum Turn-Off Time	12 microseconds						
Test Conditions for Turn-Off (Note 2)							
Instantaneous Forward Current Immediately Before Turn-Off, i_F	1 ampere						
Peak Reverse Current, I_{RXM}	1 ampere						
Rate of Rise of Reverse Current	1.0 ampere per μsecond						
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond						
Junction Temperature, T_J	+125°C						
Typical Turn-Off vs Forward Current See Chart							
Ambient Temperature Derating Constant for Frequencies above 400 cycles (Note 3)	K = 20						

Note 1

The specified peak reverse voltage (PRV) and peak reverse current ratings must not be exceeded. The peak reverse current during turn-off must be high enough to allow recovery of the device. The reverse voltage level during recovery affects both turn-off time and the rate of rise capability of the reapplied forward voltage. The factory test condition of 2.0 volts maximum reverse voltage during this interval is a conservative value and assures satisfactory performance at the higher reverse voltages.

Note 2

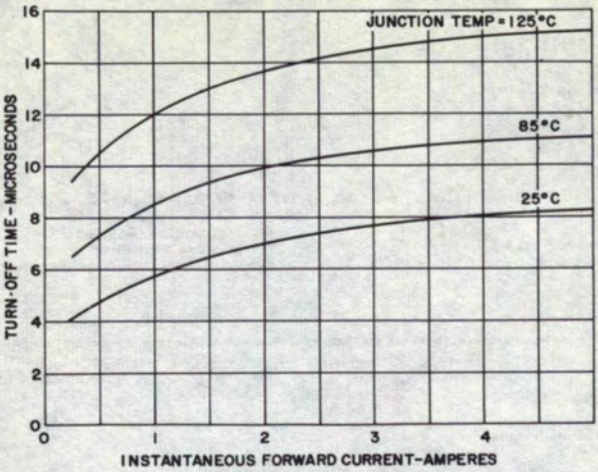
Many circuit variables have a pronounced effect on turn-off time. Decreasing the junction temperature from the test value of 125C to 25C reduces the turn-off time. Similarly, decreasing the magnitude of forward current just before turn-off reduces turn-off time. Note that the test conditions have been selected to give the maximum turn-off time of the SCR for nominal load conditions.

Note 3

At normal power frequencies in the range of 50 to 400 cps the switching losses are small and normally constitute a negligible portion of the total losses. At frequencies above 400 cps the switching losses during the turn-on interval can contribute significantly to the total losses if the circuit L/R time constant is short (10 microseconds or less) so that the build-up of current is essentially determined by the collapse of voltage across the controlled rectifier. When these conditions exist it becomes necessary to derate the average forward current vs. stud (ambient for C9) temperature relationship. The following equation gives the Stud Temperature derating in °C which must be subtracted from the value read on the inverter specification sheet for the particular average current and conduction angle:

$$\Delta T = K f V_{FX} i_F \times 10^{-6}$$

where K = constant for the particular inverter type SCR
ΔT = stud temperature derating in °C (ambient temperature for C9)
f = operating frequency in cps
V_{FX} = instantaneous anode voltage immediately prior to switching
i_F = instantaneous anode current immediately after switching



1. Typical Turn-Off Time vs Forward Current $I_F = 1$ Amp Peak

C10U–C10D

(TYPE 2N1770A–2N1777A)
Low Current
Silicon Controlled Rectifier
7 Amperes RMS Max.
Outline Drawing No. 3

The 150° maximum junction temperature of the C10 (2N1770A–1777A) will prove useful in applications calling for higher ambient temperatures or smaller heat sinks than the C11.

- Designed to meet MIL-S-19500/168
- New improved forward current rating
- Full $V_{(BR)FX}$ ratings from −65°C to +150°C
- No gate bias required
- High gate sensitivity
- Specified maximum holding current

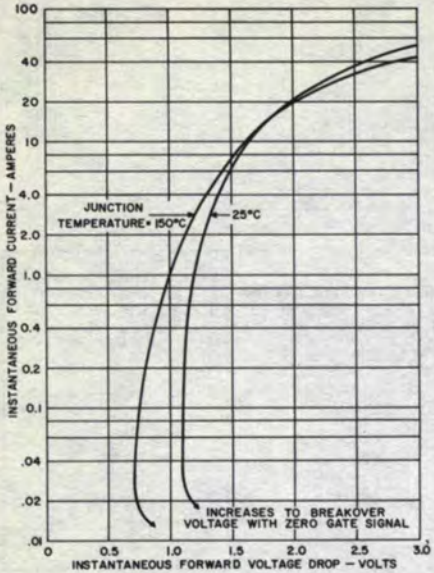
MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50–400 cps)

	(C10U) 2N1770A	(C10F) 2N1771A	(C10A) 2N1772A	(C10G) 2N1773A	(C10B) 2N1774A	(C10H) 2N1775A	(C10C) 2N1776A	(C10D) 2N1777A
Transient Peak Reverse Voltage, V_{ROM} (non rep) (<5 millisec)	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage, V_{ROM} (rep)	25	50	100	150	200	250	300	400 volts
Repetitive Peak Forward Blocking Voltage (PFV)	480 volts							
RMS Forward Current, I_f	7 amperes (For all conduction angles)							
Average Forward Current $I_{F(AV)}$	Depends on conduction angle (See Chart 3)							
Peak One Cycle Non-Recurrent Surge Current $I_{FM(surge)}$	60 amperes (See Chart 5)							
Peak Surge Current During Turn-On Time Interval	(See Chart 5)							
Peak Gate Power, P_{GM}	5 watts							
Average Gate Power, $P_{G(AV)}$	0.5 watts							
Peak Gate Current, I_{GFM}	2.0 amperes							
Peak Gate Voltage, forward and reverse, V_{GFM} & V_{GRM}	10 volts							
Storage Temperature, T_{STG}	−65°C to +150°C							
Operating Junction Temperature, T_J	−65°C to +150°C							
Stud Torque	15 inch-pounds							

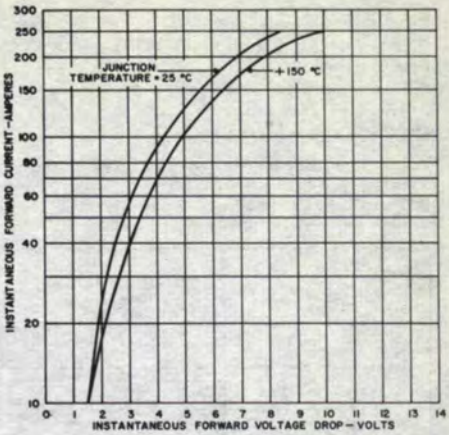
CHARACTERISTICS AT MAXIMUM RATINGS (+150°C Junction Temperature)

	(C10U) 2N1770A	(C10F) 2N1771A	(C10A) 2N1772A	(C10G) 2N1773A	(C10B) 2N1774A	(C10H) 2N1775A	(C10C) 2N1776A	(C10D) 2N1777A
Minimum Forward Break-over Voltage, $V_{(BR)FX}$	25	50	100	150	200	250	300	400 volts
Maximum Reverse $I_{RO(AV)}$ or Forward, $I_{FO(AV)}$ Current (Full Cycle Average)*	4.5	4.5	4.5	4.0	3.0	2.5	2.0	1.0 ma
Maximum on Voltage V_{FM}	0.75 volts (4.7 amp avg., 180° conduction angle)							
Maximum Gate Current to Trigger I_{GTM}	15 ma @ 25°C (See Chart 4)							
Maximum Gate Voltage to Trigger V_{GTM}	2.0 volts (See Chart 4)							
Minimum Gate Voltage to Trigger V_{GT}	0.2 volts (See Chart 4)							
Maximum Thermal Resistance θ_{J-C}	3.1°C/watt							
Maximum Holding Current, I_{HO}	25 ma @ 25°C Junction Temperature							
Typical Holding Current, I_{HO}	8 ma @ 25°C Junction Temperature							
Typical Gate Current to Trigger, I_{GT}	4.0 ma at +0.75 volts Gate to Cathode voltage							
Typical Turn-on Time ($t_d + t_r$)	2.0 microseconds							
Typical Turn-off Time, t_{off}	10.0 microseconds							

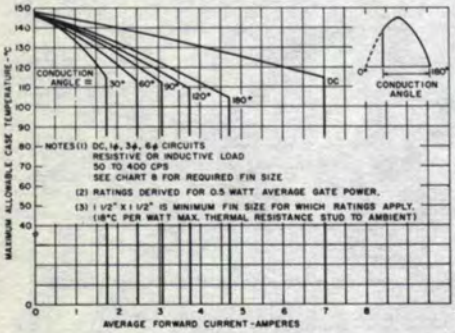
* Values apply for zero or negative gate voltage only.



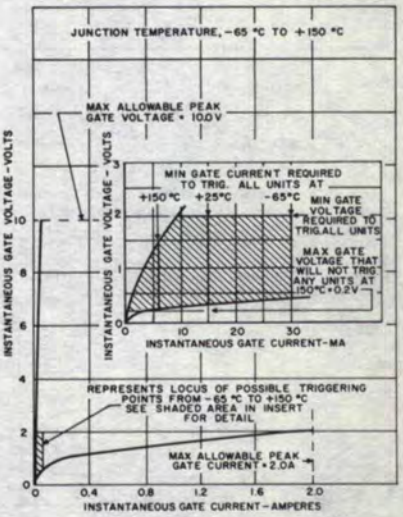
1. Maximum Forward Characteristics—On-State



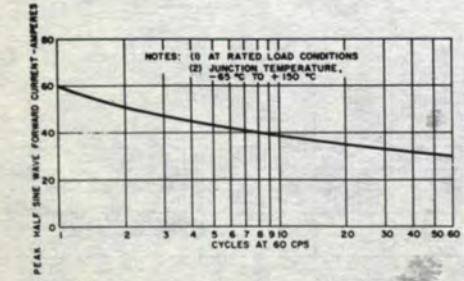
2. Maximum Forward Characteristics High Current Level—On-State



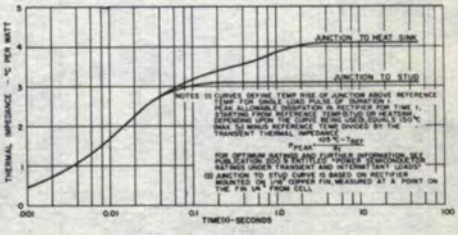
3. Maximum Allowable Stud Temperature For Sinusoidal Current Waveform



4. Triggering Characteristics



5. Maximum Allowable Non-Recurrent Surge Current Rating



6. Maximum Transient Thermal Resistance

C11

(TYPE 2N1770–2N1778, 2N2619)
Low Current
Silicon Controlled Rectifier
7 Amperes RMS Max.
Outline Drawing No. 3

The high current capability of the C11 series results from the copper anode stud construction, allowing direct mounting to a heat sink.

- Broad Voltage Range (Up to 600V)
- Long Electrical Creepage Path
- No Gate Bias Required
- High Gate Sensitivity

Type	Minimum Forward Breakover Voltage† $V_{(BR)FX}$ $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage† V_{ROM} (rep) $T_J = -65°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5 Millisec.)† V_{ROM} (non-rep) $T_J = -65°C$ to $+125°C$
C11U (2N1770)	25 Volts*	25 Volts*	40 Volts*
C11F (2N1771)	50 Volts*	50 Volts*	75 Volts*
C11A (2N1772)	100 Volts*	100 Volts*	150 Volts*
C11G (2N1773)	150 Volts*	150 Volts*	225 Volts*
C11B (2N1774)	200 Volts*	200 Volts*	300 Volts*
C11H (2N1775)	250 Volts*	250 Volts*	350 Volts*
C11C (2N1776)	300 Volts*	300 Volts*	400 Volts*
C11D (2N1777)	400 Volts*	400 Volts*	500 Volts*
C11E (2N1778)	500 Volts*	500 Volts*	600 Volts*
C11M (2N2619)	600 Volts*	600 Volts*	720 Volts*

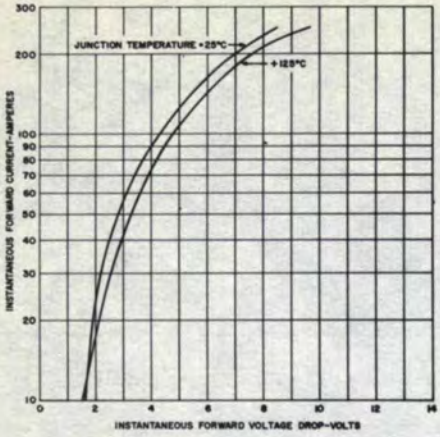
MAXIMUM ALLOWABLE RATINGS

Repetitive Peak Forward Blocking Voltage (PFV) . . . . . (C11U thru C11D) 480 Volt)
(C11E and C11M) 720 Volts
RMS Forward Current, I_f . . . . . (All conduction angles) 7.4 Amperes
Average Forward Current, $I_{F(AV)}$ . . . . . 4.7 Amperes* at 60°C Case (Half Wave Rectified)
For other operating conditions see Chart 2
Peak One Cycle Non-recurrent Surge Current, I_{FM} (surge) . . . . . 60 Amperes*
Peak Surge Current During Turn-on Time Interval . . . . . See Chart 4
Peak Gate Power, P_{GM} . . . . . 5 Watts*
Average Gate Power, $P_{G(AV)}$ . . . . . 0.5 Watt*
Peak Gate Current, I_{GFM} . . . . . 2.0 Amperes*
Peak Gate Voltage, (Forward and Reverse), V_{GFM} & V_{GRM} . . . . . 10 Volts*
Operating Junction Temperature, T_J . . . . . −65°C to +125°C*
Storage Temperature, T_{stg} . . . . . −65°C to +150°C*
Stud Torque . . . . . 15 inch-pounds

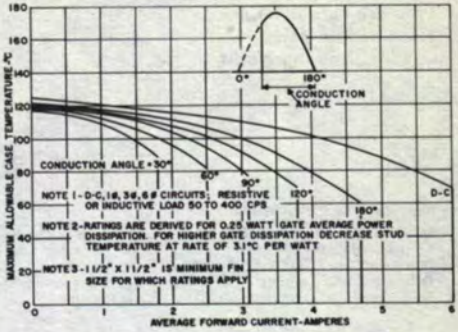
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Reverse and Forward Blocking Current†	I_{ROM} and I_{FOM}					T_J = 125°C, Gate Open
C11U (2N1770)		....	4.5	9.0	ma	$V_{ROM} = V_{FOM}$ = 25 Volts Peak
C11F (2N1771)		....	4.5	9.0	ma	50
C11A (2N1772)		....	4.5	9.0	ma	100
C11G (2N1773)		....	4.0	8.0	ma	150
C11B (2N1774)		....	3.0	6.0	ma	200
C11H (2N1775)		....	2.5	5.0	ma	250
C11C (2N1776)		....	1.5	4.0	ma	300
C11D (2N1777)		....	1.0	2.0	ma	400
C11E (2N1778)		....	1.0	2.0	ma	500
C11M (2N2619)		....	1.0	2.0	ma	600
Full Cycle Avg. Reverse and Forward Blocking Current†	$I_{RO(AV)}$ and $I_{FO(AV)}$					T_C = 60°C, $I_{F(AV)}$ = 4.7A, half sine wave 180° Conduction Angle
C11U (2N1770)		....	2.3	4.5*	mAdc	$V_{ROM} = V_{FOM}$ = 25 Volts Peak
C11F (2N1771)		....	2.3	4.5*	mAdc	50
C11A (2N1772)		....	2.3	4.5*	mAdc	100
C11G (2N1773)		....	2.0	4.0*	mAdc	150
C11B (2N1774)		....	1.5	3.0*	mAdc	200
C11H (2N1775)		....	1.3	2.5*	mAdc	250
C11C (2N1776)		....	0.8	2.0*	mAdc	300
C11D (2N1777)		....	0.5	1.0*	mAdc	400
C11E (2N1778)		....	0.5	1.0*	mAdc	500
C11M (2N2619)		....	0.5	1.0*	mAdc	600
Gate Current to Trigger	I_{GT}	....	10	15	mAdc	V_{FX} = 12Vdc, T_J = 25°C, R_L = 250 ohms
		....	20	30*	mAdc	V_{FX} = 12Vdc, T_J = −65°C, R_L = 250 ohms
		....	4	8	mAdc	V_{FX} = 12Vdc, T_J = 125°C, R_L = 250 ohms
Holding Current	I_{HO}	....	8.0	....	mAdc	Anode Supply = 6 Vdc, T_J = 25°C
Thermal Resistance	θ_{J-C}	....	1.5	3.1	°C/Watt	Junction to Case.

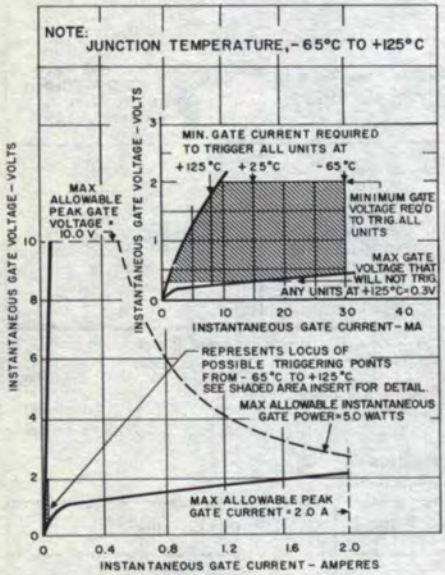
† Values apply for zero or negative gate voltage. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply = 18°C per watt.
* Indicates data included on JEDEC type number registration.



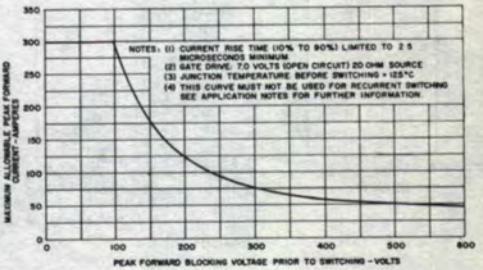
1. Maximum Forward Characteristics—On-State



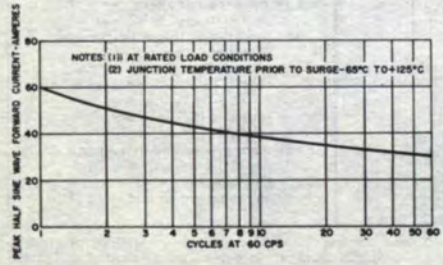
2. Maximum Allowable Case Temperature



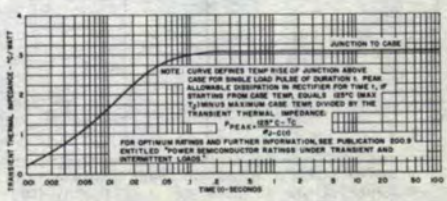
3. Trigger Characteristics



4. Peak Non-Recurrent Surge Current During Turn-On Time Interval



5. Maximum Allowable Non-Recurrent Surge Current Rating



6. Maximum Transient Thermal Impedance

C12

Fast Turn-off Type
Low Current
Silicon Controlled Rectifier
12 μ sec Turn-off Time
7.4 Amperes RMS
Outline Drawing No. 3

Features:

- Specially Designed for Inverter, Pulse Modulator, Chopper, Cycloconverter, and other High Frequency Applications.
- Insured Turn-Off Time† of Less Than 12 μsec.
- Same Top Features of General Electric's Proven, Dependable C11 Series (2N1770–78, 2N2619).
- Wide Voltage Range—Up to 400 volts.

† Turn-off time is defined as the time interval required for the silicon controlled rectifier to regain its forward blocking state after forward current conduction. This time is measured from the point where the forward current reaches zero to the time of reapplication of forward voltage. For additional information on fast turn-off cricuits, refer to Chapter 5.

Type	Minimum Forward Breakover Voltage $V_{(BR)FO}$* $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage $V_{ROM\ (rep)}$* $T_J = -65°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec.) $V_{ROM\ (non\text{-}rep)}$* $T_J = -65°C$ to $+125°C$
C12U	25 Volts	25 Volts	40 Volts
C12F	50 Volts	50 Volts	75 Volts
C12A	100 Volts	100 Volts	150 Volts
C12G	150 Volts	150 Volts	225 Volts
C12B	200 Volts	200 Volts	300 Volts
C12H	250 Volts	250 Volts	350 Volts
C12C	300 Volts	300 Volts	400 Volts
C12D	400 Volts	400 Volts	500 Volts

* Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance of which maximum V_{ROM} (rep) ratings apply equals 18° C/watt.

MAXIMUM ALLOWABLE RATINGS

All maximum allowable ratings for C11 SCR apply with the following addition:
Peak Reverse Recovery Current, I_R (recovery) . . . . . 15 amperes

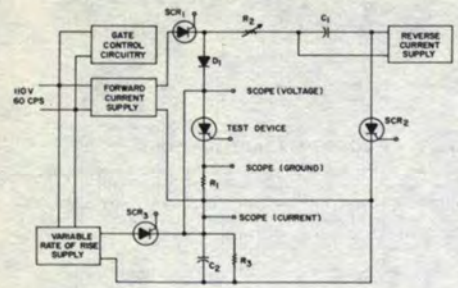
CHARACTERISTICS

All characteristics for C11 SCR's apply with the following addition:

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Circuit-Commutated Turn-off Time	t_{off}	....	8	12	μsec	(Refer to Chart 1.) Peak forward current, on-state (I_{FM}) = 5 A.† Peak reverse recovery current (I_R recovery) = 10 A. Peak reverse voltage (V_{RXM}) = rated voltage Reverse voltage (V_{RX}) = 10 V.‡ Switching (repetition rate) = 60 pps Rate of rise of re-applied forward blocking voltage (dv/dt) = 20 V/μsec Peak forward blocking voltage (V_{FXM}) = rated voltage Duty Cycle (percent on-time) = .5% Junction temperature = +125°C

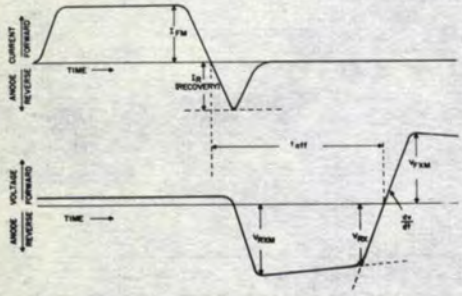
† When an SCR is switched into a high anode current, localized junction heating occurs. For reliable operation the rate of rise of the anode current should be minimized. For further information, consult Application Note 200.28 entitled "The Rating of SCR's When Switching Into High Currents."
‡ Increasing the magnitude of reverse voltage immediately prior to the reapplication of forward blocking voltage decreases circuit-commutated turn-off time.

SIMPLIFIED CIRCUIT-COMMUTATED TURN-OFF TIME TEST CIRCUIT

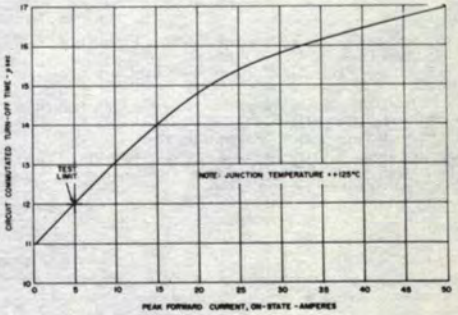


R_1 = Non-Inductive Current Viewing Resistor
R_2 = Reverse Current Adjusting Resistor
D_1 = Rectifier Diode selected for Reverse Recovery Time longer than Reverse Recovery time of test device, but shorter than Turn-off Time of test device.
SCR Triggering Sequence
At t = o, Test Device and SCR_1
At t = 50 μsec, SCR_2
At t $\geq$ 50 μsec, SCR_3

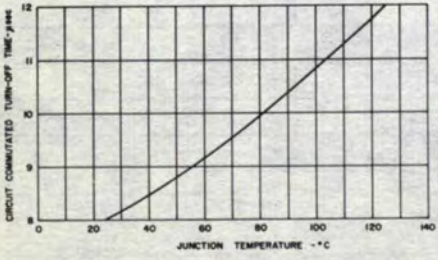
This circuit may be used to determine the circuit-commutated turn-off time of the test SCR. It operates in the following manner:
A specified (see Test Conditions, page 1) forward conduction current is passed through the device for a short period of time. The anode circuit is then driven negative, causing reverse current to flow. After sufficient stored charge has recombined or has been swept out of the base regions, the anode to cathode potential will begin to go negative with a corresponding decrease in reverse current. Forward voltage is then applied to the anode of the device and the device has fully recovered when it regains its ability to block the re-applied forward voltage at a specified rate of voltage rise.
For further information, see Application Note 200.15 entitled, "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers."



1. Circuit-Commutated Turn-Off Time Waveforms



2. Maximum Circuit-Commutated Turn-Off Time vs. Peak Forward Current—On-State



3. Maximum Circuit-Commutated Turn-Off Time Vs. Junction Temperature

4. Maximum Allowable Case Temperature For Rectangular Current Waveform

C20, C22

Low Current
Silicon Controlled Rectifier
7.4 Amperes RMS Max.
Outline Drawing No. 4

FOR HIGH VOLUME, LIGHT INDUSTRIAL AND CONSUMER APPLICATIONS

The C22 is provided in the popular "Press Fit" cup housing to insure ease of installation in large volume applications. Low cost makes this device suitable for high volume consumer and Light Industrial applications.
The C20 is the same as the C22 except that it is mounted on a $\frac{3}{8}$" hex and ¼"-28 stud as an added convenience to those manufacturers with production facilities more adaptable to "nut and bolt" type assembly.
An ideal, inexpensive trigger device for this Controlled Rectifier is a silicon Unijunction transistor such as type 2N2646.

- Flexibility of Mounting (Available in cup construction to solder, glue, or press fit, and as a stud device)
- One-piece Terminals
- High Surge Current Capabilities
- Low Power Required for Triggering

Type	Minimum Forward Breakover Voltage $V_{(BR)FX}$* T_J = −25°C to +100°C	Repetitive Peak Reverse Voltage V_{ROM} (rep)* T_J = −25°C to +100°C	Non-repetitive Peak Reverse Voltage (<5 millisec.) V_{ROM} (non-rep)* T_J = −25°C to +100°C
C20U, C22U	25 Volts	25 Volts	35 Volts
C20F, C22F	50 Volts	50 Volts	75 Volts
C20A, C22A	100 Volts	100 Volts	150 Volts
C20B, C22B	200 Volts	200 Volts	300 Volts
C20C, C22C	300 Volts	300 Volts	400 Volts
C20D, C22D	400 Volts	400 Volts	500 Volts

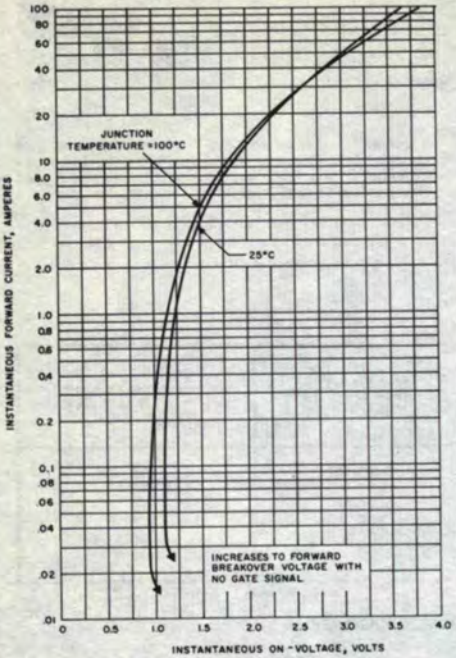
MAXIMUM ALLOWABLE RATINGS

Repetitive Peak Forward Blocking Voltage, PFV . . . . . 500 volts
RMS Forward Current, On-state, I_f . . . . . 7.4 Amperes (All conduction angles)
Average Forward Current, On-state, $I_{F(AV)}$ . . . . . 3.0 Amperes at 80°C case (Half wave rectified sine wave)
6.0 Amperes at 80°C case (Full wave rectified sine wave)
Peak One-cycle Surge Forward Current, I_{FM} (surge) . . . . . 80 amperes
I^2t (for fusing) . . . . . 27 Ampere² seconds (for times > 1.5 milliseconds)
Peak Gate Power Dissipation, P_{GM} . . . . . 5.0 watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 0.5 watts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5.0 volts
Storage Temperature, T_{stg} . . . . . −25°C to +100°C
Operating Junction Temperature, T_J . . . . . −25°C to +100°C
Stud Torque (C20 only) . . . . . 25 inch-pounds

CHARACTERISTICS

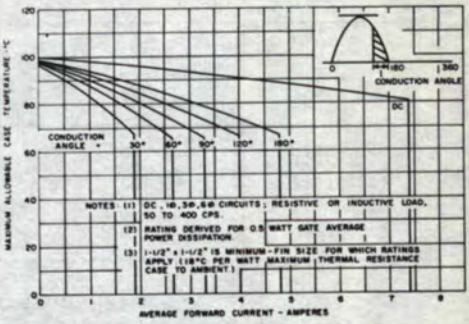
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Reverse and Forward Blocking Current*	I_{ROM} and I_{FOM}					T_J = 100°C
C20U, C22U		....	1.0	10.0	ma	V_{ROM} = V_{FOM} = 25 volts peak
C20F, C22F		....	1.0	10.0	ma	50 volts peak
C20A, C22A		....	1.0	7.0	ma	100 volts peak
C20B, C22B		....	1.0	3.5	ma	200 volts peak
C20C, C22C		....	1.0	2.3	ma	300 volts peak
C20D, C22D		....	1.0	1.7	ma	400 volts peak
Gate Trigger Current†	I_{GT}	....	4.0	25.0	mAdc	T_J = 25°C, V_{FX} = 6 Vdc, R_L = 60 ohms
		....	6.0	40.0	mAdc	T_J = −25°C, V_{FX} = 6 Vdc, R_L = 60 ohms
Gate Trigger Voltage	V_{GT}	....	0.8	1.5	Vdc	T_J = 25°C, V_{FX} = 6 Vdc, R_L = 60 ohms
		....	1.3	3.0	Vdc	T_J = −25°C, V_{FX} = 6 Vdc, R_L = 60 ohms
		0.2	0.5	....	Vdc	T_J = 100°C, V_{FXM} = rated, R_L = 100 ohms
Peak On Voltage	V_{FM}	....	1.50	1.85	V	T_J = 25°C, I_{FM} = 10 A peak, single half sine wave pulse, 2.0 millisec. wide
Holding Current	I_{HO}	....	10.0	30.0	mAdc	T_J = 25°C, anode supply = 24 Vdc

* Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 18° per watt.
† Special selections of Gate Trigger Current down to 4.0 mAdc are available upon request.

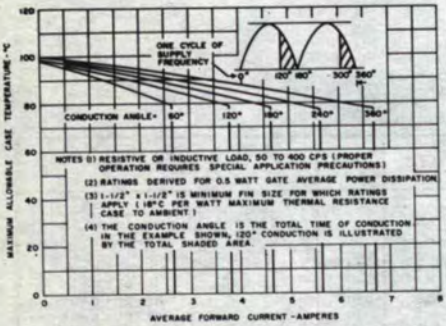


1. Maximum Forward Characteristics—On-State

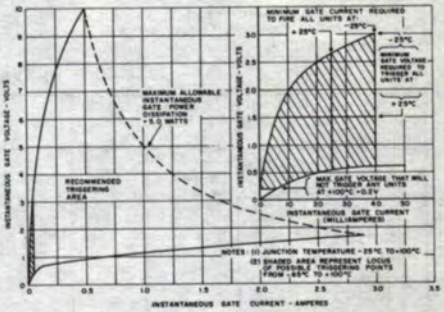
C22 Installation Instructions are the same as the C32 Installation Instructions on page 347.



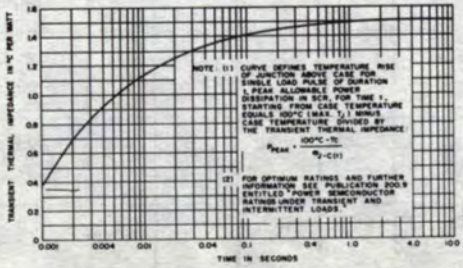
2. Maximum Allowable Case Temperature for Half Wave Rectified Sine Wave of Current



3. Maximum Allowable Case Temperature For Full Wave Rectified Sine Wave of Current



4. Gate Triggering Characteristics



5. Maximum Transient Thermal Impedance, Junction to Case

C30, C32

Light Industrial and Consumer
Medium Current SCR
25 Amperes RMS Max.
Outline Drawing No. 4

The C32 Silicon Controlled Rectifier is a three-junction semiconductor device for use in power switching and control applications requiring a blocking voltage of 400 volts or less and average load currents (full-wave rectified) up to 16 amperes. The C32 is provided in the popular "Press Fit" cup housing to insure ease of installation in large volume applications. Low cost makes this device suitable for high volume consumer and Light Industrial applications.
The C30 is the same as the C32 except that it is mounted on a $\frac{7}{16}$" hex and ¼"–28 stud as an added convenience to those manufacturers with production facilities more adaptable to "nut and bolt" type assembly.

- Flexibility of Mounting (Available in cup construction to solder, glue, or press fit, and as a stud device)
- One-piece Terminals
- High Surge Current Capabilities
- Low Power Required for Triggering

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$*	Repetitive Peak Reverse Voltage V_{ROM} (rep)*	Nonrepetitive Peak Reverse Voltage (<5.0 Millisec) V_{ROM} (non-rep)*
C30U, C32U	25 V	25 V	35 V
C30F, C32F	50 V	50 V	75 V
C30A, C32A	100 V	100 V	150 V
C30B, C32B	200 V	200 V	300 V
C30C, C32C	300 V	300 V	400 V
C30D, C32D	400 V	400 V	500 V

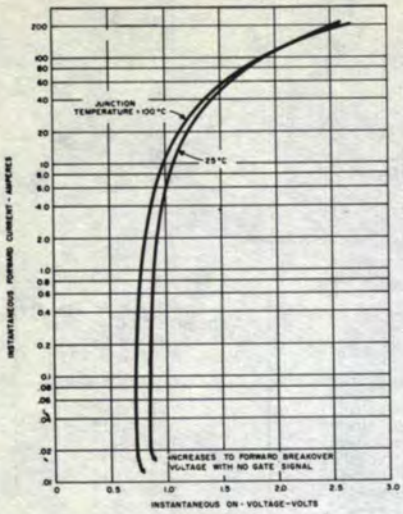
MAXIMUM ALLOWABLE RATINGS

Repetitive Peak Forward Blocking Volatge, PFV . . . . . 500 volts
RMS Forward Current, On-State . . . . . 25.0 amperes (all conduction angles)
Average Forward Current, On-State . . . . . 13 amperes at 75°C case (half wave rectified sine wave)
19 amperes at 75°C case (full wave rectified sine wave)
Peak One Cycle Surge Forward Current I_{FM} (surge) . . . . . 225 amperes
Peak Gate Power Dissipation, P_{GM} . . . . . 5.0 watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 0.5 watts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5.0 volts
Max. Storage Temperature, T_{stg} . . . . . 100°C
Max. Operating Junction Temperature . . . . . 100°C
Stud Torque (C30 Only) . . . . . 25 inch-pounds

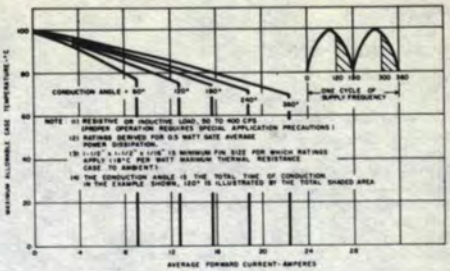
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Reverse and Forward Blocking Current*	I_{ROM} and I_{FOM}					T_J = 100°C
C30U, C32U		—	1.0	10.0	ma	$V_{ROM} = V_{FOM}$ = 25 volts peak
C30F, C32F		—	1.0	10.0	ma	= 50 volts peak
C30A, C32A		—	1.0	7.0	ma	= 100 volts peak
C30B, C32B		—	1.0	3.5	ma	= 200 volts peak
C30C, C32C		—	1.0	2.3	ma	= 300 volts peak
C30D, C32D		—	1.0	1.7	ma	= 400 volts peak
Gate Trigger Current	I_{GT}	—	4.0	25.0	mAdc	T_J = 25°C, V_{FX} = 6Vdc, R_L = 60 ohms
Gate Trigger Voltage	V_{GT}	— 0.2	0.8 0.5	1.5 —	Vdc Vdc	T_J = 25°C, V_{FX} = 6Vdc, R_L = 60 ohms T_J = 100 C, V_{FXM} = rated, R_L = 1000 ohms
Peak on Voltage	V_{FM}	—	1.30	1.5	V	T_J = 25°C, I_{FM} = 50 A peak, single half sine wave pulse, 2.0 milli-sec. wide
Holding Current	I_{HO}	—	10.0	50.0	mAdc	T_J = 25 C, anode supply = 24 Vdc

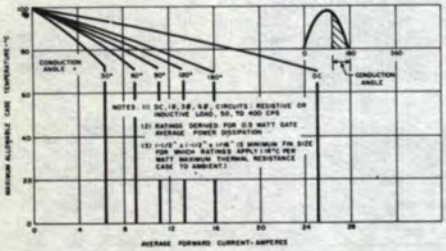
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 18°C per watt.



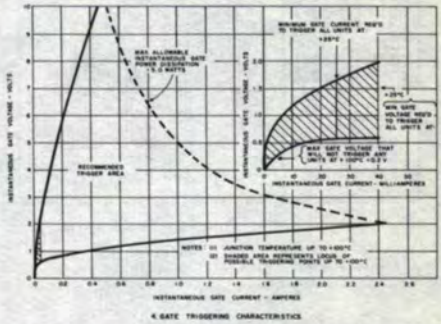
1 Maximum Forward Characteristics On-State



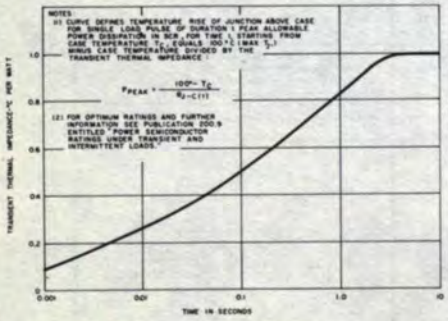
2 Maximum Allowable Case Temperature For Full Wave Rectified Sine Wave Of Current



3 Maximum Allowable Case Temperature For Half Wave Rectified Sine Wave Of Current



4 Gate Triggering Characteristics



5 Maximum Transient Thermal Impedance, Junction To Case

INSTALLATION OF C32

WHEN PRESS-FITTING THESE SCR'S INTO A HEATSINK, THE FOLLOWING SPECIFICATIONS AND RECOMMENDATIONS APPLY.

1. The heatsink materials may be copper, aluminum or steel. For maximum heat transfer and minimum corrosion problems, copper is recommended. The heatsink thickness, or amount of heatsink wall in contact with the SCR, should be ⅛ inch.
2. The hole diameter into which the SCR is pressed must be 0.4975 ± .001 inch. A slight chamfer on the hole should be used. This hole may be punched and reamed in a flat plate or extruded and sized in sheet metal.
3. The entire knurled section of the SCR should be in contact with the heatsink to insure maximum heat transfer. The SCR must not be inserted into a heatsink deeper than the knurl height.
4. The SCR insertion force must not exceed 800 pounds. If the insertion force approaches that value either the SCR is misaligned with the hole or the SCR-to-hole interference is excessive. The insertion force must be uniformly applied to the top face (terminal end) of the SCR within an annular ring which has an inside diameter not less than 0.370 inch and not larger than 0.390 inch; the outside diameter must not be less than 0.500 inch.
5. The thermal resistance between the SCR case and a copper heatsink will not exceed 0.5 C/W if the SCR is inserted in the manner described above.

C35

(TYPE 2N681–2N692)
Medium Current
Silicon Controlled Rectifier
35 Amperes RMS Max.
Outline Drawing No. 5

- Broad Voltage Range—Up to 800V (440 Volt RMS Applications)
- Thermal Fatigue Free
- No Peak Forward Voltage Limitation
- Standard TO-48 Outline
- Designed to Meet MIL-S-19500/108A
- Backed by 6 Years of Design and Field Experience

Type	Minimum Forward Breakover Voltage $V_{(BR)FX}$† $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep)† $T_J = -65°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec.) V_{ROM}(non-rep)† $T_J = -65°C$ to $+125°C$
C35U (2N681)	25 Volts*	25 Volts*	35 Volts*
C35F (2N682)	50 Volts*	50 Volts*	75 Volts*
C35A (2N683)	100 Volts*	100 Volts*	150 Volts*
C35G (2N684)	150 Volts*	150 Volts*	225 Volts*
C35B (2N685)	200 Volts*	200 Volts*	300 Volts*
C35H (2N686)	250 Volts*	250 Volts*	350 Volts*
C35C (2N687)	300 Volts*	300 Volts*	400 Volts*
C35D (2N688)	400 Volts*	400 Volts*	500 Volts*
C35E (2N689)	500 Volts*	500 Volts*	600 Volts*
C35M (2N690)	600 Volts*	600 Volts*	720 Volts*
C35S (2N691)	700 Volts*	700 Volts*	840 Volts*
C35N (2N692)	800 Volts*	800 Volts*	960 Volts*

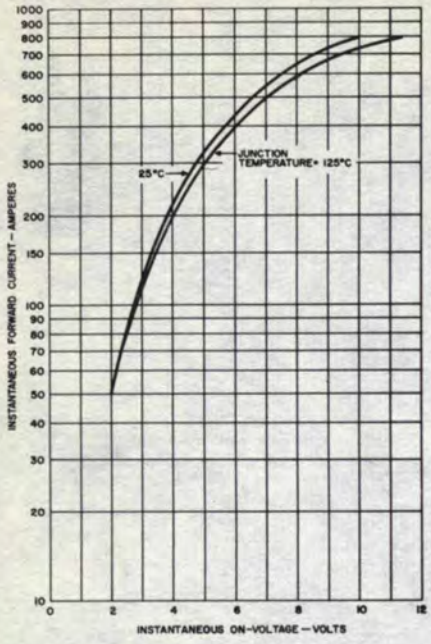
MAXIMUM ALLOWABLE RATINGS

RMS Forward Current, On-State, I_T . . . . . 35 amperes (all conduction angles)
Average Forward Current, On-State, $I_{F(AV)}$ . . . . . Depends on conduction angle (see Chart 2)
Peak One-cycle Surge Forward Current, I_{FM} (surge) . . . . . 150 amperes*
I^2t (for fusing) . . . . . 75 ampere² seconds (for times $\geq$ 1.5 milliseconds)
Peak Gate Power Dissipation, P_{GM} . . . . . 5 watts*
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 0.5 watt*
Peak Forward Gate Voltage, V_{GFM} . . . . . 10 volts*
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 volts*
Storage Temperature, T_{stg} . . . . . −65°C to +150°C*
Operating Junction Temperature, T_J . . . . . −65°C to +125°C*
Stud Torque . . . . . 30 inch-pounds
Peak Non-Recurrent Surge Forward Current During Turn-on Time Interval . . . . . See Chart 6

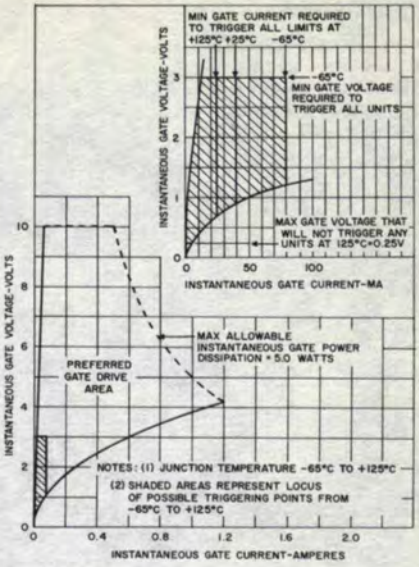
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Gate Trigger Current	I_{GT}	....	15	40	mAdc	T_J =25°C, V_{FX} =6 Vdc, R_L =50 ohms
		....	35	80*	mAdc	T_J = −65°C, V_{FX} =6 Vdc, R_L =50 ohms
		....	10	25	mAdc	T_J =125°C, V_{FX} =6 Vdc, R_L =50 ohms
Gate Trigger Voltage	V_{GT}	....	1.5	3.0*	Vdc	T_J = −65°C to 125°C, V_{FX} =6 Vdc, R_L =50 ohms
		0.25*	....	....	Vdc	T_J =125°C, V_{FXM} =Rated, R_L =1000 ohms
Holding Current	I_{HO}	....	10	100	mAdc	T_J =25°C, Anode supply =6 Vdc
Turn-on Time (Delay Time + Rise Time)	t_d+t_r	....	1.4	....	μsec.	T_J =25°C, I_F =5 Adc, V_{FXM} =rated, Gate supply: 10 volt open circuit, 25 ohm, 0.1 μsec. max. rise time.
Circuit-Commutated Turn-off Time	t_{off}	....	20	....	μsec.	T_J =125°C, I_{FM} =10A, I_R (recovery) =5A, V_{FXM} (reapplied) =Rated. Rate of rise of reapplied Forward Blocking Voltage =20 volts/μsec. linear.
Effective Thermal Resistance	θ_{J-C}	....	0.85	1.7	°C/watt	Junction to Case.
Exponential Rate of Rise of Forward Blocking Voltage	τ					T_J =125°C. Gate open circuited. V_{FOM} =Rated.
C35U (2N681)		2.6	....	....	μsec.	
C35F (2N682)		3.0	....	....		
C35A (2N683)		3.9	....	....		
C35G (2N684)		4.8	....	....		
C35B (2N685)		5.7	....	....		
C35H (2N686)		6.6	....	....		
C35C (2N687)		7.5	....	....		
C35D (2N688)		9.2	....	....		
C35E (2N689)		11.0	....	....		
C35M (2N690)		37.9	....	....		
C35S (2N691)		44.2	....	....		
C35N (2N692)		50.6	....	....		

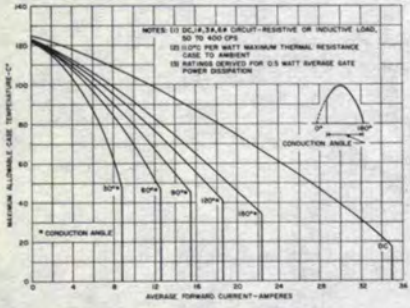
† Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 11°C/watt.
* Indicates data included on JEDEC type number registration.



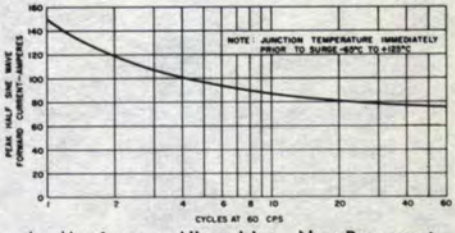
1. Maximum Forward Characteristics—High Current Level—On-State



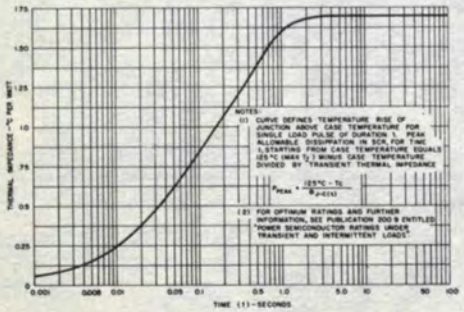
3. Gate Triggering Characteristics



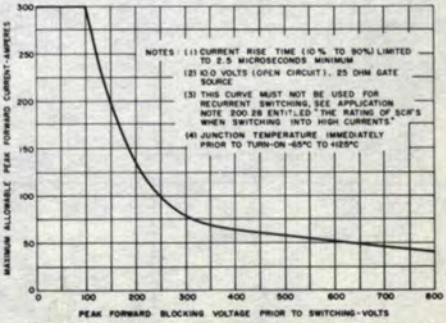
2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



4. Maximum Allowable Non-Recurrent Peak Surge Forward Current at Rated Load Conditions



5. Maximum Transient Thermal Impedance —Junction to Case



6. Peak Non-Recurrent Surge Forward Current During Turn-On Time Interval

C36U–C36N

(TYPE 2N1842–2N1850)
Medium Current Low Temperature
Silicon Controlled Rectifier
16 Amperes RMS Max.
Outline Drawing No. 5

MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50 to 400 CPS)

	C36U 2N1842	C36F 2N1843	C36A 2N1844	C36G 2N1845	C36B 2N1846	C36H 2N1847	C36C 2N1848	C36D 2N1849	C36E 2N1850
Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) (<5 millisec.)*	35	75	150	225	300	350	400	500	600 volts
Repetitive Peak Reverse Voltage, V_{ROM} (rep)*	25	50	100	150	200	250	300	400	500 volts
Repetitive Peak Forward Blocking Voltage (PFV)	600 volts up to C36E, 800 volts for C36M–N								
RMS Forward Current, I_F	16 amperes (For all conduction angles)								
Average Forward Current, $I_{F(AV)}$	Depends on conduction angle (See Chart 2)								
Peak One Cycle Surge Current, $I_{FM(surge)}$	125 amperes (See Chart 4)								
Peak Current During Turn-on Time Interval	(See Note)								
I^2t (for fusing)	40 amperes² seconds (time $\leq$.008 seconds)								
Peak Gate Power, P_{GM}	5 watts								
Average Gate Power, $P_{G(AV)}$	0.5 watt								
Peak Gate Current, I_{GFM}	2 amperes								
Peak Gate Voltage, V_{GFM} (forward)	10 volts								
Peak Gate Voltage, V_{GRM} (reverse)	5 volts								
Storage Temperature, T_{stg}	−40°C to +125°C								
Operating Junction Temperature, T_J	−40°C to +100°C								
Stud Torque	30 inch-pounds								

CHARACTERISTICS AT MAXIMUM RATINGS (100° Junction Temperature)

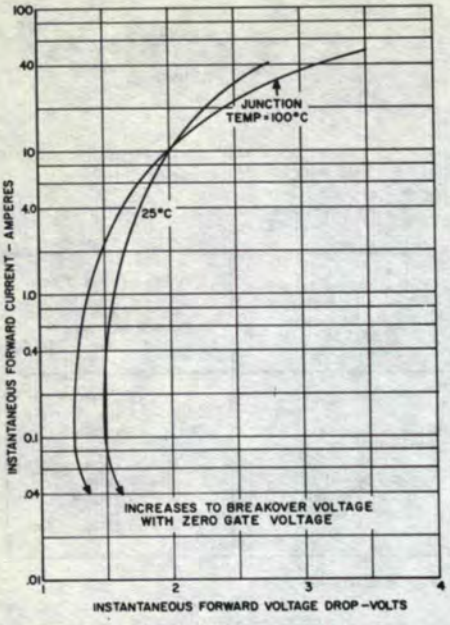
	C36U 2N1842	C36F 2N1843	C36A 2N1844	C36G 2N1845	C36B 2N1846	C36H 2N1847	C36C 2N1848	C36D 2N1849	C36E 2N1850
Minimum Forward Breakover Voltage, $V_{(BR)FX}$	25	50	100	150	200	250	300	400	500 volts
Minimum Time Constant for Application of Forward Blocking Voltage (Also See Chart 6)	2.6	3.0	3.9	4.8	5.7	6.6	7.5	9.2	11.0 microsec.
Maximum Reverse, $I_{ROM(AV)}$ or Forward, $I_{FOM(AV)}$ Blocking Current*	22.5	19.0	12.5	6.5	6.0	5.5	5.0	4.0	3.0 ma
Maximum on Voltage, ($V_{F(AV)}$)	1.25 volts (Full Cycle Average)								
Gate Triggering Characteristic	(See Chart 3)								
Maximum Thermal Resistance, θ_{J-C}	2.5°C/watt (Junction to Stud)								
Typical Holding Current, I_{HO}	20 ma								

* V_{ROM} (rep) ratings apply for zero or negative gate voltage. For positive gate voltage applied simultaneously with V_{ROM} (rep), see Application Notes. Maximum heat sink thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 11.0°C per watt.

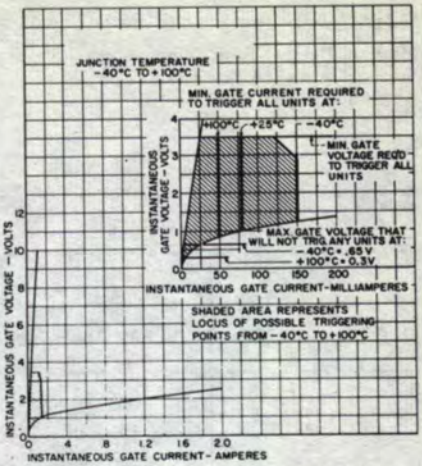
C36M	C36S	C36N
600	700	800

NOTE: Peak recurrent current during turn-on interval must be limited to values below.

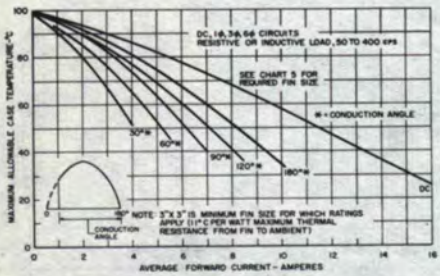
Max Voltages to be Switched	Max Allowable Recurrent Peak Current (Rise Time 5.0 Microseconds)
100V	300A
200V	140A
300V	75A
400V	65A
500V	60A



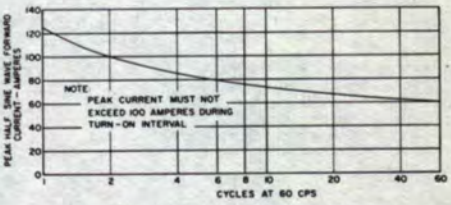
1. Maximum Forward Characteristics—On-State



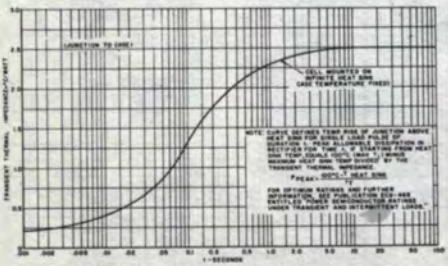
3. Gate Triggering Characteristics



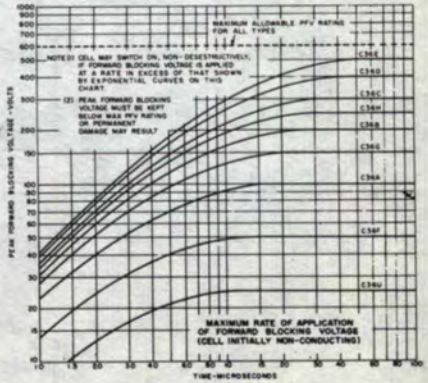
2. Maximum Allowable Case Temperature for Sinusoidal Current Waveform



4. Maximum Allowable Surge Current at Rated Load Conditions



5. Maximum Transient Thermal Impedance



6. Maximum Rate of Application of Forward Blocking Voltage

C38

Medium Current High Temperature Silicon Controlled Rectifier
35 Amperes RMS Max.
Outline Drawing No. 5

The C38 with a higher Junction Temperature Rating than the C35 (2N681-92) series, will prove useful in applications calling for higher ambient temperatures or smaller heat sinks than the C35 series permits.

- No Peak Forward Voltage Limitation
- Thermal Fatigue Free
- High Junction Temperature (150°C)
- Standard TO-48 Outline
- Long Creepage Path
- Low Thermal Resistance

Type	Minimum Forward Breakover* Voltage $V_{(BR)FX}$ $T_J = -65°C$ to $+150°C$	Repetitive Peak Reverse* Voltage V_{ROM} (rep) $T_J = -65°C$ to $+150°C$	Non-Repetitive Peak Reverse* Voltage V_{ROM} (non-rep) (<5.0 Millisec.)* $T_J = -65°C$ to $+150°C$
C38U	25 volts	25 volts	35 volts
C38F	50 volts	50 volts	75 volts
C38A	100 volts	100 volts	150 volts
C38G	150 volts	150 volts	225 volts
C38B	200 volts	200 volts	300 volts
C38H	250 volts	250 volts	350 volts
C38C	300 volts	300 volts	400 volts
C38D	400 volts	400 volts	500 volts
C38E	500 volts	500 volts	600 volts

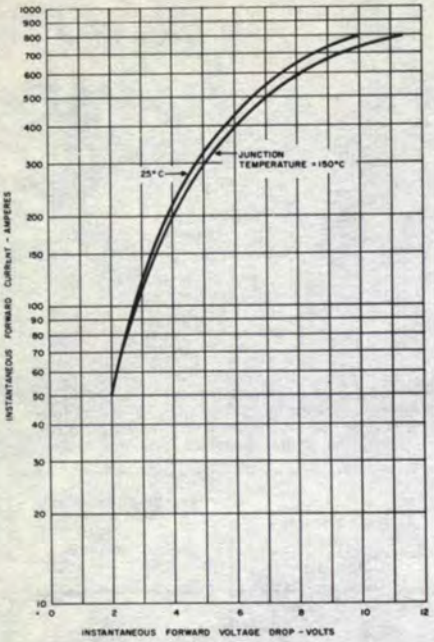
MAXIMUM ALLOWABLE RATINGS

RMS Forward Current, I_T . . . . . 35 amperes (all conduction angles)
Average Forward Current, $I_{F(AV)}$ . . . . . Depends on conduction angle (see Chart 2)
Peak One-cycle Non-recurrent Surge Current, I_{FM} (surge) . . . . . 150 amperes
Peak Non-recurrent Surge Current during Turn-on time Interval . . . . . See Chart 5
I^2t (for fusing) . . . . . 75 ampere² seconds (for times $\geq$ 1.5 milliseconds)
Peak Gate Power, P_{GM} . . . . . 12 watts
Average Gate Power, $P_{G(AV)}$ . . . . . 0.5 watt
Peak Gate Current, I_{GFM} . . . . . 2.0 amperes
Peak Gate Voltage (Forward and Reverse), V_{GFM} and V_{GRM} . . . . . 10 volts
Storage Temperature, T_{stg} . . . . . −65°C to +150°C
Operating Junction Temperature, T_J . . . . . −65°C to +150°C
Stud Torque . . . . . 30 inch-pounds

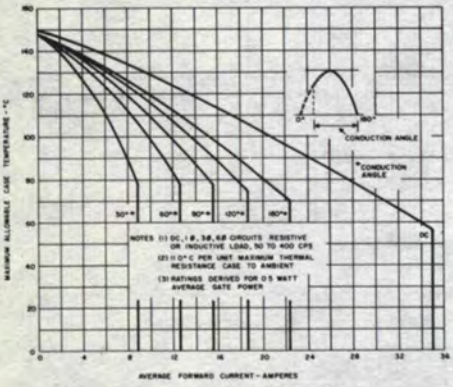
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Reverse and Forward Blocking Current*	I_{ROM} and I_{FOM}					$T_J = 150°C$
C38U		....	9.0	13.0	ma	$V_{ROM} = V_{FOM} =$ 25v peak
C38F		....	8.9	13.0	ma	50
C38A		....	7.8	13.0	ma	100
C38G		....	7.7	13.0	ma	150
C38B		....	7.5	12.0	ma	200
C38H		....	7.3	11.0	ma	250
C38C		....	6.8	10.0	ma	300
C38D		....	5.3	8.0	ma	400
C38E		....	2.6	6.0	ma	500
Rate of Rise of Forward Voltage that Will Not Turn on SCR**	dv/dt	20.0	40.0	....	volts/ μsec	$T_J = 150°C$ Gate open circuited. V_{AC} = Rated.
Gate Current to Trigger	I_{GT}	....	15	40	mAdc	$T_J = 25°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
		....	35	80	mAdc	$T_J = -65°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
		....	7.5	20	mAdc	$T_J = 150°C$, $V_{FX} = 6$ Vdc $R_L = 50$ ohms
Gate Voltage to Trigger	V_{GT}	....	1.2	3.0	Vdc	$V_{FX} = 6$ Vdc, $T_J = 25°C$, $R_L = 50$ ohms
		....	2.0	3.0	Vdc	$V_{FX} = 6$ Vdc, $T_J = -65°C$, $R_L = 50$ ohms
		0.15	....	....	Vdc	V_{FXM} = Rated, $T_J = 150°C$, $R_L = 1000$ ohms
On Voltage	V_F	....	1.7	2.0	v	$i_F = 50a$ peak, $T_J = 25°C$
Holding Current	I_{HO}	....	10	80	mAdc	$T_J = 25°C$, Anode Supply = 6 Vdc
Turn-on Time	$t_d + t_r$	....	1.4	....	μsec	$T_J = 25°C$, $i_F = 5.0$ Adc, V_{FXM} = Rated. Gate supply: 10 volt open circuit, 25 ohm, 0.1 μsec. max. rise time.
Turn-off Time	t_{off}	....	24	....	μsec	$T_J = 150°C$, $i_F = 10a$, $i_R = 5a$, V_{FXM} (reapplied) = Rated, $dv/dt = 20v/\mu sec$ Linear
Thermal Resistance	θ_{J-C}	....	.75	1.5	°C/watt	Junction to case

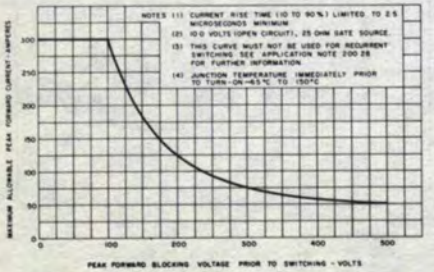
* Values apply for zero or negative gate voltage. Max. case to ambient thermal resistance for which max. V_{ROM} (rep) ratings apply = 11°C per watt.
** See Chart 4.



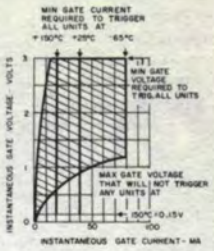
1. Maximum Forward Characteristics—High Current Level—On-State

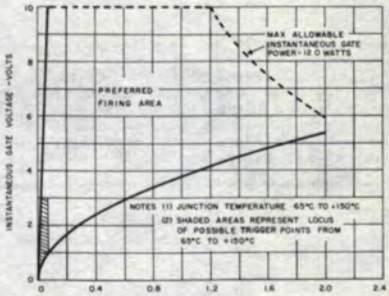


2. Maximum Allowable Case Temperature for Sinusoidal Current Waveform

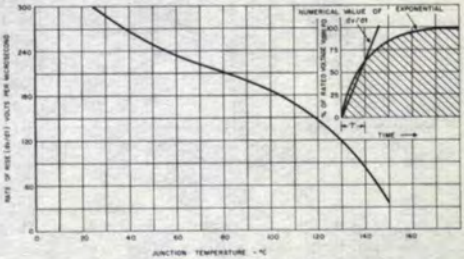


5. Peak Non-Recurrent Surge Current During Turn-On Time Interval

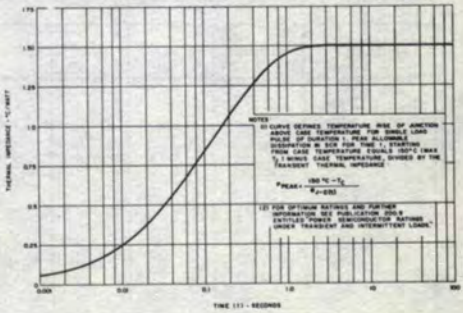




3. Triggering Characteristics



4. Typical Rate of Rise (dv/dt) Of Forward Voltage That Will Not Turn on SCR



6. Maximum Transient Thermal Impedance Junction to Case

NOTE: For Maximum Allowable Non-Recurrent Surge Current at Rated Load Conditions—See Curve on C35 Specifications.

C40

Fast Turn-off Type
Medium Current
Silicon Controlled Rectifier
35 Amps RMS Max.
12 μsec Turn-off Time
Outline Drawing No. 5

FEATURES:
- Specially designed for inverter, pulse modulator, chopper, cycloconverter, and other high frequency applications.
- Insured turn-off time† of less than 12 μsec.
- Same top features of General Electric's famous C35 line.
- Wide Voltage Range—Up to 500V.

† Turn-off time is defined as the time interval required for the silicon controlled rectifier to regain its forward blocking state after forward current conduction. This time is measured from the point where the forward current reaches zero to the time of reapplication of forward voltage. For additional information refer to Chapter 5.

Type	Minimum Forward Breakover Voltage $V_{(BR)FX}$* $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep)* $T_J = -65°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec.) V_{ROM} (non-rep)* $T_J = -65°C$ to $+125°C$
C40U	25 Volts	25 Volts	35 Volts
C40F	50 Volts	50 Volts	75 Volts
C40A	100 Volts	100 Volts	150 Volts
C40G	150 Volts	150 Volts	225 Volts
C40B	200 Volts	200 Volts	300 Volts
C40H	250 Volts	250 Volts	350 Volts
C40C	300 Volts	300 Volts	400 Volts
C40D	400 Volts	400 Volts	500 Volts
C40E	500 Volts	500 Volts	600 Volts

* Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 11°C/watt.

MAXIMUM ALLOWABLE RATINGS

All maximum allowable ratings for C35 SCR apply with the following addition:
Peak Reverse Recovery Current (I_R (recovery)) ..... 20 amperes

CHARACTERISTICS

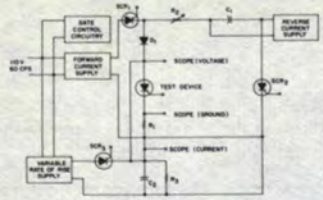
All characteristics for C35 SCR's apply with the following addition:

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Circuit-commutated Turn-off Time	t_{off}	....	8	12	μsec	(Refer to Chart 1.) Peak forward current, on-state (I_{FM}) = 10 A.† Peak reverse recovery current (I_R recovery) = 10 A. Peak reverse voltage (V_{RXM}) = rated voltage Reverse voltage (V_{RX}) = 10 V.‡ Switching (repetition rate) = 60 pps Rate of rise of re-applied forward blocking voltage (dv/dt) = 20 V/μsec Peak forward blocking voltage (V_{FXM}) = rated voltage Duty Cycle (percent on-time) = .5% Junction temperature = +125°C

† When an SCR is switched into a high anode current, localized junction heating occurs. For reliable operation, the rate of rise of the anode current should be minimized. For further information, consult Application Note 200.28 entitled "The Rating of SCR's When Switching Into High Currents."

‡ Increasing the magnitude of reverse voltage immediately prior to the reapplication of forward blocking voltage decreases circuit-commutated turn-off time.

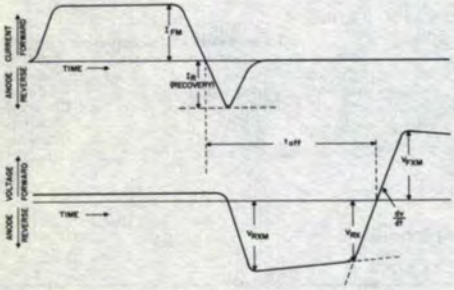
SIMPLIFIED
CIRCUIT-COMMUTATED TURN-OFF TIME TEST CIRCUIT



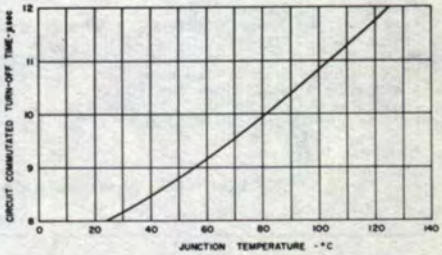
R_1 = Non-inductive Current Viewing Resistor
R_2 = Reverse Current Adjusting Resistor
D_1 = Rectifier Diode selected for Reverse Recovery Time longer than Reverse Recovery time of test device, but shorter than Turn-off Time of test device.

SCR Triggering Sequence
At $t = 0$, Test Device and SCR_1
At $t = 50$ μsec, SCR_2
At $t \geq 50$ μsec, SCR_3

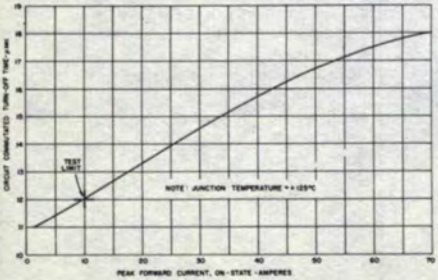
This circuit may be used to determine the circuit-commutated turn-off time of the test SCR. It operates in the following manner:
A specified (see Test Conditions, page 1) forward conduction current is passed through the device for a short period of time. The anode circuit is then driven negative, causing reverse current to flow. After sufficient stored charge has recombined or has been swept out of the base regions, the anode to cathode potential will begin to go negative with a corresponding decrease in reverse current. Forward voltage is then applied to the anode of the device and the device has fully recovered when it regains its ability to block the re-applied forward voltage at a specified rate of voltage rise.
For further information, see Application Note 200.15 entitled, "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers."



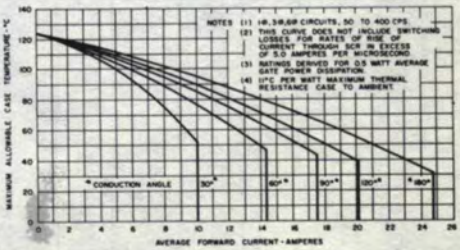
1. Circuit-Commutated Turn-Off Time Waveforms



2. Maximum Circuit-Commutated Turn-Off Time vs. Peak Forward Current—On-State



3. Maximum Circuit-Commutated Turn-Off Time Vs. Junction Temperature



4. Maximum Allowable Case Temperature For Rectangular Current Waveform

C45—Flag Terminal Cathode
C46—Braided Cathode Lead

High Current
Silicon Controlled Rectifier
55 Amperes RMS Max.
Outline Drawing No. 6 for C45
Outline Drawing No. 7 for C46

An outstanding feature of the C45 and C46 (formerly ZJ246) is their hard solder construction affording a high degree of freedom from thermal fatigue.

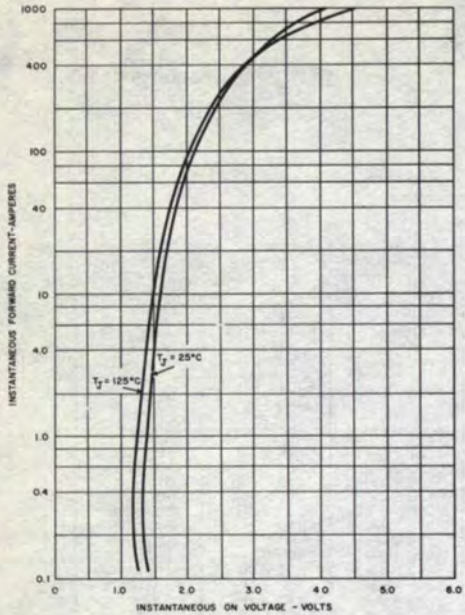
Type	Minimum Forward Breakover Voltage $V_{BR\ FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-repetitive Peak Reverse Volt. (<5.0 Millisec) V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$
C45/C46U	25 Volts	25 Volts	35 Volts
C45/C46F	50 Volts	50 Volts	75 Volts
C45/C46A	100 Volts	100 Volts	150 Volts
C45/C46G	150 Volts	150 Volts	225 Volts
C45/C46B	200 Volts	200 Volts	300 Volts
C45/C46H	250 Volts	250 Volts	350 Volts
C45/C46C	300 Volts	300 Volts	400 Volts
C45/C46D	400 Volts	400 Volts	500 Volts
C45/C46E	500 Volts	500 Volts	650 Volts
C45/C46M	600 Volts	600 Volts	720 Volts
C45/C46S	700 Volts	700 Volts	840 Volts
C45/C46N	800 Volts	800 Volts	960 Volts
C45/C46T	900 Volts	900 Volts	1040 Volts

MAXIMUM ALLOWABLE RATINGS

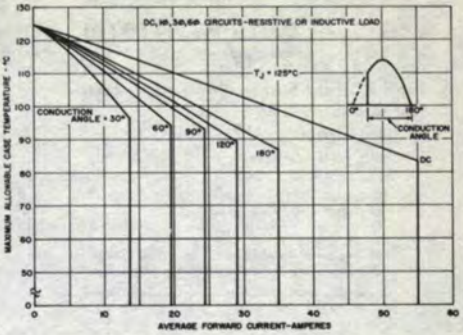
RMS Forward Current, On-State . . . . . 55 amperes (all conduction angles)
Average Forward Current, On-State . . . . . Depends on conduction angle (see Chart 2)
Peak One-cycle Surge Forward Current, I_{FM} (surge) . . . . . 700 amperes
I^2t (for fusing) $T_J = -40°C$ to $+125°C$ . . . . . 2000 ampere^2 seconds (for times $\geq$ 1.5 milliseconds)
di/dt . . . . . Depends on voltage, (see Chart 6)
Peak Gate Power Dissipation, P_{GM} . . . . . 5 watts
Average Gate Power Dissipation, $P_{G\ (AV)}$ . . . . . 0.5 watt
Peak Forward Gate Voltage, V_{GFM} . . . . . 10 volts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 volts
Storage Temperature, T_{stg} . . . . . $-40°C$ to $+150°C$
Operating Temperature . . . . . $-40°C$ to $+125°C$
Stud Torque . . . . . 150 inch-pounds
Peak Forward Voltage (PFV) (Self-protecting in forward direction) . . . . . ∞ (infinite)

CHARACTERISTICS

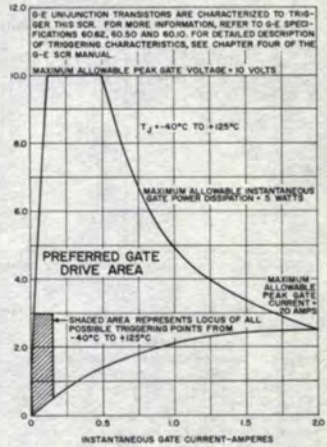
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Gate Trigger Current	I_{GT}	....	30	75	mAdc	$T_J = +25°C$, $V_{FX} = 6$Vdc, $R_L = 50$ ohms
		....	50	125	mAdc	$T_J = -65°C$, $V_{FX} = 6$Vdc, $R_L = 50$ ohms
		....	20	40	mAdc	$T_J = +125°C$, $V_{FX} = 6$Vdc, $R_L = 50$ ohms
Holding Current	I_{HO}	....	18	100	mAdc	$T_J = +25°C$, Anode supply = 22 Vdc
Exponential Rate of Rise of Forward Blocking Voltage	dv/dt	....		....	V/μsec	$T_J = +125°C$ Gate open circuited. V_{ROM} = Rated
C45, C46U			30			$dv/dt = \left(\frac{V_{FOM}}{\tau}\right)(.632)$
C45, C46F			30			
C45, C46A			30			
C45, C46G			30			
C45, C46B			30			
C45, C46H			30			
C45, C46C			20			
C45, C46D			20			
C45, C46E			20			
C45, C46M			20			
C45, C46S			15			
C45, C46N			15			
C45, C46T			15			



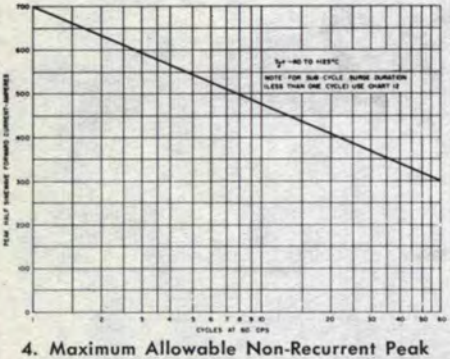
1. Maximum Forward Characteristics—On-State, High Current Level



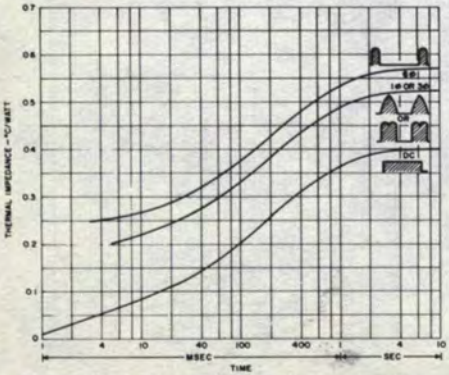
2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



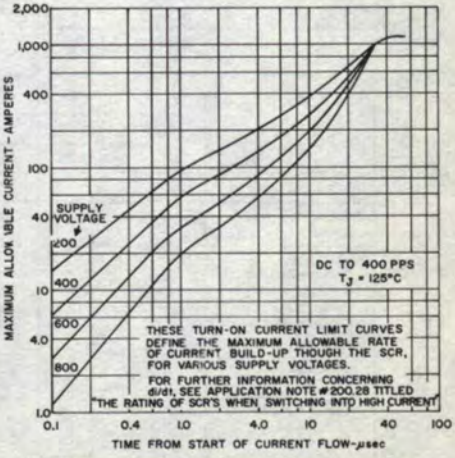
3. Gate Triggering Characteristics



4. Maximum Allowable Non-Recurrent Peak Surge Forward Current At Rated Load Conditions



5. Transient Thermal Impedance—Junction To Case



6. Current Limit For Steep Waveform Operation

C50 (Type 2N1909-2N1916)
C52 (Type 2N1792-2N1798)

High Current Silicon Controlled Rectifier
110 Amperes RMS Max.
Outline Drawing No. 7 for C50
Outline Drawing No. 6 for C52

The C52 high current SCR is the flag type (cathode and gate terminals) version of the C50 (2N1910) series.

- Broad Voltage Range—Up to 900V (440 Volt RMS Applications)
- Thermal Fatigue Free
- No Peak Forward Voltage Limitation Above 500 Volt Rating
- Standard TO-19 Outline
- Designed to Meet MIL-S-19500/243A
- Backed by 5 Years of Design and Field Experience

Type				Minimum Forward Breakover Voltage $V_{(BR)\,FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage (<5.0 millisec.) V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$	Peak Forward Voltage (PFV)*
C50U	(2N1909)	C52U	.....	25 Volts	25 Volts	35 Volts	500 Volts
C50F	(2N1910)	C52F	(2N1792)	50 Volts	50 Volts	75 Volts	500 Volts
C50A	(2N1911)	C52A	(2N1793)	100 Volts	100 Volts	150 Volts	500 Volts
C50G	(2N1912)	C52G	(2N1794)	150 Volts	150 Volts	225 Volts	500 Volts
C50B	(2N1913)	C52B	(2N1795)	200 Volts	200 Volts	300 Volts	500 Volts
C50H	(2N1914)	C52H	(2N1796)	250 Volts	250 Volts	350 Volts	500 Volts
C50C	(2N1915)	C52C	(2N1797)	300 Volts	300 Volts	400 Volts	500 Volts
C50D	(2N1916)	C52D	(2N1798)	400 Volts	400 Volts	500 Volts	500 Volts
C50E		C52E		500 Volts	500 Volts	650 Volts	No Limitation
C50M		C52M		600 Volts	600 Volts	720 Volts	No Limitation
C50S		C52S		700 Volts	700 Volts	840 Volts	No Limitation
C50N		C52N		800 Volts	800 Volts	960 Volts	No Limitation
C50T		C52T		900 Volts	900 Volts	1040 Volts	No Limitation

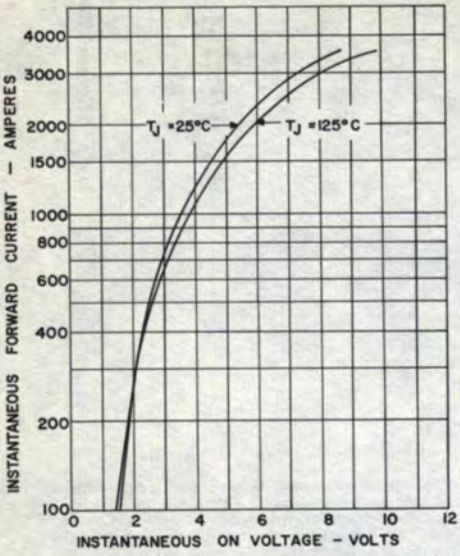
* Device may be safely switched into forward conducting state by anode voltage.

MAXIMUM ALLOWABLE RATINGS

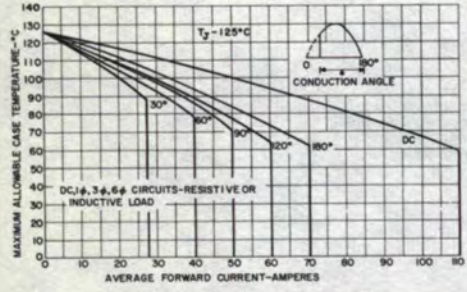
di/dt ..... Depends on voltage (see chart 6)
RMS Forward Current, On-State, I_F ..... 110 amperes (all conduction angles)
Average Forward Current, On-state, $I_{F(AV)}$ ..... Depends on conduction angle (see charts)
Peak One-cycle Surge Forward Current, I_{FM} (surge) ..... 1000 amperes
I^2t (for fusing) $T_J = -40°C$ to $-20°C$ ..... 2000 ampere² seconds (for times ≥1.5 milliseconds)
I^2t (for fusing) $T_J = -20°C$ to $+125°C$ ..... 4000 ampere² seconds (for times ≥1.5 milliseconds)
Peak Gate Power Dissipation, P_{GM} ..... 5 watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 0.5 watts
Peak Forward Gate Voltage, V_{GFM} ..... 10 volts
Peak Reverse Gate Voltage, V_{GRM} ..... 5 volts
Storage Temperature, T_{stg} ..... −40°C to +150°C
Operating Junction Temperature, T_J ..... −40°C to +125°C
Stud Torque ..... 150 inch-pounds

CHARACTERISTICS

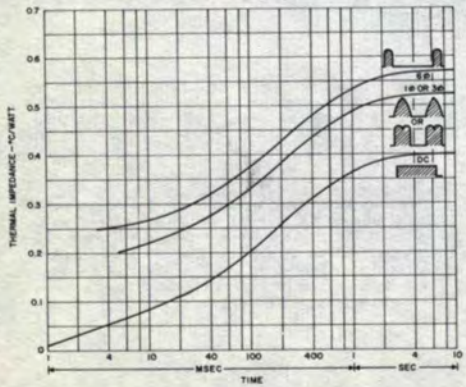
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Gate Trigger Current	I_{GT}	....	30	75	mAdc	$T_J = +25°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
		....	50	125	mAdc	$T_J = -40°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
		....	20	40	mAdc	$T_J = +125°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
Holding Current	I_{HO}	....	18	100	mAdc	$T_J = +25°C$, Anode supply = 22 Vdc
Effective Thermal Resistance	$\theta_{J\text{-}C}$	....	.3	.4	°C/watt	Junction to Case (Dc)
Exponential Rate of Rise of Forward Blocking Voltage	dv/dt				V/μsec	$T_J = +125°C$. Gate open circuited. V_{FOM} = Rated. $dv/dt = \left(\frac{V_{FOM}}{\tau}\right)(.632)$
C50, C52U		....	30	....		
C50, C52F		....	30	....		
C50, C52A		....	30	....		
C50, C52G		....	30	....		
C50, C52B		....	30	....		
C50, S52H		....	30	....		
C50, C52C		....	20	....		
C50, C52D		....	20	....		
C50, C52E		....	20	....		
C50, C52M		....	20	....		
C50, C52S		....	15	....		
C50, C52N		....	15	....		
C50, C52T		....	15	....		



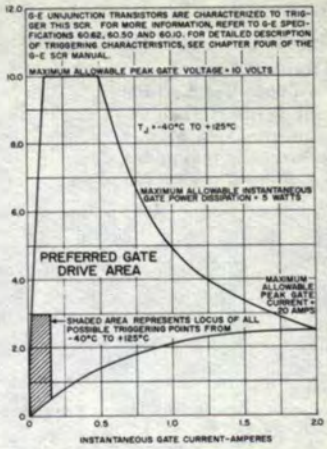
1. Maximum Forward Characteristics—On-State, High Current Level



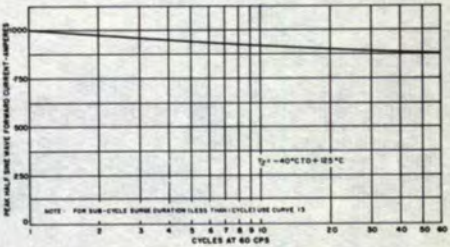
2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



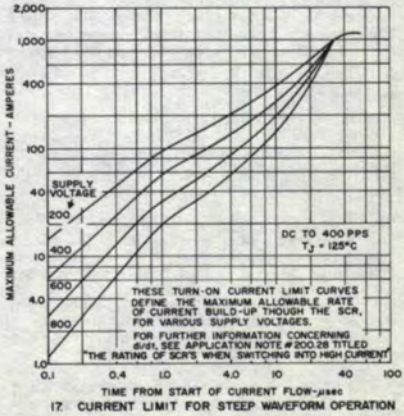
5. Transient Thermal Impedance—Junction To Case



3. Gate Triggering Characteristics



4. Maximum Allowable Non-Recurrent Peak Surge Forward Current At Rated Load Conditions



17. CURRENT LIMIT FOR STEEP WAVEFORM OPERATION

6. Current Limit For Steep Waveform Operation

C55—Braided Cathode Lead
C56—Flag Terminal Cathode

Fast Turn-off Type
Silicon Controlled Rectifier
20 μsec Turn-off Time
110 Amperes RMS Max.
C-55 Outline Drawing No. 7
C-56 Outline Drawing No. 6

FEATURES:
- Specially Designed for Inverter, Pulse Modulator, Chopper Frequency Changer, Cycloconverter, and other High Frequency Applications
- Insured Turn-off Time† of Less than 12 μsec
- Same Top Features of General Electric's Proven Dependable C50 Series (Type 2N1906-1916)
- Voltage Range—Up to 300 volts

† Turn-off time is defined as the time interval required for the silicon controlled rectifier to regain its forward blocking state after forward current conduction. This time is measured from the point where the forward current reaches zero to the time of reapplication of forward voltage. For additional information, refer to Chapter 5. The C55 is specially selected from the C50 Series (2N1906-1916). Ratings and characteristics (with the following additions) apply as described for type C50 (2N1906-1916) specifications.

Maximum Allowable Ratings (Note 1)

	C55U	C55F	C55A	C55G	C55B	C55H	C55C
Repetitive Peak Reverse Voltage (PRV)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	30 amperes						
Junction Temperature Range	−65°C to +125°C						
Maximum Turn-Off Time	20 microseconds						
Test Conditions for Turn-Off (Note 2)							
Instantaneous Forward Current Immediately Before Turn-Off	50 amperes						
Peak Reverse Current	10 amperes						
Rate of Rise of Reverse Current	5 amperes per μsecond						
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond						
Junction Temperature	+125°C						

Typical Turn-Off vs Forward Current See Chart
Stud Temperature Derating Constant
for Frequencies above 400 cycles (Note 3) K = 0.3

Note 1

The specified peak reverse voltage (PRV) and peak reverse current ratings must not be exceeded. The peak reverse current during turn-off must be high enough to allow recovery of the device. The reverse voltage level during recovery affects both turn-off time and the rate of rise capability of the reapplied forward voltage. The factory test condition of 2.0 volts maximum reverse voltage during this interval is a conservative value and assures satisfactory performance at the higher reverse voltages.

Note 2

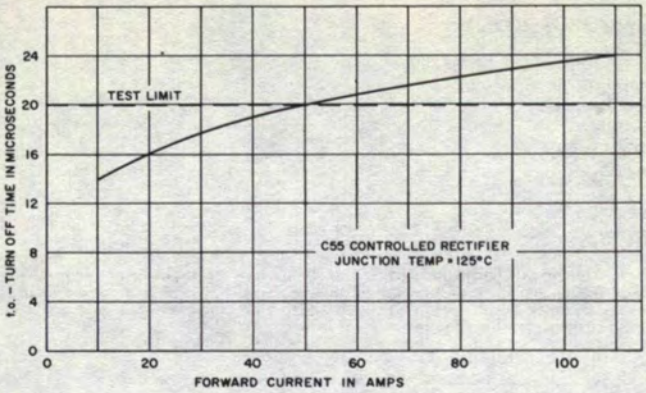
Many circuit variables have a pronounced effect on turn-off time. Decreasing the junction temperature from the test value of 125C to 25C reduces the turn-off time. Similarly, decreasing the magnitude of forward current just before turn-off reduces turn-off time. Note that the test conditions have been selected to give the maximum turn-off time of the SCR for nominal load conditions.

Note 3

At normal power frequencies in the range of 50 to 400 cps the switching losses are small and normally constitute a negligible portion of the total losses. At frequencies above 400 cps the switching losses during the turn-on interval can contribute significantly to the total losses if the circuit L/R time constant is short (10 microseconds or less) so that the build-up of current is essentially determined by the collapse of voltage across the controlled rectifier. When these conditions exist it becomes necessary to derate the average forward current vs. stud (ambient for C9) temperature relationship. The following equation gives the Stud Temperature derating in °C which must be subtracted from the value read on the inverter specification sheet for the particular average current and conduction angle:

$$\Delta T = K f V_m I_m \times 10^{-6}$$

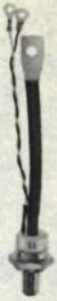
where K = constant for the particular inverter type SCR
ΔT = stud temperature derating in °C (ambient temperature for C9)
f = operating frequency in cps
V_m = instantaneous anode voltage immediately prior to switching
I_m = instantaneous anode current immediately after switching



1. Typical Turn-Off Time vs. Forward Current $I_r = 10$ Amps Peak

C60 (Type 2N2023–2029)
C61

High Current
Silicon Controlled Rectifier
110 Amperes RMS Max.
(High Temperature Type)
Outline Drawing No. 7



General Electric's C60 (2N2023-2029) and C61 Silicon Controlled Rectifiers are designed for high current operation at extreme temperatures. Rated as high as 110 amperes DC—with a maximum junction temperature of 150°C—they are especially suited for applications where high ambients or small heat sinks preclude the use of other controlled rectifiers at a required current level.
The C60 has a guaranteed low temperature limit of −65°C; the C61 series is guaranteed to −40°C. In all other respects they are identical, both offering these features:

- Hard Soldered Joints
- Welded Seals
- Silicon Rubber Insulated Lead
- Available with flag type terminal upon request
- Freedom from Thermal Fatigue

MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50 to 400 cps)

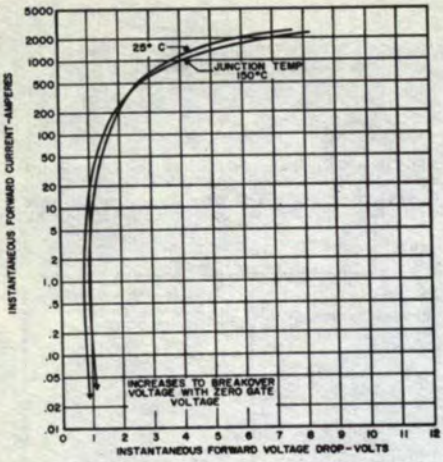
	C61U C60U (2N2023)	C61F C60F (2N2024)	C61A C60A (2N2025)	C61G C60G (2N2026)	C61B C60B (2N2027)	C61H C60H (2N2028)	C61C C60C (2N2029)	C61D C60D (2N2030)
Non-Repetitive Peak Reverse Voltage, V_{RSM} (non-rep) (<5 millisecond)*	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage, V_{ROM} (rep)*	25	50	100	150	200	250	300	400 volts
Repetitive Peak Forward Blocking Voltage (PFV)	400	400	400	400	400	400	400	500 volts
RMS Forward Current, I_T	110 amperes (For all conduction angles)							
Average Forward Current, $I_{F(AV)}$	Depends on conduction angle (See Chart 2)							
Peak One Cycle Surge Current, I_{FM} (surge)	1000 amperes (See Chart 4)							
I^2t (for fusing)	Up to 4000 ampere^2 seconds (See Chart 5)							
Peak Gate Power, P_{GM}	5 watts							
Average Gate Power, $P_{G(AV)}$	0.5 watt							
Peak Gate Current, I_{GFM}	2 amperes							
Peak Gate Voltage (Forward) V_{GFM}	10 volts							
Peak Gate Voltage (Reverse) V_{GRM}	5 volts							
Storage and Operating Junction Temperature, T_{stg} and T_J	−65°C to +150°C for C60 (−40°C to 150°C for C61)							
Stud Torque	150 inch-pounds							

CHARACTERISTICS AT MAXIMUM RATINGS (150°C Junction Temperature)

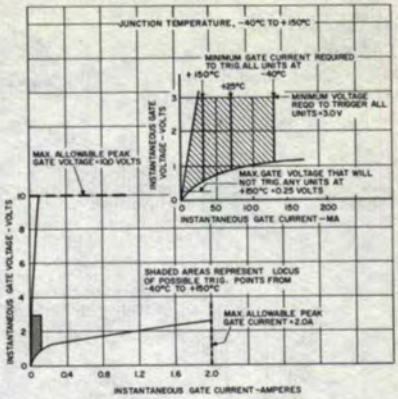
	C61U C60U (2N2023)	C61F C60F (2N2024)	C61A C60A (2N2025)	C61G C60G (2N2026)	C61B C60B (2N2027)	C61H C60H (2N2028)	C61C C60C (2N2029)	C61D C60D (2N2030)
Minimum Forward Breakover Voltage, $V_{(BR)FX}$	25	50	100	150	200	250	300	400 volts
Maximum Reverse $I_{ROM(AV)}$ or Forward $I_{FOM(AV)}$ Blocking Current*	6.5	6.5	6.5	6.5	6.0	5.5	5.0	4.5 ma
Maximum On Voltage, $V_{FM(AV)}$	0.8 volts (70 amp avg., 180° conduction angle)							
Gate Triggering Characteristics	(See Chart 3)							
Maximum Thermal Resistance, θ_{J-C}	4°C/watt (Junction to Case)							
Typical Holding Current, I_{HO}	20 ma							

*V_{ROM} (rep) ratings apply for zero or negative gate voltage. Minimum heatsink thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 3.5°C/watt.

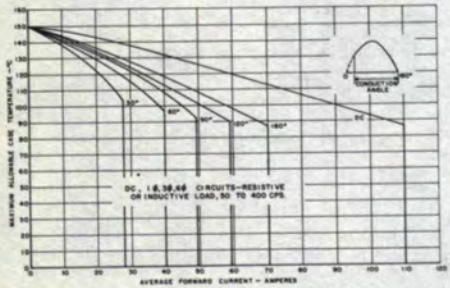
NOTE: Peak current during turn-on interval must be limited to the following values:
Switching from 200 volts or below −400 amperes
Switching from 201 volts or higher −300 amperes



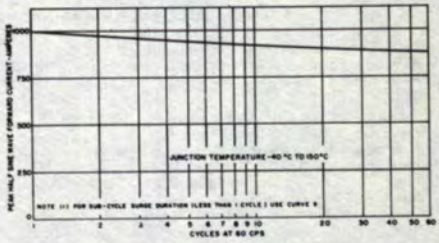
1. Maximum Forward Characteristics—Conducting State



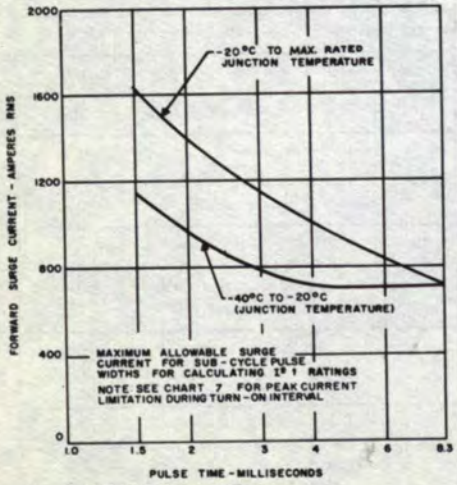
3. Triggering Characteristics



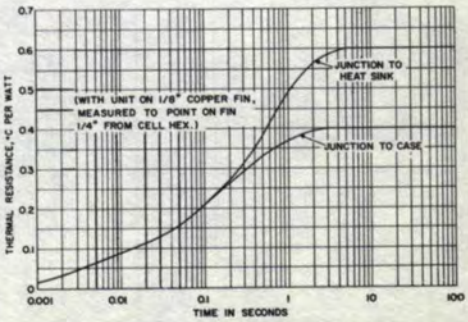
2. Maximum Allowable Case Temperature for Sinusoidal Current Waveform



4. Maximum Allowable Surge Current at Rated Load Conditions



5. Sub-Cycle Surge Rating



6. Maximum Transient Thermal Impedance

C150 (ZJ260)

High Current High Voltage Type
Silicon Controlled Rectifier
110 Amperes RMS max.
Outline Drawing No. 7

The C150 is a new generation SCR developed by the General Electric Company—optimized for high voltage applications. It incorporates all-diffused, all hard solder construction. It is rated at 110 amperes RMS, has V_{ROM} (rep) and $V_{(BR)FX}$ ratings to 1000 volts, and a minimum guaranteed dv/dt (rate of rise of forward voltage) of 200 volts per microsecond. Its static and dynamic rating suit it for use on 240 and 480 volt AC systems.

The C150 conforms to EIA registered outline TO-49.

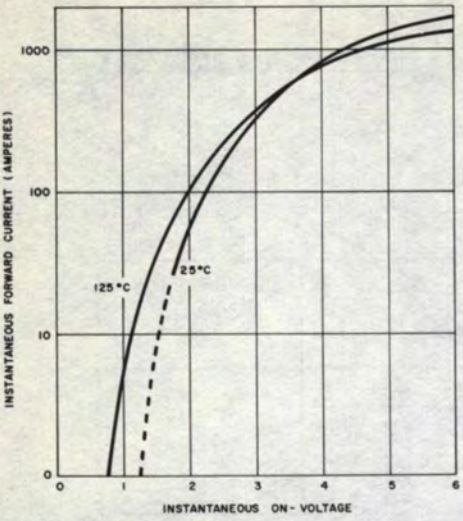
Type	Minimum Forward Breakover Voltage $V_{(BR)FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec) V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$
C150B	200 volts	200 volts	300 volts
C150C	300 volts	300 volts	400 volts
C150D	400 volts	400 volts	500 volts
C150E	500 volts	500 volts	600 volts
C150M	600 volts	600 volts	700 volts
C150S	700 volts	700 volts	850 volts
C150N	800 volts	800 volts	950 volts
C150T	900 volts	900 volts	1075 volts
C150P	1000 volts	1000 volts	1200 volts
C150PA	1100 volts	1100 volts	1325 volts

MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50 to 400 cps)

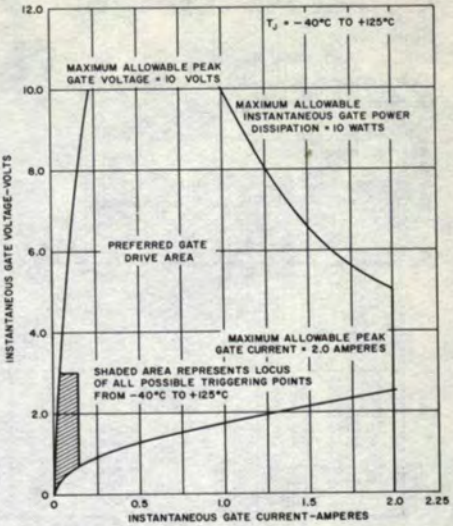
RMS Forward Current, On-State, I_t . . . . . 110 amperes (all conduction angles)
Average Forward Current, On-State, $I_{F(AV)}$ . . . . . Depends on conduction angle (see Chart 2)
Peak One-cycle Surge Forward Current, I_{FM} (surge) . . . . . 1000 amperes
I^2t (for fusing) . . . . . 4000 ampere² seconds (for times $\leq$ 1.5 milliseconds)
Max. Initial Rate of Rise of Forward Current . . . . . 5 amps/μsec
Peak Gate Power Dissipation, P_{GM} . . . . . 10 watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 2 watts
Peak Forward Gate Voltage, V_{GFM} . . . . . 10 volts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 volts
Storage Temperature, T_{stg} . . . . . −40°C to +150°C
Operating Junction Temperature, T_J . . . . . −40°C to +125°C
Stud Torque . . . . . 150 inch-pounds

CHARACTERISTICS

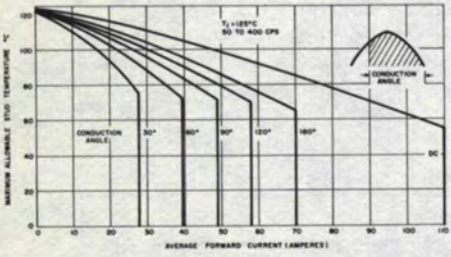
Test	Symbol	Min.	Typ.	Max	Units	Test Conditions
Gate Trigger Current	I_{GT}	....	20	125	mAdc	$T_J = +25°C$, $V_{FX} = 6V$, $R_L = +50$ ohms
			50	150	mAdc	$T_J = -40°C$, $V_{FX} = 6V$, $R_L = 50$ ohms
			10	100	mAdc	$T_J = +125°C$, $V_{FX} = 6V$, $R_L = 50$ ohms
Gate Trigger Voltage	V_{GT}		1.25	3	volts	$T_J = -40°C$ to $+125°C$, $V_{FX} = 6V$, $R_L = 50$ ohms
		0.15			volts	$T_J = +125°C$, $V_{FX} = 6V$, $R_L = 50$ ohms
Holding Current	I_{HO}		20	500	mAdc	$T_J = +25°C$, Anode supply 22 vdc
Turn-on Time (Delay Time + Rise Time)	$t_d + t_r$		8		μsec	$T_J = +25°C$, $I_F = 5$Adc, V_{FXM} = Rated. Gate Supply 125 ma max., 3V max 0.1 μsec max. rise time
Circuit Commutated Turn-Off Time	t_{off}		50		μsec	$T_J = +125°C$, $I_{FM} = 250A$, $V_R = 150$ volts max, V_{FXM} = Rated Rate of rise of reapplied Forward Blocking Voltage = 20v/μsec LINEAR
Effective Thermal Resistance	θ_{J-C}		.15	.3	°C/W	Junction to Stud
Exponential Rate of Rise of Forward Blocking Voltage	dv/dt	200	500		V/μsec	V_{FOM} = Rated, $T_J = 125°C$ Gate open $dv/dt = \left(\frac{V_{FOM}}{\tau}\right) .632$



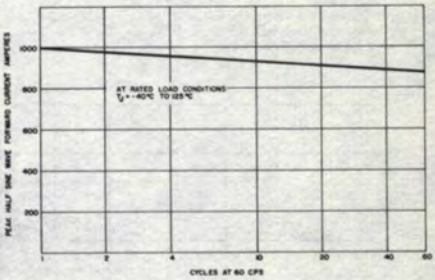
1. Forward Conduction Characteristic



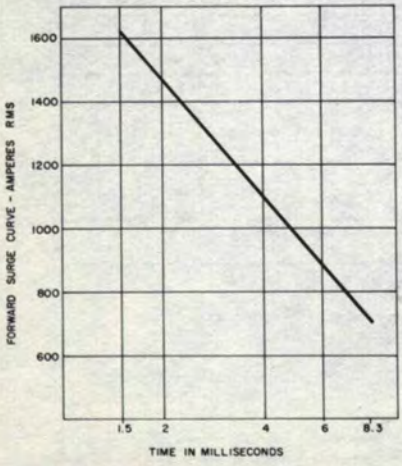
3. Firing Characteristic



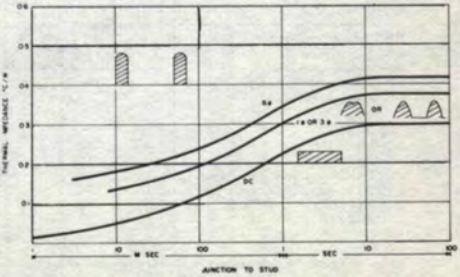
2. Maximum Allowable Stud Temperature for Sinusoidal Current Waveform



4. Maximum Allowable Surge Current



5. Sub-Cycle Surge Rating



6. Transient Thermal Impedance

C80 (Type 2N2542-2N2548)

High Current
Silicon Controlled Rectifier
235 Amperes RMS Max.
Outline Drawing No. 8

- Broad Voltage Range—up to 700 Volts
- Hard Solder Joints
- Welded Seals
- Freedom from Thermal Fatigue
- Fast Devices Available on Special Request

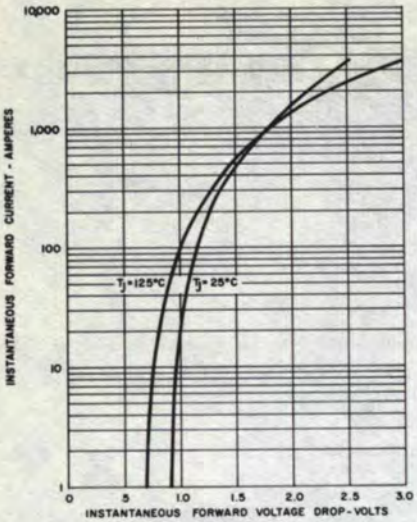
Type	Minimum Forward Breakover Voltage $V_{(BR)\,FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec.) V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$
2N2542 C80F	50	50	100
2N2543 C80A	100	100	200
2N2544 C80B	200	200	300
2N2545 C80C	300	300	400
2N2546 C80D	400	400	500
2N2547 C80E	500	500	625
2N2548 C80M	600	600	750
C80S	700	700	875
C80N	800	800	1000

MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50 to 400 cps)

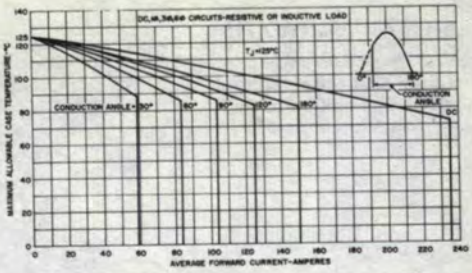
RMS Forward Current, On-State, I_T ..... 235 amperes (all conduction angles)
Average Forward Current, On-State, $I_{F(AV)}$ ..... Depends on conduction angle (see Chart 3)
di/dt ..... Depends on voltage (see Chart 6)
Peak One-cycle Surge Forward Current, $I_{FM(surge)}$ ..... 3500 amperes
I^2t (for fusing) −40 to +125°C ..... 32,000 ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Gate Power Dissipation, P_{GM} ..... 10 watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 2 watts
Peak Forward Gate Voltage, V_{GFM} ..... 10 volts
Peak Reverse Gate Voltage, V_{GRM} ..... 5 volts
Storage Temperature, T_{stg} ..... −40°C to +150°C
Operating Junction Temperature, T_J ..... −40°C to +125°C
Stud Torque ..... 300 inch-pounds

CHARACTERISTICS

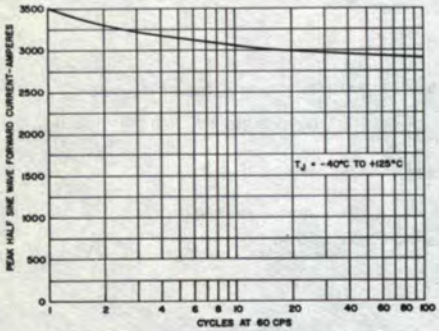
Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Gate Trigger Current	I_{GT}	....	35	125	mAdc	$T_J = +25°C$, $V_{FX} = 6V$, $R_L = +50\Omega$
		....	50	150	mAdc	$T_J = -40°C$, $V_{FX} = 6V$, $R_L = 50\Omega$
		....	10	100	mAdc	$T_J = +125°C$, $V_{FX} = 6V$, $R_L = 50\Omega$
Gate Trigger Voltage	V_{GT}	....	1.25	3	volts	$T_J = -40°C$ to $+125°C$, $V_{FX} = 6V$, $R_L = 50\Omega$
		0.15	....	....	volts	$T_J = +125°C$, $V_{FX} = 6V$, $R_L = 50\Omega$
Peak On-Voltage	V_{FM}	....	1.7	2.0	volts	$T_J = +25°C$, $I_{FM} = 1500$ A peak
Holding Current	I_{HO}	....	12	100	mAdc	$T_J = +25°C$, Anode supply 22 vdc
Turn-on Time (Delay Time + Rise Time)	$t_d + t_r$	....	5	....	μsec	$T_J = +25°C$, $I_F = 5$ Adc, V_{FXM} = Rated, Gate-supply 10 volts open gate, 25 ohm, 0.1 μsec max rise time
Circuit Commutated Turn-Off Time	t_{off}	....	30	....	μsec	$T_J = +125°C$, $I_{FM} = 250A$, $V_R = 50$ volts max, V_{FXM} = Rated, Rate of rise of reapplied Forward Blocking Voltage = 20v/μsec linear
Effective Thermal Resistance	$\theta_{J\text{-}C}$	....	.165	.18	°C/W	Junction to Case (D-c)
Exponential Rate of Rise of Forward Blocking Voltage	dv/dt			....	V/μsec	V_{FOM} = Rated, $T_J = 125°C$ $dv/dt = \left(\frac{V_{FOM}}{\tau}\right)(.632)$
2N2542 C80F		4	30			
2N2543 C80A		4	30			
2N2544 C80B		4	20			
2N2545 C80G		4	20			
2N2546 C80D		4	20			
2N2547 C80E		4	20			
2N2548 C80M		4	15			
C80S		4	15			
C80N		4	15			



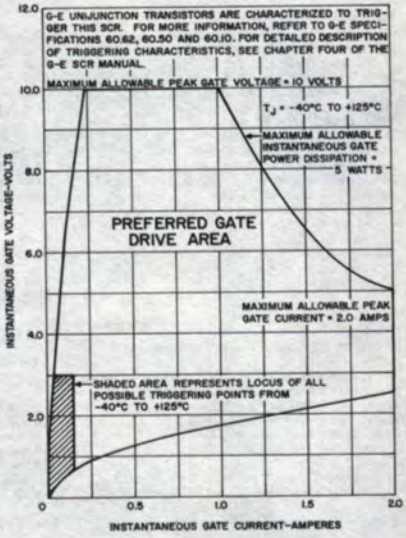
1. Maximum Forward Characteristics—On-State, High Current Level



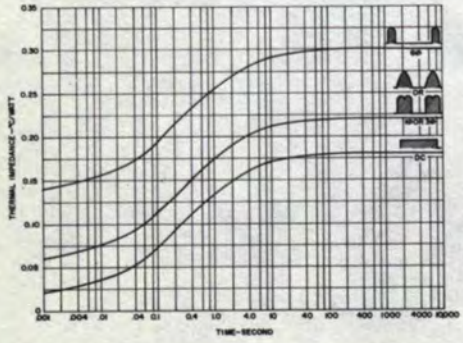
2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



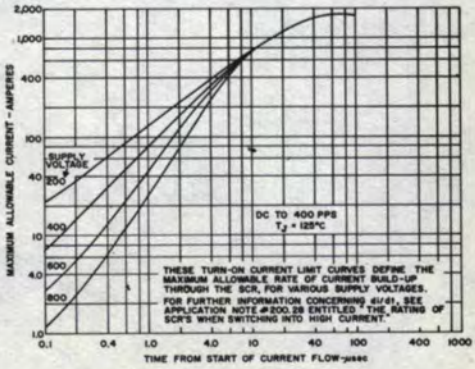
4. Maximum Allowable Non-Recurrent Peak Surge Forward Current At Rated Load Conditions



3. Gate Triggering Characteristics



5. Transient Thermal Impedance—Junction To Case



6. Current Limit For Steep Waveform Operation

6RW71A–6RW71H

Very High Current
Silicon Controlled Rectifier
470 Amperes RMS Max.
Outline Drawing No. 9

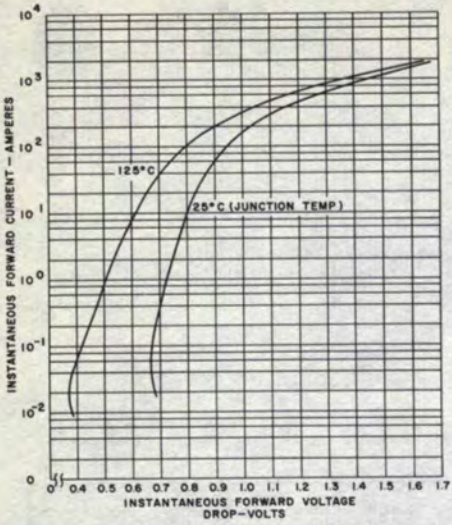
MAXIMUM ALLOWABLE RATINGS (Resistive or Inductive Load, 50 to 400 cps)

	6RW71A	6RW71B	6RW71C	6RW71D	6RW71E	6RW71F	6RW71G	
Repetitive Peak Reverse Voltage V_{ROM} (rep)	50	100	150	200	250	300	350	Volts
Repetitive Peak Forward Blocking Voltage (PFV)	400 volts							
RMS Forward Current, I_F	470 (For all conduction angles)							
Avg. Forward Current, $I_{F(AV)}$	Depends on conduction angle See Fig. 3 and 4							
Peak One Cycle Surge Current, $I_{FM(surge)}$	5500 amperes							
I^2t (for fusing)	Up to 120,000 ampere² seconds							
Peak Gate Power, P_{GM}	16 watts							
Average Gate Power, $P_{G(AV)}$	3.0 watts							
Peak Gate Current, I_{GFM}	4.0 amperes							
Peak Gate Voltage Forward, V_{GFM}	10 volts							
Reverse, V_{GRM}	5 volts							
Storage and Operating Junction Temperature, T_{stg} and T_J	−40°C to +125°C							
Stud Torque	280 inch-pounds maximum							

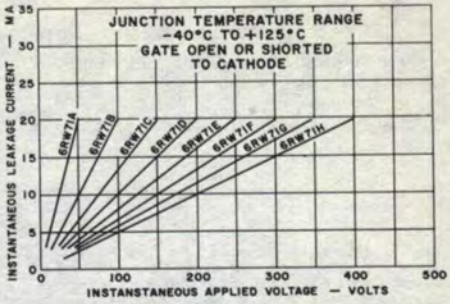
CHARACTERISTICS AT MAXIMUM RATINGS (125°C Junction Temperature)

	50	100	150	200	250	300	350	Volts
Minimum Forward Breakover Voltage $V_{(BR)FO}$								
Max. Reverse $I_{ROM(AV)}$ or Forward $I_{FOM(AV)}$ Blocking Current (Full Cycle Average)	10							
Max. on Voltage $V_{FM(AV)}$	0.65 volts (300 amp avg., 180° conduction angle)							
Max. Thermal Resistance, θ_{J-C}	13°C/W 1 ϕ							
Typical Holding Current, I_{HO}	25 ma							
Typical Gate Current to Trigger, I_{GT}	30 ma at + 1.0 volts (gate to cathode voltage)							
Typical Turn-on Time ($t_d + t_r$)	0.5–4.5 microseconds							
Typical Delay Time (t_d)	0.1–1.0 microseconds } Depends on Circuit							
Typical Rise Time (t_r)	0.4–3.5 microseconds							
Typical Turn-off Time (t_{off})	Depends on Circuit							

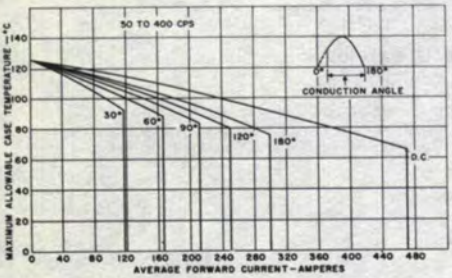
6RW71H	6RW71KY	6RW71MY	
400	500	600	volts



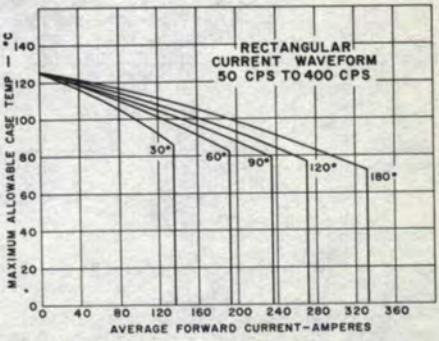
1. Maximum Forward Characteristics—Conducting State—High Current Level



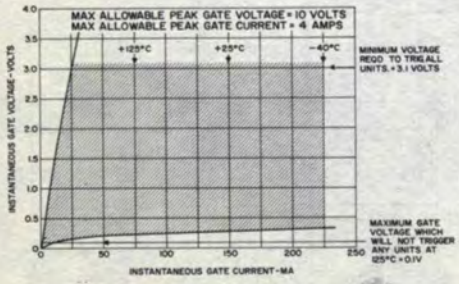
2. Maximum Reverse and Forward Blocking Characteristics



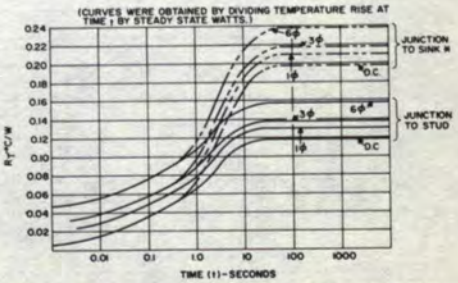
3. Maximum Allowable Case Temperature for Sinusoidal Current Waveform



4. Maximum Allowable Case Temperature for Rectangular Current Waveform



5. Triggering Characteristics



* JUNCTION TO SINK VALUES ARE TRUE ONLY IF RECOMMENDED MOUNTING PROCEDURE IS FOLLOWED. THESE VALUES ARE MEASURED TO A POINT ON THE SINK 1/4" FROM THE LARGEST RADIUS OF THE HEX.

6. Transient Thermal Resistance

L8, L9
L811, L911 (Diamond Base*) Series

Light Activated Silicon Controlled Rectifier
Up to 1.6 amps
Up to 200 volts
Outline Drawing No. 1

The L8, L9 Light Activated SCR's are basically Silicon Controlled Rectifiers with incident light taking the place of (or adding to) an electrical gate current. Thus it is a photo-operated device that is truly a switch. It features optional gate triggering inputs; i.e., from either an isolated light source or direct electrical supply. The former trigger technique offers a range of light trigger intensity with varying gate bias. The L8, L9 is expected to be particularly useful in such applications as . . .

Optical logic control
Counting
Sorting
Meter relays
Precision indexing
Explosion proof isolated switches
Static relays

This series conforms to the JEDEC TO-5 package outline with a .218 circular glass window in the top of the cap.
* The L811 and L911 series are identical to the L8 and L9 respectively except that they are soldered to a diamond base heat sink. See Chart 6.

Types†	Peak Forward Blocking** Voltage, V_{FXM}. $T_J = -65°C$ to $+100°C$ $R_{GK} = 56{,}000$ Ohms Maximum	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM}(rep) $T_J = -65°C$ to $+100°C$	Non-repetitive Peak Reverse Voltage, V_{ROM}(non-rep) (<5 Millisec.) $T_J = -65°C$ to $+100°C$
L8U, L9U	25 Volts	25 Volts	40 Volts
L8F, L9F	50 Volts	50 Volts	75 Volts
L8A, L9A	100 Volts	100 Volts	150 Volts
L8G, L9G	150 Volts	150 Volts	225 Volts
L8B, L9B	200 Volts	200 Volts	300 Volts

† The diamond base versions are L811U, 9L11U, L811F, etc.

MAXIMUM ALLOWABLE RATINGS

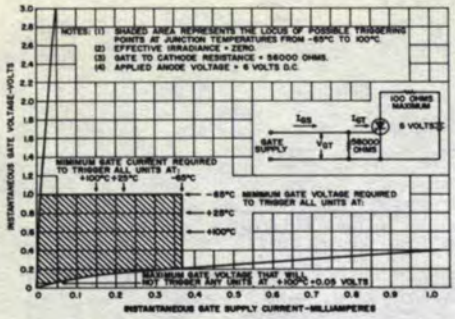
Peak Forward Voltage, PFV . . . . . 300 Volts
RMS Forward Current, On-state . . . . . 1.6 Amperes
Average Forward Current, On-state . . . . . Depends on conduction angle (see charts 5 and 6)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (Surge) . . . . . 15 Amperes
I^2t (for fusing) . . . . . 0.5 Ampere² Seconds (for times <1.5 milliseconds)
Peak Forward Gate Power Dissipation, P_{GM} . . . . . 0.1 Watt
Average Forward Gate Power Dissipation, P_G (AV) . . . . . 0.01 Watt
Peak Gate Voltage, Forward and Reverse, V_{GFM} and V_{GRM} . . . . . 6 Volts
Storage Temperature, T_{stg} . . . . . $-65°C$ to $+150°C$
Operating Temperature . . . . . $-65°C$ to $+100°C$
Peak Non-recurrent Surge Forward Current During Turn-on Time Interval (Current Rise Time <5 Microseconds) . . . . . 40 Amperes

** H_e <0.08 mw/cm² for L8 types and H_e <0.02 mw/cm² for L9 types.

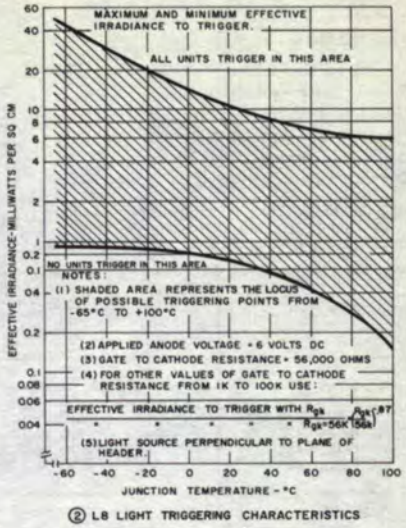
CHARACTERISTICS

Test		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Holding Current		I_{HX}	20	75	560	μamperes	$T_J = +25°C$, $V_{FX} = 5$ vdc, $H_e = 0$, $R_{GK} = 56{,}000$ ohms
			10	40	450	μamperes	$T_J = +100°C$, $V_{FX} = 5$ vdc, $H_e = 0$, $R_{GK} = 56{,}000$ ohms
			30	180	750	μamperes	$T_J = -65°C$, $V_{FX} = 5$ vdc, $H_e = 0$, $R_{GK} = 56{,}000$ ohms
Effective Irradiance to Trigger	L8	H_{ET}	0.68	5.0	10.0	milliwatts/Cm²	$T_J = +25°C$
	L9		0.68	2.0	4.2		
	L8		0.15	2.0	6.0		$T_J = +100°C$
	L9		0.15	0.7	2.5		
	L8		0.9	15.0	50.0		$T_J = -65°C$
	L9		0.9	4.0	20.0		
	L8		0.02	.....	.....		$T_J = +100°C$, $R_{GK} = 56{,}000$ ohms, $V_{FX} =$ Rated V_{FXM}, $R_L = 500$ ohms
	L9		0.02	.....	.....		
Rate of Rise of Applied Forward Voltage	L8U, L9U	dv/dt	0.01	0.02	.....	volts/μsec	$V_{FXM} = 25$ volts
	L8F, L9F		0.02	0.04	.....		$V_{FXM} = 50$ volts
	L8A, L9A		0.05	0.07	.....		$V_{FXM} = 100$ volts
	L8G, L9G		0.07	0.10	.....		$V_{FXM} = 150$ volts
	L8B, L9B		0.09	0.12	.....		$V_{FXM} = 200$ volts
							$T_J = +100°C$, $R_{GK} = 56{,}000$ ohms
Delay Time		t_d	.....	1 to 100	.....	μsec	See Application Note
Rise Time		t_r	.....	0.6	.....	μsec	$T_J = +25°C$, $I_F = 1.0$ ampere, $V_{FX} =$ Rated V_{FXM}
Circuit—Commutated Turn-off Time		t_{off}	.....	40	.....	μsec	$T_J = +100°C$, $I_{FM} = 1.0$ ampere, I_R (recovery) = 1.0 ampere

Reapplied V_{FXM} = Rated V_{FXM}, Rate of rise of Reapplied V_{FXM} = 20 volts per μsec, $R_{GK} = 100$ ohms, $H_e = 0$

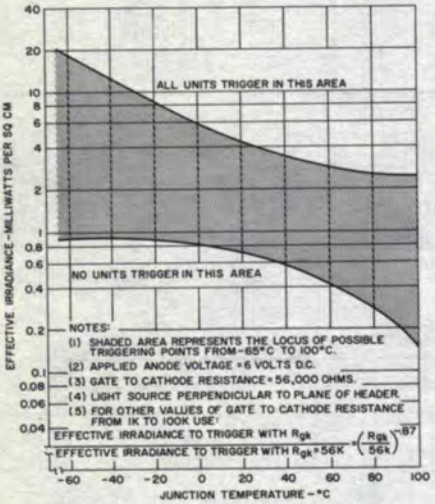


1. Electrical Gate Triggering Characteristics

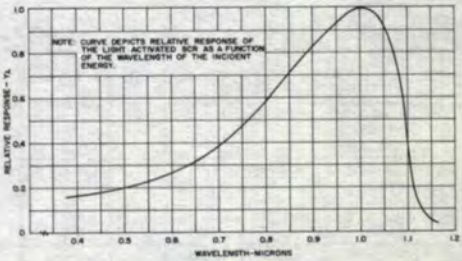


② L8 LIGHT TRIGGERING CHARACTERISTICS

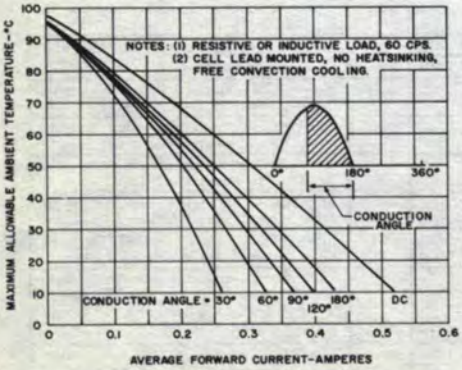
2. L8 Light Triggering Characteristics



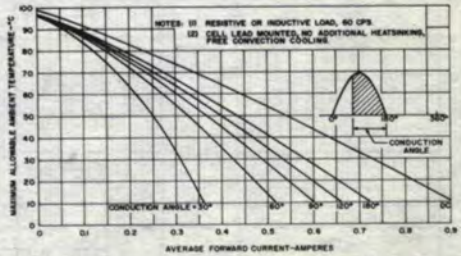
3. L9 Light Triggering Characteristics



4. Typical Spectral Response

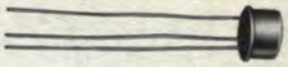


5. Maximum Ambient Temperature for Half Wave Rectified Sine Wave Current



6. Maximum Ambient Temperature for Half Wave Rectified Sine Wave Current (Diamond Base)

G5 Series
G6 Series



GATE TURN-OFF SWITCHES
Silicon Type—all diffused
Up to 1 ampere (G5 Series)
Up to 2 amperes (G6 Series)
Up to 400 volts
Outline Drawing No. 1

- Guaranteed Turn-off Gain at High Anode Current Levels (G6 Series)
- Characterized for Pulse Duty in D-C Circuits
- Low Holding Current (G5 Series)
- High Speed Operation

Type	Minimum Forward Breakover Voltage $V_{(BR)FX}$† $T_J = -65°C$ to $+100°C$	Repetitive Peak Reverse Voltage $V_{RXM(rep)}$† $T_J = -65°C$ to $+100°C$
G5U, G6U	25 Volts	25 Volts
G5F, G6F	50 Volts	25 Volts
G5A, G6A	100 Volts	25 Volts
G5B, G6B	200 Volts	25 Volts
G5C, G6C	300 Volts	25 Volts
G5D, G6D	400 Volts	25 Volts

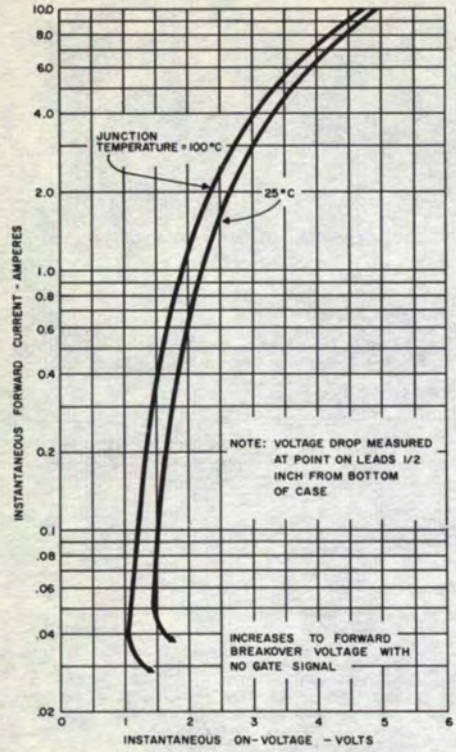
† Applies only with 1000 ohms or less connected between gate and cathode.

MAXIMUM ALLOWABLE RATINGS

Repetitive Peak Forward Blocking Voltage, P_{FV} . . . . . 500 volts
RMS Forward Current, I_f On-state . . . . . 1.4 amperes
Average Forward Current, $I_{F(AV)}$ On-state . . . . . 0.25 amperes at 30°C ambient (50% duty cycle)
Peak Rectangular Surge Forward Current, 5 milliseconds, $I_{FM(surge)}$ . . . . . 5 amperes
Peak Gate Power Dissipation, P_{GM} . . . . . .3 watts
Peak Gate Current, Forward and Reverse, I_{GFM} and I_{GRM} . . . . . 0.5 amperes
Peak Gate Voltage, Forward and Reverse V_{GFM} and V_{GRM} . . . . . 6 volts
Storage Temperature, T_{stg} . . . . . −65°C to +125°C
Operating Junction Temperature, T_J . . . . . −65°C to +100°C

CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Forward Blocking Current G5, G6	I_{FXM}	. . .	2	10	μa	T_J =25°C, R_{GK} =1000 ohms, V_{FXM} =rated peak forward voltage
Peak Forward Blocking Current	I_{FXM}					T_J =100°C, R_{GK} =1000 ohms
G5UB, G6UB		. . .	40	100	μa	V_{FXM} =25 volts peak
G5C, G6C		. . .	30	80	μa	V_{FXM} =300 volts peak
G5D, G6D		. . .	20	60	μa	V_{FXM} =400 volts peak
Peak Reverse Blocking Current	I_{RXM}	. . .	2	10	μa	T_J =25°C V_{RXM} =25 volts peak, R_{GK} =1000 ohms
Peak Reverse Blocking Current	I_{RXM}	. . .	40	100	μa	T_J =100°C V_{RXM} =25 volts peak, R_{GK} =1000 ohms
Gate Trigger Current	I_{GTM}	. . .	G5 G6	G5 G6		T_J =25°C, V_{FX} =6 vdc, R_L =30 ohms
			4 10	10 20	ma	Gate pulse width =20 μsec
		. . .	2 5	. . . .	ma	T_J =100°C, V_{FX} =6 vdc, R_L, 30 ohms, Gate pulse width =20 μsec
		. . .	40 100	. . . .	ma	T_J = −65°C, V_{FX} =6 vdc, R_L =30 ohms, Gate pulse width =20 μsec
Gate Trigger Voltage	V_{GTM}	0.5	1.0	2.0	volts	T_J =25°C, V_{FX} =6 vdc, R_L =30 ohms, Gate pulse width =20 μsec
		. . .	0.6	. . . . .	volts	T_J =100°C, V_{FX} =6 vdc, R_L =30 ohms, Gate pulse width =20 μsec.
		. . .	3.0	. . . . .	volts	T_J = −65°C, V_{FX} =6 vdc, R_L =30 ohms, Gate pulse width =20 μsec
Turn-off Gain	G_I	5	8	. . . . .		T_J =100°C, gate pulse width =10μsec, I_F =0.2 amp to 1 amp for G5 series, I_F =0.5 amp to 2 amp for G6 series
Peak On Voltage	V_{FM}	. . .	1.8	2.2	volts	T_J =25°, I_{FM} =1 amp
Holding Current	I_{HX}	. . .	G5 G6	G5 G6	ma	T_J =25°C, anode supply =24 volts.
			20 40	40 60		R_{GK} =1000 ohms
Rise Time	t_r	. . .	1.0	. . . . .	μsec	T_J =25°C, I_F =1 amp
Fall Time	t_f	. . .	1.0	. . . . .	μsec	T_J =25°C, I_F =1 amp

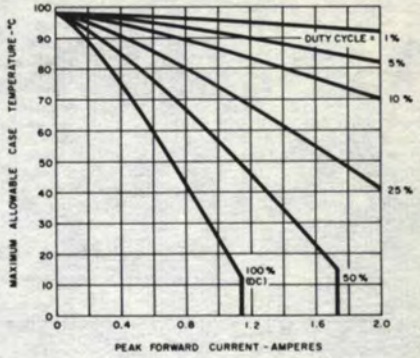


1. Maximum Forward Characteristics—On-State

NOTES (1) RATINGS DERIVED FOR RECTANGULAR CURRENT PULSES AND APPLY FOR RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 CPS.

(2) CASE TEMPERATURE MEASURED AT TAB ON HEADER.

(3) RATINGS DERIVED FOR 0.01 WATTS AVERAGE GATE POWER DISSIPATION.

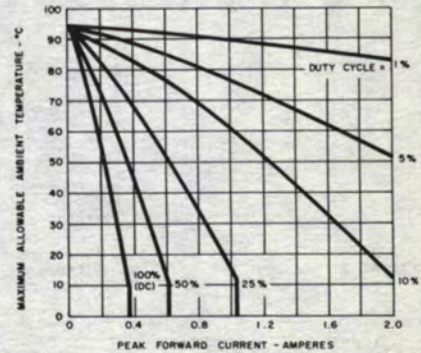


2. Maximum Allowable Case Temperature vs. Peak Forward Current

NOTES (1) RATINGS DERIVED FOR RECTANGULAR CURRENT PULSES AND APPLY FOR RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 CPS.

(2) CELL LEAD MOUNTED, NO HEAT SINK, FREE CONVECTION COOLING.

(3) RATINGS DERIVED FOR 0.01 WATTS AVERAGE GATE POWER DISSIPATION.



3. Maximum Allowable Ambient Temperature vs. Peak Forward Current

2N2646 & 2N2647

Unijunction Transistors—Silicon Types

Outline Drawing No. 10

The General Electric 2N2646 and 2N2647 Silicon Unijunction Transistors have an entirely new structure resulting in lower saturation voltage, peak-point current and valley current as well as a much higher base-one peak pulse voltage. In addition, these devices are much faster switches.

The 2N2646 is intended for general purpose industrial applications where circuit economy is of primary importance, and is ideal for use in triggering circuits for Silicon Controlled Rectifiers and other applications where a guaranteed minimum pulse amplitude is required. The 2N2647 is intended for applications where a low emitter leakage current and a low peak point emitter current (trigger current) are required (i.e. long timing applications), and also for triggering high power SCR's.

ABSOLUTE MAXIMUM RATINGS: (25°C)

Power Dissipation (Note 1).....300 mw
RMS Emitter Current.....50 ma
Peak Emitter Current (Note 2).....2 amperes
Emitter Reverse Voltage.....30 volts
Interbase Voltage.....35 volts
Operating Temperature Range −65°C to +125°C
Storage Temperature Range.. −65°C to +150°C

ELECTRICAL CHARACTERISTICS: (25°C)

PARAMETER		2N2646			2N2647			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Intrinsic Standoff Ratio (V_{BB} =10V)	η	0.56	0.65	0.75	0.68	0.75	0.82	
Interbase Resistance (V_{BB} =3V, I_E =0)	R_{BBO}	4.7	7	9.1	4.7	7	9.1	KΩ
Emitter Saturation Voltage (V_{BB} =10V, I_E =50 ma)	$V_{E(SAT)}$		2			2		volts
Modulated Interbase Current (V_{BB} =10V, I_E =50 ma)	$I_{B2(MOD)}$		12			12		ma
Emitter Reverse Current (V_{B2E} =30V, I_{B1} =0)	I_{EO}		0.05	12		0.01	0.2	μa
Peak Point Emitter Current (V_{BB} =25V)	I_P		0.4	25		0.4	2	μa
Valley Point Current (V_{BB} =20V, R_{B2} =100Ω)	I_V	4	6		8	11	18	ma
Base-One Peak Pulse Voltage (Note 3) SCR Firing Conditions (See Figure 26, back page)	V_{OB1}	3.0	6.5		6.0	7.5		volts

NOTES:

1. Derate 3.0 MW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.
2. Capacitor discharge—10 μfd or less, 30 volts or less.
3. The Base-One Peak Pulse Voltage is measured in the circuit below. This specification on the 2N2646 and 2N2647 is used to ensure a minimum pulse amplitude for applications in SCR triggering circuits and other types of pulse circuits.
4. The intrinsic standoff ratio, η, is essentially constant with temperature and interbase voltage. η is defined by the equation:

$$V_P = \eta V_{BB} + V_D$$

Where V_P = Peak Point Emitter Voltage
V_{BB} = Interbase Voltage
V_D = Junction Diode Drop (Approx. .5V)

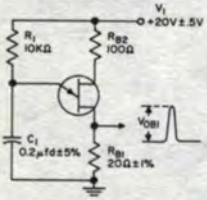


FIGURE 1

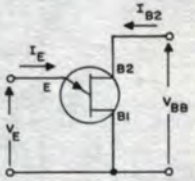


FIGURE 2
Unijunction Transistor Symbol with Nomenclature used for voltage and currents.

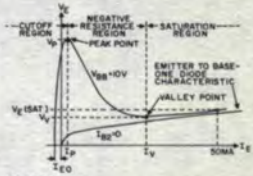


FIGURE 3
Static Emitter Characteristics curves showing important parameters and measurement points (exaggerated to show details).

G-E SCR's, RECTIFIERS, AND UNIJUNCTION TRANSISTORS WORK WELL TOGETHER!

G-E Controlled Rectifier (SCR) Type	Compatible Rectifier: G-E Rectifier Type	Max On-Current $I_{F(AV)}$ at Stud Temperature	Peak 1 Cycle Surge	Max. Rectifier Transient V_{RM} (non-rep)	Package	Compatible Unijunction Triggering Transistor
C5, C7, 2N1595–1599	1N536–1N547	.75 A at 50°C Amb.	15 A	800 V	Double Ended Lead	2N2646
	1N2610–1N2615	.75 A at 50°C Amb.	30 A	775 V		
C8, C9	1N1341A–1N1348B	7 A at 140°C	150 A	800 V	7/16" Hex	2N2646
C10, C11, C12	CAR A27	8.5 A at 150°C	240 A	∞	7/16" Hex	
C20, C22, C30	A40 or A41 A44 or A45	15 A at 150°C	300 A	600 V	9/16" Hex	2N2646
C35, C38, C40	1N1199A–1N1206A	12 A at 150°C	240 A	800 V	7/16" Hex	2N2646
	1N2154–1N2160	25 A at 145°C	400 A	800 V	11/16" Hex	2N2646
	CAR A38	22 A at 140°C	500 A	∞	11/16" Hex	
C36,C37	1N1341A–1N1348A	7 A at 140°C	150 A	800 V	7/16" Hex	2N2646
	1N1199A–1N1206A	12 A at 150°C	240 A	800 V	7/16" Hex	2N2646
C45, C46, C50, C52, C55 C56, C60, C61, C150	1N3289–1N3293 (A70)	70 A at 150°C	1600 A	1300 V	1–1/16" Hex	2N2647
	CAR A76	70 A at 150°C	1600 A	∞		
C80, C85	1N3736–3742 (A90)	200 A at 150°C	4500 A	1300 V	1–1/4" Hex	2N2647
	CAR A92	200 A at 150°C	4500 A	∞		
6RW71	1N3736–3742 (A90)	200 A at 150°C	4500 A	1300 V	1–1/4" Hex	2N2647
	CAR A92	200 A at 150°C	4500 A	∞		
	6RW62	390 A at 150°C	7000 A	1000 V	1–5/8" Hex	2N2647

Stock assemblies available for all rectifier types listed.

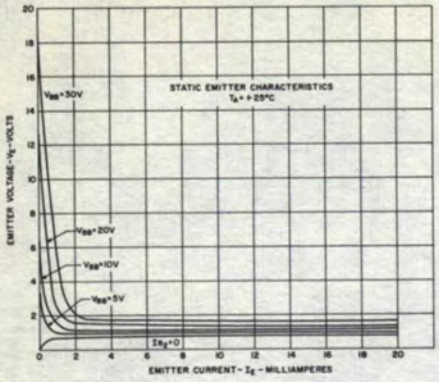


FIGURE 4

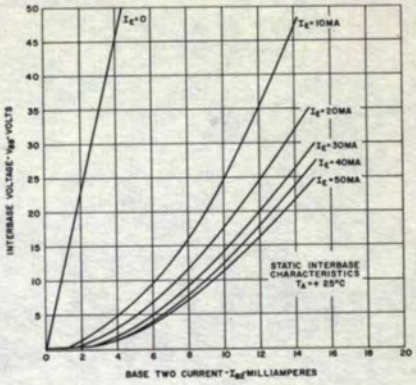


FIGURE 5

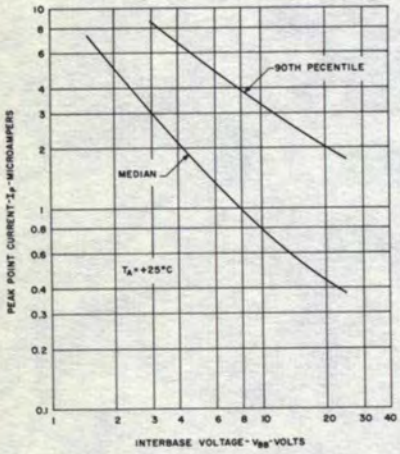


FIGURE 6

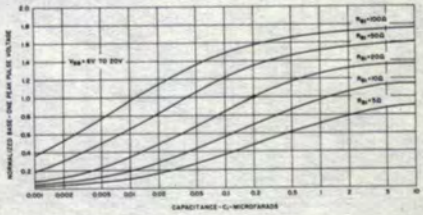


FIGURE 7

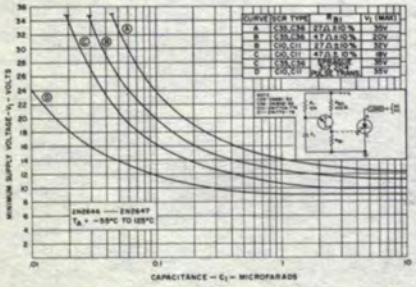


FIGURE 8—BOTH TYPES—LO & MED. SCR's

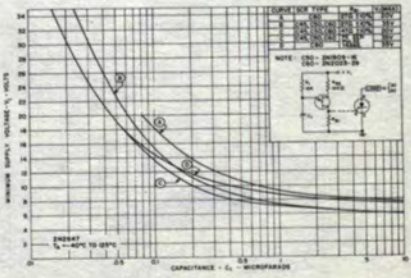


FIGURE 9—2N2647—HI CURRENT SCR's

Note: For simultaneous Firing of more than one SCR see Section 4.13.5.

RECTIFIER CELLS . . . CONDENSED SPECIFICATIONS

A casual glance through the circuits on the foregoing pages shows that diode rectifier cells play an important role in SCR circuitry. Rectifiers in series with SCR's help them to block reverse voltage. Other rectifiers act as free-wheeling elements across inductive loads, and some circuits employ rectifiers as companion elements to SCR's in the non-controllable legs of bridge circuits. Low current rectifiers appear in large numbers of every practical SCR circuit as power supplies for control purposes, and as clamps and blocking elements in SCR gate triggering circuits.

General Electric activity with metallic rectifiers dates back to 1927 when copper oxide ruled the dry type rectifier field unchallenged. Ten years later G.E. introduced its line of selenium rectifiers.

More recently, in 1950, General Electric made the first single crystal large area rectifier cell. Fabricated from germanium, this cell was the grandfather of the vast germanium and silicon rectifier industry that has sprung up in the decade since then.

In addition to their vital help in SCR circuitry, silicon and germanium rectifier cells have contributed to the success of the SCR in another significant way. In order to develop the first successful SCR, G.E. drew heavily on its long experience in designing and manufacturing reliable rectifier cells. Without the large storehouse of rectifier "know-how," the SCR might not be a reality even today. Welded hermetic seals, high voltage characteristics, surface stabilization techniques, absence of thermal fatigue limitations, rating and application philosophies . . . these are only a few of the areas in which the SCR capitalized on G-E rectifier preeminence.

General Electric's work in subduing Thermal Fatigue, a major Semiconductor killer, has helped earn it the reputation of being the quality Semiconductor Rectifier producer of the industry. In addition, the Rectifier Components Department has recognized the problems associated with transient voltages and developed a complete line of controlled avalanche rectifiers which are self protecting against normal voltage transients.

In medium and high-current rectifiers, General Electric has completely eliminated soft solder joints, thus greatly reducing the problem of thermal fatigue. This means that G-E Rectifiers and Controlled Rectifiers can be worked right up to maximum current and temperature ratings, even on highly cyclical loads.

In addition to the controlled avalanche rectifiers, all other General Electric rectifiers and Controlled Rectifiers carry *transient* reverse voltage ratings which give the user additional protection against voltage transients.

The rectifier cells shown are listed in ascending order based on forward current ratings in each section. Maximum full load voltage drop is taken at full cycle average unless otherwise specified.

Finned Assemblies

General Electric silicon rectifiers, controlled rectifiers, and controlled avalanche rectifiers are also available in pre-assembled stacks complete with heatsink and electrical interconnections for a great variety of typical rectifier circuits.

Potted High Voltage Assemblies

For applications up to 10,000 volts, low current silicon rectifiers are available in preassembled encapsulated blocks. When controlled avalanche rectifiers are used in these high voltage potted assemblies, no balancing resistors are needed; and with recently developed matching techniques, shunt capacitors are minimized, even eliminated in some applications. With the A7, A27, A38, A76 and A92 con-

trolled avalanche diodes as building blocks, high voltage assemblies with current ratings from a few milliamperes to hundreds of amperes are available.

You will also find a General Electric rectifier cell or stack available for every job to be done in conjunction with SCR's.

The following pages list the various rectifiers together with condensed specifications on each.

Complete specifications are available through your Semiconductor Products District Sales office or through your authorized G-E Semiconductor Distributor.

G-E rectifiers and SCR's work well together.

Silicon Subminiature Glass Rectifier Cells

Up to 600 ma
Up to 600 volts

For A7 Control Avalanche Rectifier, See Page 387
Designed for maximum thermal conductance.
Rugged design to meet military requirements.
Insulated Housing.

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	V_{RM} (non-rep)	Max. $I_{F(AV)}$		Max. Rev. Current I_{RM}	Max. Oper. Temp. T_A in °C	Outline No.
			T_A25°C	150°C	T_A =100°C		
1N645	225	275	400 ma	150 ma	15 μa	175	11
1N646	300	360	400 ma	150 ma	15 μa	175	11
1N647	400	480	400 ma	150 ma	20 μa	175	11
1N648	500	600	400 ma	150 ma	20 μa	175	11
1N649	600	720	400 ma	150 ma	25 μa	175	11
Meets MIL-E-1/1143 & 19500/240A Specifications							
					T_A =150°C		
1N676	100	120	200 ma	75 ma	.2 ma	175	11
1N677	100	120	400 ma	150 ma	.2 ma	175	11
1N678	200	240	200 ma	75 ma	.2 ma	175	11
1N679	200	240	400 ma	150 ma	.2 ma	175	11
1N681	300	360	200 ma	75 ma	.2 ma	175	11
1N682	300	360	400 ma	150 ma	.2 ma	175	11
1N683	400	480	200 ma	75 ma	.2 ma	175	11
1N684	400	480	400 ma	150 ma	.2 ma	175	11
1N685	500	600	200 ma	75 ma	.2 ma	175	11
1N686	500	600	400 ma	150 ma	.2 ma	175	11
1N687	600	720	200 ma	75 ma	.2 ma	175	11
1N689	600	720	400 ma	150 ma	.2 ma	175	11
					T_A =175°C		
1N3544	100	120	600 ma	250 ma	75 μa	200	11
1N3545	200	240	600 ma	250 ma	75 μa	200	11
1N3546	300	360	600 ma	250 ma	75 μa	200	11
1N3547	400	480	600 ma	250 ma	75 μa	200	11
1N3548	500	600	600 ma	250 ma	75 μa	200	11
1N3549	600	720	600 ma	250 ma	75 μa	200	11
Low leakage at High temperature							

Germanium Low Current Rectifier Cells

Up to 1200 ma
Up to 400 volts

Feature extremely low forward resistance, high back resistance.
Industry standard for high reliability units.

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM}(Surge)	Max. Rev. Current $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.
		@ 55°C					
1N93	300	75 ma	25A	.6 ma	.18V	95°C	12
USN 1N93	300	75 ma	25A	.6 ma	.18V	95°C	12
1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio 700 @ 55°C		85°C	12
USAF 1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio 700 @ 55°C .3 ma @ 150		85°C	12
1N368	200	100 ma	25A	V.D.C.	.48V	55°C	12
1N92	200	100 ma	25A	.95 ma	.19V	95°C	12
1N91	100	150 ma	25A	1.35 ma	.22V	95°C	12
1N153	300	750 ma	25A			95°C	13
1N158	400	1000 ma	25A			95°C	14
1N152	200	1000 ma	25A			95°C	13
1N151	100	1200 ma	25A			95°C	13
Very Low Forward Voltage Drop							

Silicon Low Current Top Hat Rectifier Cells

Up to 750 ma
Up to 1000 volts

These low current top hat alloy junction silicon rectifiers are designed for maximum forward conductance at high operating temperatures. A prime feature of these devices is that high current loads are carried *without the use of any external heat sink whatsoever.* The reverse current at maximum junction temperature is maintained at an extremely low level, making the devices ideal for magnetic amplifier and other low leakage applications.

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM}(Surge)	Max. Rev. Current $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.
		@ 50°C		@ 25°C	@ 25°C		
1N440	100	300 ma	15A	.3 μa	1.5V peak	150°C	12
1N441	200	300 ma	15A	.75 μa	1.5V	150°C	12
1N442	300	300 ma	15A	1.0 μa	1.5V	150°C	12
1N443	400	300 ma	15A	1.5 μa	1.5V	150°C	12
1N444	500	300 ma	15A	1.75 μa	1.5V	150°C	12
1N445	600	300 ma	15A	2.0 μa	1.5V	150°C	12
1N440B	100	750 ma	15A	0.3 μa	1.5V	165°C	12
1N441B	200	750 ma	15A	0.75 μa	1.5V	165°C	12
1N442B	300	750 ma	15A	1.0 μa	1.5V	165°C	12
1N443B	400	750 ma	15A	1.5 μa	1.5V	165°C	12
1N444B	500	650 ma	15A	1.75 μa	1.5V	150°C	12
1N445B	600	650 ma	15A	2.0 μa	1.5V	150°C	12
Low Leakage —Transient Voltage Ratings Up to 800V							
		@ 25°C			@ 200 ma		
1N599	50	600 ma	10A	1.0 μa	1.5V peak	150°C	12
1N599A	50	600 ma	10A	1.0 μa	1.5V	150°C	12
1N600	100	600 ma	10A	1.0 μa	1.5V	150°C	12
1N600A	100	600 ma	10A	1.0 μa	1.5V	150°C	12
1N601	150	600 ma	10A	1.0 μa	1.5V	150°C	12
1N601A	150	600 ma	10A	1.0 μa	1.5V	150°C	12
1N602	200	600 ma	10A	1.0 μa	1.5V	150°C	12
1N602A	200	600 ma	10A	1.0 μa	1.5V	150°C	12
1N603	300	600 ma	10A	1.0 μa	1.5V	150°C	12
1N603A	300	600 ma	10A	1.0 μa	1.5V	150°C	12
1N604	400	600 ma	10A	1.5 μa	1.5V	150°C	12
1N604A	400	600 ma	10A	1.5 μa	1.5V	105°C	12
1N605	500	600 ma	10A	2.0 μa	1.5V	150°C	12
1N605A	500	600 ma	10A	2.0 μa	1.5V	150°C	12
1N606	600	600 ma	10A	2.5 μa	1.5V	150°C	12
1N606A	600	600 ma	10A	2.5 μa	1.5V	150°C	12
		@ 30°C		@ 150°C	@ 150°C		
1N560	800	600 ma	15A	.3 ma	0.5V	150°C	12
1N561	1000	600 ma	15A	.3 ma	0.5V	150°C	12
Now Transient PRV Ratings Up to 1200V							
		@ 50°C		@ 100°C	@ 100°C		
1N1692	100	600 ma	20A	.5 ma	0.6V	115°C	12
1N1693	200	600 ma	20A	.5 ma	0.6V	115°C	12
1N1694	300	600 ma	20A	.5 ma	0.6V	115°C	12
1N1695	400	600 ma	20A	.5 ma	0.6V	115°C	12
1N1696	500	600 ma	20A	.5 ma	0.6V	115°C	12
1N1697	600	600 ma	20A	.5 ma	0.6V	115°C	12
Lowest Price Series, Lower Temp. & Current than 1N536–47 Series							
		@ 50°C		@ 150°C			
1N1100	100	750 ma	15A	.3 ma	1.5V peak	165°C	12
1N1101	200	750 ma	15A	.3 ma	1.5V	165°C	12
1N1102	300	750 ma	15A	.3 ma	1.5V	165°C	12
1N1103	400	750 ma	15A	.3 ma	1.5V	165°C	12
Very Low Leakage. Ideal for Magnetic-amplifier Applications. Premium Price.							
		@ 25°C		@ 125°C	@ 125°C		
1N1487	100	750 ma	15A	.4 ma	.55 V	140°C	12
1N1488	200	750 ma	15A	.3 ma	.55V	140°C	12
1N1489	300	750 ma	15A	.3 ma	.55V	140°C	12
1N1490	400	750 ma	15A	.3 ma	.55V	140°C	12
1N1491	500	750 ma	15A	.3 ma	.55V	125°C	12
1N1492	600	750 ma	15A	.3 ma	.55V	120°C	12
Similar to 1N536–47 Series. Intermediate Temp. Operation. Lower Priced.							

Silicon Low Current Top Hat Rectifier Cells, Cont.

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM}(Surge)	Max. Rev. Current $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.
		@ 50°C		@ 150°C	@ 150°C		
1N536	50	750 ma	15A	.4 ma	.5V	165°C	12
1N537	100	750 ma	15A	.4 ma	.5V	165°C	12
1N538*	200	750 ma	15A	.3 ma	.5V	165°C	12
1N539	300	750 ma	15A	.3 ma	.5V	165°C	12
1N540*	400	750 ma	15A	.3 ma	.5V	165°C	12
1N1095	500	750 ma	15A	.3 ma	.5V	150°C	12
1N1096	600	750 ma	15A	.3 ma	.5V	150°C	12
1N547*	600	750 ma	15A	.3 ma	.5V	165°C	12

The popular line. Transient voltage ratings up to 800V.

* Military Approved units also available.

		@ 110°C		@ 150°C	@ 125°C		
1N1217	50	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1217A					1.0V	175°C	12
1N1218	100	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1218A					1.0V	175°C	12
1N1219	150	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1219A					1.0V	175°C	12
1N1220	200	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1220A					1.0V	175°C	12
1N1221	300	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1221A					1.0V	175°C	12
		@ 100°C					
1N1222	400	500 ma	15A	1.5 ma	1.0V	175°C	12
		@ 110°C					
1N1222A		500 ma			1.0V	175°C	12
		@ 100°C					
1N1223	500	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1223A		@ 110°C			1.0V	175°C	12
		@ 90°C					
1N1224	600	500 ma	15A	1.5 ma	1.0V	175°C	12
1N1224A		@ 110°C			1.0V	175°C	12
		@ 85°C			@ 150°C		
A10A	100	.9A	45A	.4 ma	.5V	165°C	12
A10B	200	.9A	45A	.4 ma	.5V	165°C	12
A10C	300	.9A	45A	.4 ma	.5V	165°C	12
A10D	400	.9A	45A	.4 ma	.5V	165°C	12
A10E	500	.9A	45A	.4 ma	.5V	165°C	12
A10M	600	.9A	45A	.4 ma	.5V	165°C	12
A10N	800	.9A	45A	.4 ma	.5V	150°C	12
A10P	1000	.9A	45A	.4 ma	.5V	150°C	12

High Surge ratings desired in dimmer circuits and television and radio voltage doublers.

Silicon Low Current Rectifier Cells

Stud Mounted
Up to 1.5 amps
Up to 1000 volts

JEDEC or G-E Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Cur. $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A °C	Outline No.
		@ 150°C Case		@ 150°C			
1N340	100	200 ma	10A	1 ma	2V @ 400 ma	170	16
1N349	100	200 ma	10A	1 ma	2V @ 400 ma	170	16
1N337	200	200 ma	10A	1 ma	2V @ 400 ma	170	16
1N346	200	200 ma	10A	5 ma	2V @ 400 ma	170	16
1N335	300	200 ma	10A	2 ma	2V @ 400 ma	170	16
1N344	300	200 ma	10A	5 ma	2V @ 400 ma	170	16
1N333	400	200 ma	10A	2 ma	2V @ 400 ma	170	16
1N342	400	200 ma	10A	5 ma	2V @ 400 ma	170	16

Silicon Low Current Rectifier Cells, Cont.

JEDEC or G-E Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Cur. $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A °C	Outline No.
1N339	100	400 ma	15A	1 ma	2V @ 800 ma	170	16
1N348	100	400 ma	15A	5 ma	2V @ 800 ma	170	16
1N336	200	400 ma	15A	1 ma	2V @ 800 ma	170	16
1N345	200	400 ma	15A	5 ma	2V @ 800 ma	170	16
1N334	300	400 ma	15A	2 ma	2V @ 800 ma	170	16
1N343	300	400 ma	15A	5 ma	2V @ 800 ma	170	16
1N332	400	400 ma	15A	2 ma	2V @ 800 ma	170	16
1N341	400	400 ma	15A	5 ma	2V @ 800 ma	170	16
Popular Series.							
		@ 100°C Case					
1N562	800	400 ma	15A	3 ma	.65V @ 150°C	150	16
1N563	1000	400 ma	15A	3 ma	.65V @ 150°C	150	16
1N-560-61 mounted on studs.							
		@ 100° Amb.		@ 25°C	@ T_c =25°C		
1N550	100	500 ma	4A, 3 ms	.5 μa	1.5V	150	16
1N551	200	500 ma	4A, 3 ms	1.0 μa	1.5V	150	16
1N552	300	500 ma	4A, 3 ms	1.5 μa	1.5V	150	16
1N553	400	500 ma	4A, 3 ms	2.5 μa	1.5V	150	16
1N554	500	500 ma	4A, 3 ms	3.5 μa	1.5V	150	16
1N555	600	500 ma	4A, 3 ms	5.0 μa	1.5V	150	16
Very low leakage for magnetic amplifier applications. The 1N440B-5B series mounted on studs.							
		@ 135° Case		@ 135°C			
1N253*	95	1000 ma	15A	.1 ma	1.2V @ 1A	170	16
1N254*	190	800 ma	15A	.1 ma	1.2V @ 1A	170	16
1N255*	380	800 ma	15A	.15 ma	1.2V @ 1A	170	16
1N256*	570	600 ma	15A	.25 ma	1.2V @ 1A	155	16
* Military Approved units also available—Mil-S-19500/194A. Refer also to 1N1115-1120 Series.							
		@ 100°C Amb.		@ 25°C	@ 25°C		
1N607	50	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N607A	50	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150	16
1N608	100	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N608A	100	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150	16
1N609	150	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N609A	150	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150	16
1N610	200	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N610A	200	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150	16
1N611	300	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N611A	300	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150	16
1N612	400	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N612A	400	1A	2A, .1 sec	.0015 ma	1.5V @ 200 ma	150	16
1N1613	500	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N613A	500	1A	2A, .1 sec	.002 ma	1.5V @ 200 ma	150	16
1N614	600	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150	16
1N614A	600	1A	2A, .1 sec	.0025 ma	1.5V @ 200 ma	150	16
		@ 85° Case		@ 150°C			
1N1115	100	1.5A	15A	.4 ma	.65V @ 150°C	170	16
1N1116	200	1.5A	15A	.3 ma	.65V @ 150°C	170	16
1N1117	300	1.5A	15A	.3 ma	.65V @ 150°C	170	16
1N1118	400	1.5A	15A	.3 ma	.65V @ 150°C	170	16
1N1119	500	1.3A	15A	.3 ma	.65V @ 150°C	155	16
1N1120	600	1.3A	15A	.3 ma	.65V @ 150°C	155	16
The popular line. 1N536-40, 1N547, 1N1095-6 mounted on studs.							

Silicon Low Current Flangeless Rectifier Cells

Up to 1 Amp
Up to 800 volts

The most desirable features of the top hat, such as long life, reliability and unit stability have been incorporated into this smaller package. These devices feature:

- High Surge Capability
- Thermal Fatigue Free Operation
- Transient Reverse Voltage Ratings
- Hermetically Sealed
- Small, Easy to Mount Package
- Strong Welded Tube Seal

JEDEC or G-E Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ at T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.
		@ 50°C		@ 150°C	@ 150°C		
1N2610	100	750 ma	30A	.3 ma	.5V	175°C	15
1N2611	200	750 ma	30A	.3 ma	.5V	175°C	15
1N2612	300	750 ma	30A	.3 ma	.5V	175°C	15
1N2613	400	750 ma	30A	.3 ma	.5V	175°C	15
1N2614	500	750 ma	30A	.3 ma	.5V	175°C	15
1N2615	600	750 ma	30A	.3 ma	.5V	175°C	15
		@ 75°C		@ 25°C	@ 25°C		
1N3639	200	750 ma	40A	10 μa	1.2V	100°C	15
1N3640	400	750 ma	40A	10 μa	1.2V	100°C	15
1N3641	600	750 ma	40A	10 μa	1.2V	100°C	15
1N3642	800	500 ma	40A	10 μa	1.2V	100°C	15
		@ 100°C		@ 150°C			
1N3189	200	1.A	30A	.5 ma	1.0V	175°C	15
1N3190	400	1.A	30A	.5 ma	1.0V	175°C	15
1N3191	600	1.A	30A	.5 ma	1.0V	175°C	15

A new line of silicon low current diffused rectifiers in the flangeless package designed to meet the stringent requirements of Mil-S-19500.

Silicon Medium Current Rectifier Cells

Up to 35 amperes
Up to 1000 volts

The major features of these designs are:

- High Junction Temperatures
- Hard-Solder, Thermal Fatigue Free
- Solid One-piece Terminal
- Low Thermal Impedance
- Transient PRV Ratings
- For A27 and A38 Controlled Avalanche Rectifiers, See Page 387.

These rectifiers may be mounted directly to a chassis or fin or may be insulated by using insulating kit provided. Most units are also available with negative polarity (stud is anode).

JEDEC or G-E Type Number	$V_{RM(rep)}$ or $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_C	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ Full Load	Max. T_J in °C	Outline No.
		@ 85°C		@T_A = 150°C		
1N3569	100	3.5A	35A	.4 ma	165	16
1N3570	200	3.5A	35A	.4 ma	165	16
1N3571	300	3.5A	35A	.4 ma	165	16
1N3572	400	3.5A	35A	.4 ma	165	16
1N3573	500	3.5A	35A	.4 ma	165	16
1N3574	600	3.5A	35A	.4 ma	165	16
1N3958	100	3.5A	35A	.4 ma	165	16
1N3959	200	3.5A	35A	.4 ma	165	16
1N3960	300	3.5A	35A	.4 ma	165	16
1N3961	400	3.5A	35A	.4 ma	165	16
1N3962	500	3.5A	35A	.4 ma	165	16
1N3963	600	3.5A	35A	.4 ma	165	16

Fast recovery diodes for high frequency power applications.

Silicon Medium Current Rectifier Cells, Cont.

JEDEC or G-E Type Number	$V_{RM(rep)}$ or $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ Full Load	Max. T_J in °C	Outline No.
		@ 150°C		@ T_C = 150°C		
1N1612	50	5A	150A	1 ma	190	16
1N1613	100	5A	150A	1 ma	190	16
1N1614*	200	5A	150A	1 ma	190	16
1N1615*	400	5A	150A	1 ma	190	16
1N1616*	600	5A	150A	1 ma	190	16
* Meets MIL-S-19500/162A U.S. Army Spec—also in reverse polarity 1N1612R–1616R.						
		@ 145°C				
1N1341A	50	6A	150A	3 ma	200	16
1N1342A	100	6A	150A	2.5 ma	200	16
1N1343A	150	6A	150A	2.25 ma	200	16
1N1344A	200	6A	150A	2.0 ma	200	16
1N1345A	300	6A	150A	1.75 ma	200	16
1N1346A	400	6A	150A	1.5 ma	200	16
1N1347A	500	6A	150A	1.25 ma	200	16
1N1348A	600	6A	150A	1.0 ma	200	16
Reverse units 1N1341RA–1348RA available.						
		T_C = 145°C		T_C = 150°C		
1N1199A	50	12A	240A	3.0 ma	200	16
1N1200A	100	12A	240A	2.5 ma	200	16
1N1201A	150	12A	240A	2.25 ma	200	16
1N1202A	200	12A	240A	2.0 ma	200	16
1N1203A	300	12A	240A	1.75 ma	200	16
1N1204A	400	12A	240A	1.5 ma	200	16
1N1205A	500	12A	240A	1.25 ma	200	16
1N1206A	600	12A	240A	1.0 ma	200	16
Designed to meet Mil-E-1/1108 USAF Spec. Reverse Polarity 1N1199RA–1206RA.						
		@ 150°C				
1N3670A	700	12A	240A	.9 ma	200	16
1N3671A	800	12A	240A	.8 ma	200	16
1N3672A	900	12A	240A	.7 ma	200	16
1N3673A	1000	12A	240A	.6 ma	200	16
New High Voltage—Long Creepage Path Housing—Diffused Junction.						
		T_C = 150°C		T_C = 150°C		
1N248	50	10A	200A	5 ma	175	17
1N249	100	10A	200A	5 ma	175	17
1N250	200	10A	200A	5 ma	175	17
1N248A	50	20A	350A	5 ma	175	17
1N249A	100	20A	350A	5 ma	175	17
1N250A	200	20A	350A	5 ma	175	17
1N248B	55	20A	350A	5 ma	175	17
1N249B*	110	20A	350A	5 ma	175	17
1N250B*	220	20A	350A	5 ma	175	17
1N2135*	400	20A	250A	40 ma	150	17
* Available as military units to Mil-S-19500/134.						
1N248C	55	20A	350A	3.8 ma	175	17
1N249C	110	20A	350A	3.6 ma	175	17
1N250C	220	20A	350A	3.4 ma	175	17
1N1195A	300	20A	350A	3.2 ma	175	17
1N1196A	400	20A	350A	2.5 ma	175	17
1N1197A	500	20A	350A	2.2 ma	175	17
1N1198A	600	20A	350A	1.5 ma	175	17
				T_C = 145°C		
1N2154	50	25A	400A	5 ma	200	17
1N2155	100	25A	400A	4.5 ma	200	17
1N2156	200	25A	400A	4.0 ma	200	17
1N2157	300	25A	400A	3.5 ma	200	17
1N2158	400	25A	400A	3.0 ma	200	17
1N2159	500	25A	400A	2.5 ma	200	17
1N2160	600	25A	400A	2.0 ma	200	17
Available with negative polarity (stud is anode) 1N2154R–2160R.						

Silicon Medium Current Rectifier Cells, Cont.

JEDEC or G-E Type Number	$V_{RM(rep)}$ or $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ Full Load	Max. T_J in °C	Outline No.
		T_C = 140°C		T_C = 140°C		
1N1183	50	35A	500A	10 ma	200	20
1N1184	100	35A	500A	10 ma	200	20
1N1185	150	35A	500A	10 ma	200	20
1N1186	200	35A	500A	10 ma	200	20
1N1187	300	35A	500A	10 ma	200	20
1N1188	400	35A	500A	10 ma	200	20
1N1189	500	35A	500A	10 ma	200	20
1N1190	600	35A	500A	10 ma	200	20
1N3765	700	35A	500A	10 ma	200	20
1N3766	800	35A	500A	10 ma	200	20
1N3767	900	35A	500A	10 ma	200	20
1N3768	1000	35A	500A	10 ma	200	20
New High Voltage—Long Creepage Path Housing.						

General Purpose Types
Up to 20 amperes
Up to 600 volts

General Electric has designed these 20 Ampere rectifiers specifically for the normal industrial and consumer *low ambient temperature* applications. The design utilizes the smallest practical size for the rating with particular attention to rigidity and rugged construction. The solid one-piece terminal and the case-to-hex solder mounting technique provides good mechanical strength, minimizes breakage problems, and promotes stability of heat transfer characteristics from the diffused junction to the stud.

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$		I_{FM}(surge)	Max. Rev. Cur. $I_{R(AV)}$ @ Full Load	Max. T_J in °C	Outline No.
		T_C = 110°C	T_C = 150°C				
A40F, A41F	50	20A	15A	300A	10 ma	175	18
A40A, A41A	100	20A	15A	300A	9 ma	175	18
A40B, A41B	200	20A	15A	300A	8 ma	175	18
A40C, A41C	300	20A	15A	300A	6 ma	175	18
A40D, A41D	400	20A	15A	300A	5 ma	175	18
A40E, A40E	500	20A	15A	300A	4.5 ma	175	18
A40M, A41M	600	20A	15A	300A	4 ma	175	18
A41F–M is reverse polarity (stud is Anode)							
A44F, A45F	50	20A	15A	300A	10 ma	175	19
A44A, A45A	100	20A	15A	300A	9 ma	175	19
A44B, A45B	200	20A	15A	300A	8 ma	175	19
A44C, A45C	300	20A	15A	300A	6 ma	175	19
A44D, A45D	400	20A	15A	300A	5 ma	175	19
A44E, A45E	500	20A	15A	300A	4.5 ma	175	19
A44M, A45M	600	20A	15A	300A	4 ma	175	19
A45F–M is reverse polarity (case is Anode)							

Silicon High Current Rectifier Cells

Up to 500 amperes
Up to 1200 volts

These large area junction rectifiers are the ultimate in today's High Current Silicon Rectifier field. By taking full advantage of the most advanced semiconductor component manufacturing techniques, General Electric now offers the industry's first *double diffused, all hard solder* 100 & 250 ampere rectifiers in $V_{RM(rep)}$ ratings up to 1200 volts—also available is a 500 amp rectifier up to 800 volts. As a result, circuit designers now receive:

- Freedom from Thermal Fatigue Failure
- Higher Surge Current Capabilities
- NEMA Overload Ratings
- Forward and Reverse Polarities
- For Controlled Avalanche Types, See Page 387

G-E Type Number	JEDEC Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	$V_{RM(non-rep)}$	Max. $I_{F(AV)}$	$I_{FM(surge)}$ 1~ @60cps	Max. Rev. Cur. $I_{R(AV)}$ @ Full Load	Max. Oper. Temp. T_J in °C	Outline No.
				T_C = 130°C		T_C = 130°C		
A70B	1N3289	200	300	100A	1600A	9.5 ma	200	21
A70C	1N3290	300	400	100A	1600A	9.0 ma	200	21
A70D	1N3291	400	525	100A	1600A	9.0 ma	200	21
A70E	1N3292	500	650	100A	1600A	8.0 ma	200	21
A70M	1N3293	600	800	100A	1600A	6.5 ma	200	21
A70N	1N3294	800	1050	100A	1600A	5.5 ma	200	21
A70P	1N3295	1000	1300	100A	1600A	4.5 ma	200	21
A70PB	1N3296	1200	1500	100A	1600A	3.5 ma	200	21
A71B thru PB (1N3289R–3296R) reverse polarity units available 1N3289M–3295M Military Types per Mil-S-19500/246A A76D thru A76P—Controlled avalanche units								
A90B	1N3736	200	300	250A	4500A	16 ma	200	22
A90C	1N3737	300	400	250A	4500A	16 ma	200	22
A90D	1N3738	400	525	250A	4500A	16 ma	200	22
A90E	1N3739	500	650	250A	4500A	15 ma	200	22
A90M	1N3740	600	800	250A	4500A	12.5 ma	200	22
A90N	1N3741	800	1050	250A	4500A	10 ma	200	22
A90P	1N3742	1000	1300	250A	4500A	8 ma	200	22
A91B thru A91P (1N3736R–3742R) reverse polarity units—stud is Anode A92E thru A92P—Controlled avalanche units								
6RW62D	.....	200	400	500A	7000A	35 ma	200	23
6RW62F	.....	300	500	500A	7000A	35 ma	200	23
6RW62H	.....	400	600	500A	7000A	35 ma	200	23
6RW62K	.....	500	700	500A	7000A	35 ma	200	23
6RW62M	.....	600	800	500A	7000A	30 ma	200	23
6RW62P	.....	700	900	500A	7000A	25 ma	200	23
6RW62R	.....	800	1000	500A	7000A	23 ma	200	23
Largest single crystal diode rectifier commercially available.								

Controlled Avalanche Rectifier Cells

A7 series 0.5A — **150–500 $V_{RM(rep)}$**
A27 series 12A — **200–1200 $V_{RM(rep)}$**
A38 series 35A — **200–1200 $V_{RM(rep)}$**
A76 series 100A — **400–1200 $V_{RM(rep)}$**
A92 series 250A — **500–1000 $V_{RM(rep)}$**

Featuring these outstanding advances in silicon rectifier applications:

- Self-protection against normal voltage transient. Dissipates many watts of peak power in reverse direction. Permits decreased peak reverse voltage safety factors in equipment due to greatly reduced transient voltage vulnerability.
- New standards of reliability at peak reverse voltages.
- Protection of other circuit components against overvoltage through rigidly specified maximum/minimum avalanche characteristics.
- Make ideal voltage equalizing elements for series connected SCR's and conventional silicon rectifiers, also for anode triggering SCR's to prevent damage from voltage transients in forward direction.
- Simplified series operation of rectifiers in high voltage applications . . . no shunting resistors necessary for Controlled Avalanche Rectifiers. Makes possible compact high voltage assemblies.
- Can operate in Avalanche breakdown region at high voltages . . . unharmed by hi-pot and megger tests.

For information on application of Controlled Avalanche Rectifiers, see Section 14.3.4 and Application Note 200.27, "An Introduction to the Controlled Avalanche Silicon Rectifier."

JEDEC or G-E Type Number	$V_{RM(rep)}$ & $V_{RM(wkg)}$ Volts	Avalanche Voltage T_J = 25°C		Max. Rev. Power Surge $P_{RM(non-rep)}$	Max. $I_{F(AV)}$	I_{FM} (surge)	Max. Rev. Cur. $I_{R(AV)}$ @ $V_{RM(wkg)}$	Max. T_J in °C	Outline No.
		Min.	Max.						
				T_J = 50°C	T_A = 50°C		T_A = 150°C		
A7G	150	200	450	310W	500 ma	10A	100 μa	175	11
A7B	200	300	550	310W	500 ma	10A	100 μa	175	11
A7C	300	400	650	310W	500 ma	10A	100 μa	175	11
A7D	400	500	750	310W	500 ma	10A	100 μa	175	11
A7E	500	600	850	310W	500 ma	10A	100 μa	175	11
	Units also available in Potted Assemblies up to 10kv and 820 ma.								
				T_J = 25°C	T_C = 135°C		T_C = 135°C		
A27B	200	250	515	3.9Kw	12A	240A	2.5 ma	175	16
A27C	400	500	770	3.9Kw	12A	240A	2.5 ma	175	16
A27M	600	750	1030	3.9Kw	12A	240A	2.5 ma	175	16
A27N	800	1000	1290	3.9Kw	12A	240A	2.0 ma	175	16
A27P	1000	1250	1550	3.9Kw	12A	240A	1.75 ma	175	16
A27PB	1200	1500	1930	3.9Kw	12A	240A	1.5 ma	175	16
					T_C = 115°C		T_C = 115°C		
A38B	200	250	515	12Kw	35A	500A	3.5 ma	175	20
A38D	400	500	770	12Kw	35A	500A	3.5 ma	175	20
A38M	600	750	1030	12Kw	35A	500A	3.5 ma	175	20
A38N	800	1000	1290	12Kw	35A	500A	3.0 ma	175	20
A38P	1000	1250	1550	12Kw	35A	500A	2.5 ma	175	20
A38PB	1200	1500	1930	12Kw	35A	500A	2.0 ma	175	20
				T_J = 25°C	T_C = 130°C		T_C = 130°C		
A76D	400	600	900	2.8Kw	100A	1600A	9 ma	200	21
A76E	500	700	980	2.8Kw	100A	1600A	8 ma	200	21
A76M	600	800	1080	2.8Kw	100A	1600A	6.5 ma	200	21
A76S	700	900	1180	2.8Kw	100A	1600A	6 ma	200	21
A76N	800	1000	1280	2.8Kw	100A	1600A	5.5 ma	200	21
A76T	900	1100	1360	2.8Kw	100A	1600A	5 ma	200	21
A76P	1000	1200	1460	2.8Kw	100A	1600A	4.5 ma	200	21
A92E	500	700	1020	70Kw	250A	4500A	14 ma	200	22
A92M	600	800	1120	70Kw	250A	4500A	12.5 ma	200	22
A92S	700	900	1240	70Kw	250A	4500A	11.5 ma	200	22
A92N	800	1000	1340	70Kw	250A	4500A	10 ma	200	22
A92T	900	1100	1440	70Kw	250A	4500A	9 ma	200	22
A92P	1000	1200	1540	70Kw	250A	4500A	8 ma	200	22

THESE GENERAL ELECTRIC SILICON AND GERMANIUM POWER SEMICONDUCTORS MEET MILITARY SPECIFICATIONS

Silicon Controlled Rectifiers

Type	MIL Specification	$V_{RM(rep)}$ & $V_{(BR)FO}$	Max. $I_{F(AV)}$	Outline No.
USN 2N1771A	MIL-S-19500/168	50	7A @ 115°C Case	3
USN 2N1772A	MIL-S-19500/168	100	7A @ 115°C Case	3
USN 2N1774A	MIL-S-19500/168	200	7A @ 115°C Case	3
USN 2N1776A	MIL-S-19500/168	300	7A @ 115°C Case	3
USN 2N1777A	MIL-S-19500/168	400	7A @ 115°C Case	3
	For low power switching and control applications			
USN 2N681	MIL-S-19500/108A	25	25A @ 57°C Case	5
USN 2N682	MIL-S-19500/108A	50	25A @ 57°C Case	5
USN 2N683	MIL-S-19500/108A	100	25A @ 57°C Case	5
USN 2N684	MIL-S-19500/108A	150	25A @ 57°C Case	5
USN 2N685	MIL-S-19500/108A	200	25A @ 57°C Case	5
USN 2N686	MIL-S-19500/108A	250	25A @ 57°C Case	5
USN 2N687	MIL-S-19500/108A	300	25A @ 57°C Case	5
USN 2N688	MIL-S-19500/108A	400	25A @ 57°C Case	5
USN 2N689	MIL-S-19500/108A	500	25A @ 57°C Case	5
	For medium power switching and control applications			
USN 2N1910W	MIL-S-19500/204A	50	110A @ 60°C Case	6
USN 2N1911W	MIL-S-19500/204A	100	110A @ 60°C Case	7
USN 2N1912W	MIL-S-19500/204A	200	110A @ 60°C Case	7
USN 2N1913W	MIL-S-19500/204A	300	110A @ 60°C Case	7
USN 2N1914W	MIL-S-19500/204A	400	110A @ 60°C Case	7
USN 2N2031W	MIL-S-19500/204A	50*	110A @ 60°C Case	7
	For high power switching and control applications			

* Turn-off time 15 μsec.

	Germanium Rectifiers			
		$V_{RM(rep)}$		
USN 1N93	MIL-E-1/895	300	75 ma @ 55°C Amb.	12
USAF 1N315	MIL-E-1/1088	100	100 ma @ 71°C Amb.	12
	Silicon Subminiature Rectifiers			
USN 1N645, 647, 649	MIL-E-19500/240A	225 to 600	150 ma @ 150°C Amb.	11
USAF 1N645, 647, 649	MIL-E-1/1143	225 to 600	150 ma @ 150°C Amb.	11
	Silicon Low Current Rectifiers			
JAN 1N538, 540, 547	MIL-S-19500/202A	200 to 600	250 ma @ 150°C Amb.	12
JAN 1N253	MIL-S-19500/194A	100	1A @ 135°C Case	16
JAN 1N254, 255	MIL-S-19500/194A	200, 400	400 ma @ 135°C Case	16
JAN 1N256	MIL-S-19500/194A	600	200 ma @ 135°C Case	16
	Silicon Medium Current Rectifiers			
USA 1N1614, 1614R	MIL-S-19500/162A	200	5A @ 150°C Case	16
USA 1N1615, 1615R	MIL-S-19500/162A	400	5A @ 150°C Case	16
USA 1N1616, 1616R	MIL-S-19500/162A	600	5A @ 150°C Case	16
USAF 1N1199, 1200, 1201, 02, 03, 04, 05, 06	MIL-E-1/1108	50 to 600	12A @ 145°C Case	16
USA 1N249B	MIL-S-19500/134	125	20A @ 150°C Case	17
USA 1N250B	MIL-S-19500/134	250	20A @ 150°C Case	17
USA 1N2135A	MIL-S-19500/134	500	20A @ 150°C Case	17
	Silicon High Current Rectifiers			
USA 1N3289, 91, 93, 94, 95	MIL-S-19500/246A	200, 400, 600, 800, 1000	100A @ 130°C Case	21

Silicon Zener Diodes

1 Watt Axial Lead
Zener voltages from 5.1 to 22 volts

These 1 watt Zener Diodes utilize the all welded flangeless package for ease in mounting. This small package is a tried and proved design with an exceptional reliability history over the past several years. The design incorporates know-how which promotes very good voltage regulation, and voltage stability over a long period of time under the severest environmental conditions. Complete specifications are available upon request

RATING TABLES

JEDEC or G-E Type Number	V_{ZT} @ I_{ZT} Nominal ZENER VOLTAGE @ 25°C Volts	Test Current I_{ZT} mA	Maximum Dynamic Impedance Z_{ZT} @ I_{ZT} @ 25°C Ohms	Typical Voltage Regulation $\triangle V_Z$ Volts	MAXIMUM ZENER CURRENT I_{ZM}—MA T_A = 50°C Maximum	Outline No.	Max. T_J in °C
4JZ4X5.1B	5.1	100	7.0	0.11	160	15	175
1N1765	5.6	100	1.2	0.14	150	15	175
1N1766	6.2	100	1.5	0.16	130	15	175
1N1767	6.8	100	1.7	0.20	120	15	175
1N1768	7.5	100	2.1	0.24	109	15	175
1N1769	8.2	100	2.4	0.28	100	15	175
1N1770	9.1	50	3.0	0.34	90	15	175
1N1771	10.0	50	3.5	0.41	82	15	175
1N1772	11.0	50	4.2	0.48	74	15	175
1N1773	12.0	50	5.0	0.57	68	15	175
1N1774	13.0	50	5.8	0.66	63	15	175
4JZ4X14B	14.0	50	6.6	0.75	58	15	175
1N1775	15.0	50	7.6	0.86	54	15	175
1N1776	16.0	50	8.6	0.97	51	15	175

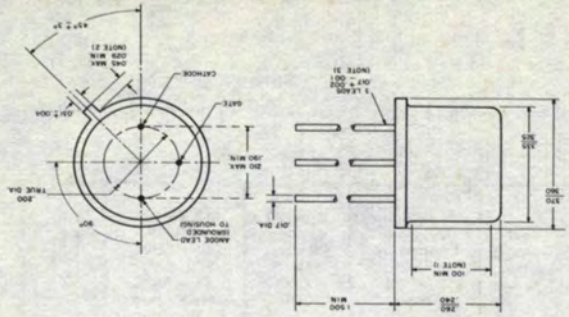
Standard types are supplied to the ±10% of voltage values listed. For 5% tolerance, change B suffix to A suffix in G-E Type Number (i.e., 4JZ4X5.1A), add A suffix in 1N number (i.e., 1N1776A).
The Z4XL6.2 to XL22 1 watt zener diodes are intended for consumer and low cost industrial applications. While designed and produced for economy, this design features low thermal resistance, good voltage regulation and stability.

Z4XL6.2	6.2	20	9.0	.....	123	15	165
Z4XL7.5	7.5	20	12.0	.....	101	15	165
Z4XL9.1	9.1	20	15.0	.....	83	15	165
Z4XL12	12.0	20	24.0	.....	63	15	165
Z4XL14	14.0	20	30.0	.....	54	15	165
Z4XL16	16.0	20	40.0	.....	47	15	165
Z4XL18	18.0	20	50.0	.....	43	15	165
Z4XL20	20.0	20	60.0	.....	38	15	165
Z4XL22	22.0	20	72.0	.....	34	15	165

Standard types are supplied to ±20% of nominal voltage values listed.
For ±10% tolerance, add suffix B to G-E type number (i.e., Z4XL6.2B).

SCR OUTLINE DRAWINGS

1



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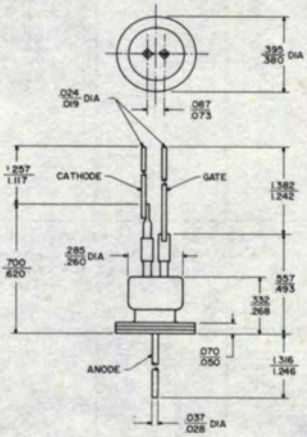

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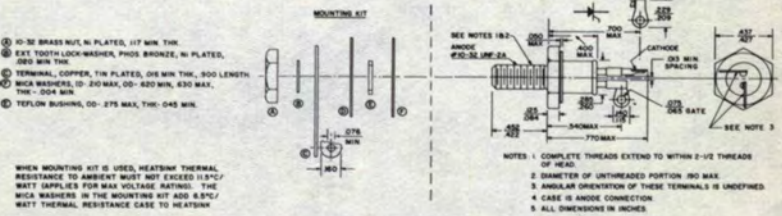

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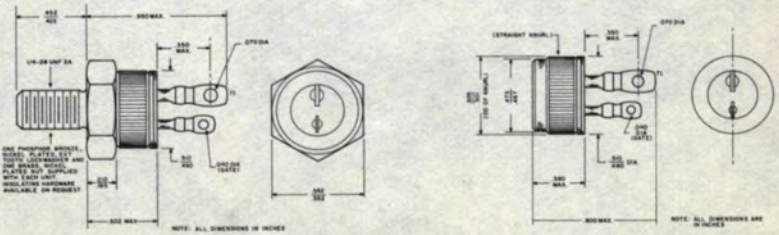

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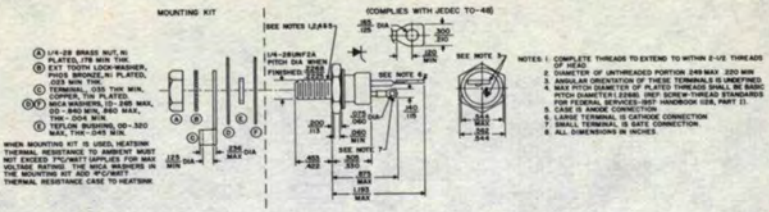

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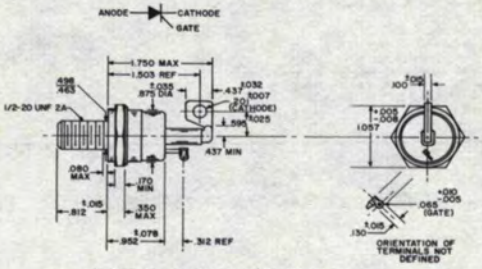
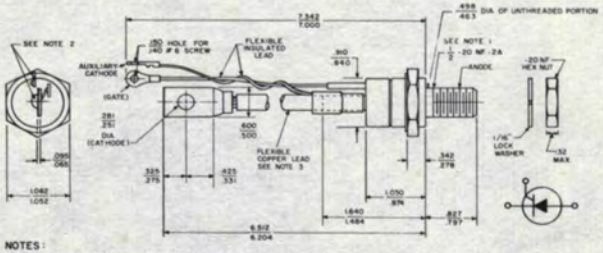


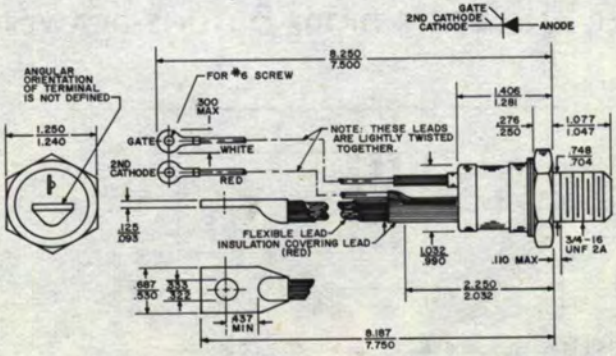
NOTE: ONE 1/2-20 BRASS NI PLATED NUT AND ONE SILICON BRONZE SPRING LOCKWASHER SUPPLIED WITH EACH UNIT.

7



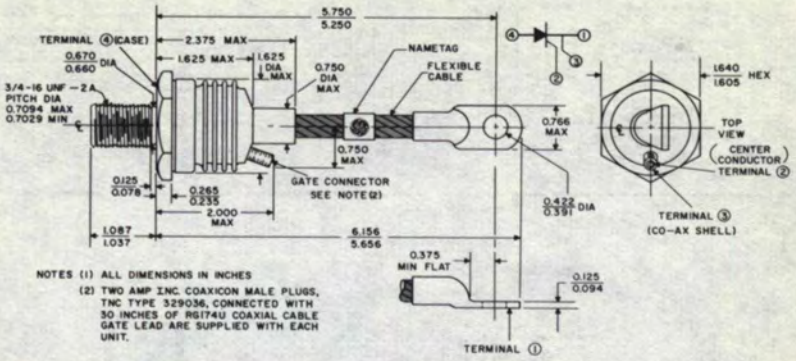
NOTES:
1. COMPLETE THREADS TO EXTEND TO WITHIN 2 1/2 THREADS OF HEAD.
2. ANGULAR ORGANIZATION OF THESE TERMINALS IS UNDEFINED.
3. LEAD COVERED WITH SILICON RUBBER INSULATION (CLASS H) 600 VOLT ASTM STANDARD WALL.
4. APPROX. WEIGHT 4 OZS.
5. CONFORMS TO JEDEC TO-49 OUTLINE.

8



NOTE: ONE BRASS NI PLATED NUT 3/4-16 AND ONE PHOSPHOR BRONZE INT. TOOTHED LOCK WASHER SUPPLIED WITH EACH UNIT.

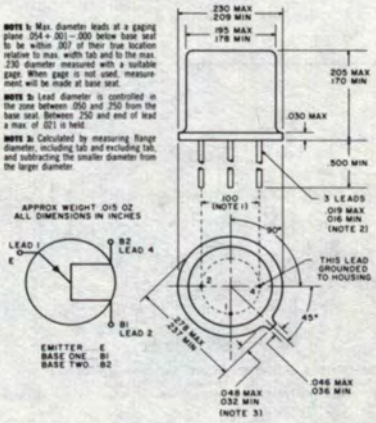
9



NOTES (1) ALL DIMENSIONS IN INCHES

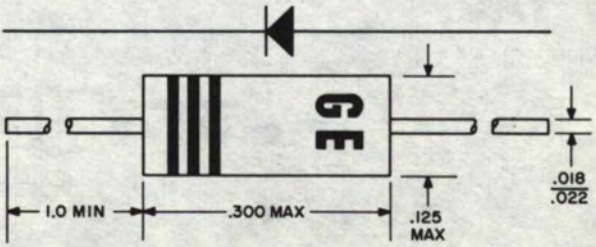
(2) TWO AMP INC. COAXICON MALE PLUGS, TNC TYPE 329036, CONNECTED WITH 30 INCHES OF RGI74U COAXIAL CABLE. GATE LEAD ARE SUPPLIED WITH EACH UNIT.

10 Unijunction Transistors 2N2646 And 2N2647



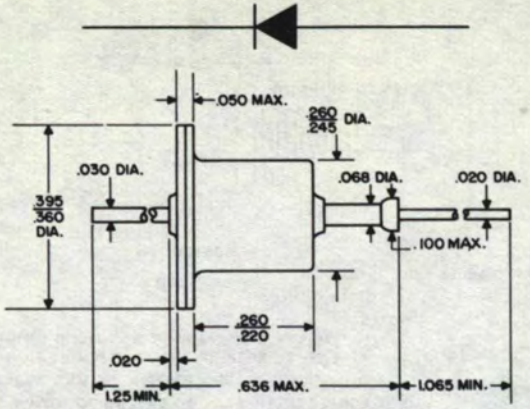
RECTIFIER AND ZENER DIODE OUTLINE DRAWINGS

11



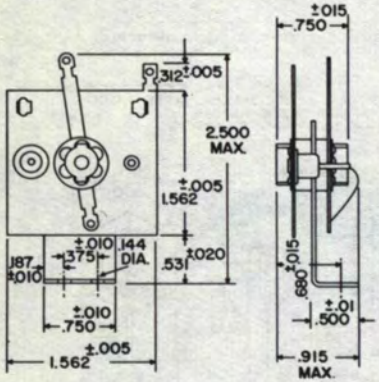
NOTES: 1. JEDEC COLOR CODED BANDS DENOTE CATHODE END
2. UNIT WEIGHT — .25 GMS

12



COMPLIES WITH EIA REGISTERED OUTLINE DO-3
APPROX. WEIGHT = .05 OZ.

13



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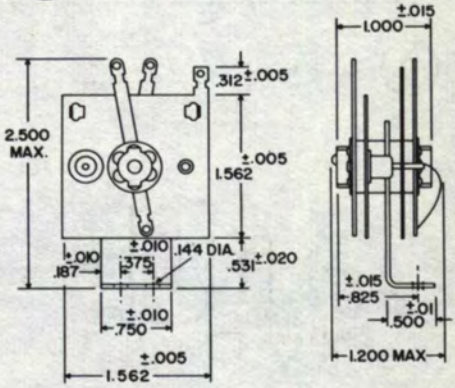

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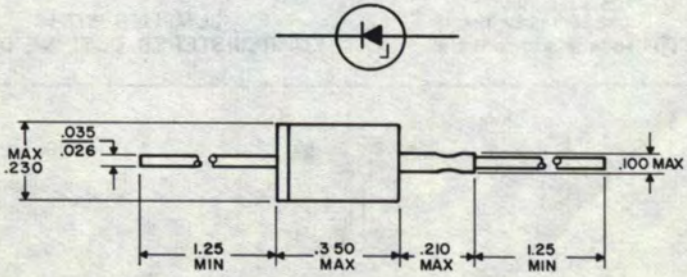

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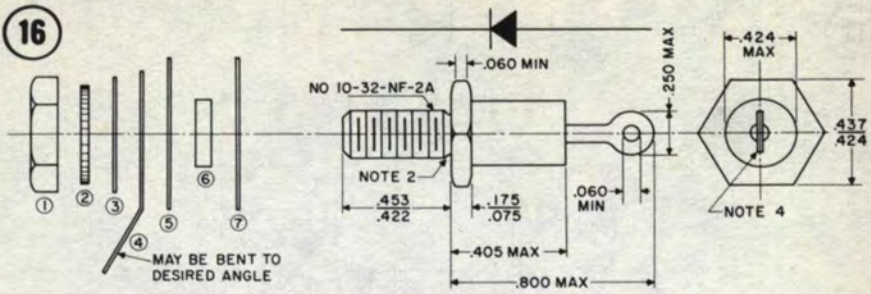


① 10-32 BRASS NI. PL. HEX. NUT
② LOCK WASHER (EXT.) STEEL NI. PL.
③ FLAT WASHER 7/16" O.D. .004 THK.
④ TERMINAL: .010 THK. COPPER TIN PL.
⑤ MICA WASHER .005 THK.
⑥ TEFLON WASHER .032 WALL THK.
⑦ MICA WASHER .005 THK.

NOTES:
1. UNIT MUST NOT BE DAMAGED BY TORQUE OF 15 IN. LB. APPLIED TO 10-32-NF-2B NUT ASSEMBLED ON THREAD.
2. DIA. OF UNTHREADED PORTION .189 MAX. AND .169 MIN.
3. COMPLETE THREADS TO EXTEND TO WITHIN 2 1/2 THREADS OF HEAD.
4. ANGULAR ORIENTATION OF THIS TERMINAL IS UNDEFINED.
5. MAXIMUM PITCH DIAMETER OF PLATED THREADS SHALL BE BASIC PITCH DIAMETER (.1697) REFERENCE SCREW THREAD STANDARD FOR FEDERAL SERVICES 1957 HANDBOOK H28 1957 PI.

COMPLIES WITH EIA REGISTERED OUTLINE DO-4

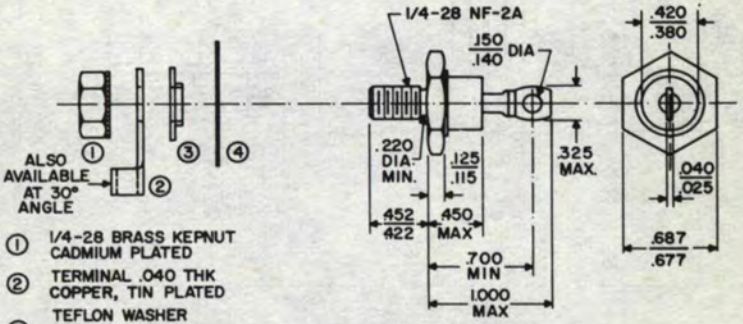
APPROX WEIGHT = .15 OZ

17

NOTE: MICA WASHER IN MOUNTING KIT MAY ADD UP TO 2.5° C/WATT THERMAL RESISTANCE STUD TO AMBIENT
UNIT WEIGHT .5 OZ.

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154 – IN2160; IN248A – IN250A; IN248B – IN250B

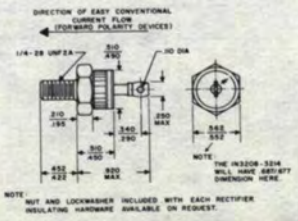
DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154R – IN2160R; IN248R – IN250R
IN248RA – IN250RA; IN248RB – IN250RB



① 1/4-28 BRASS KEPNUT CADMIUM PLATED
② TERMINAL .040 THK COPPER, TIN PLATED
③ TEFLON WASHER .025 WALL THK. .032 SHOULDER THK.
④ MICA WASHER .005 THK.

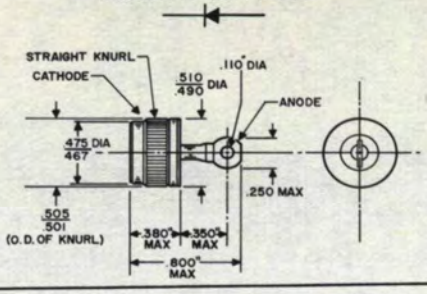
COMPLIES WITH EIA REGISTERED OUTLINE DO-5

18



19

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
(FORWARD POLARITY DEVICES)



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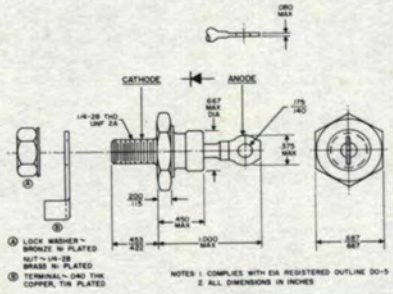
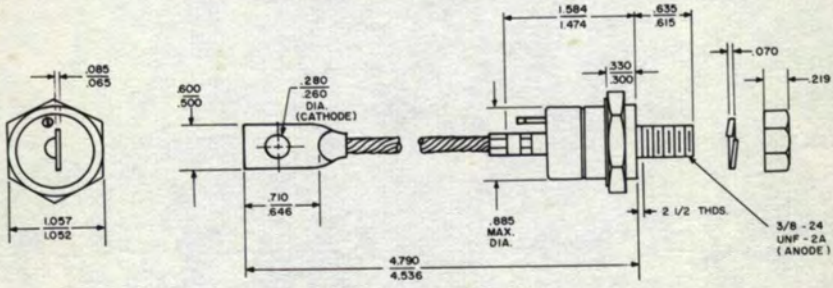


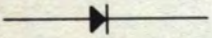
21

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW

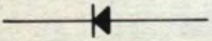


CONFORMS TO JEDEC OUTLINE DO-8

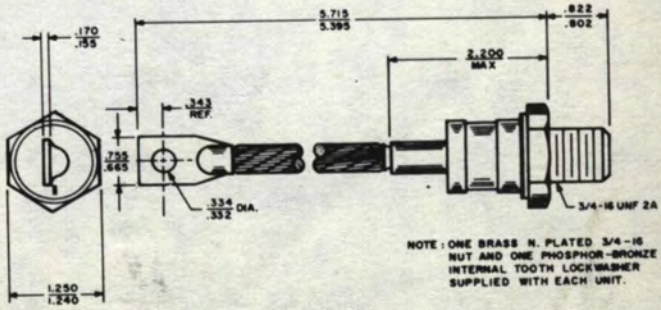
22



A90, IN3736 SERIES STUD CATHODE

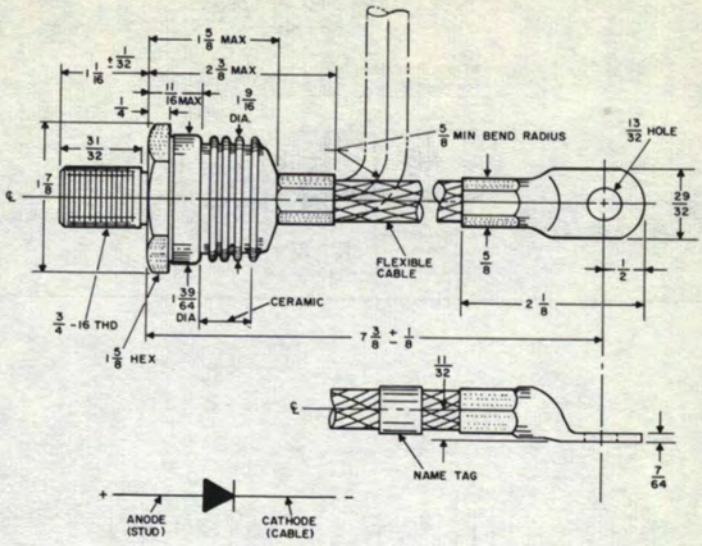


A91, IN3736R SERIES STUD ANODE



NOTE: ONE BRASS N. PLATED 3/4-16 NUT AND ONE PHOSPHOR-BRONZE INTERNAL TOOTH LOCKWASHER SUPPLIED WITH EACH UNIT.

23



Application and Specification Literature; Sales Offices

General Electric rectifier and SCR Application Notes and Specification Sheets provide greater detail on the application data and device specifications in this Manual. Copies of the literature listed in Sections 21.1 and 21.2 may be ordered by Publication Number from:

General Electric Co.,
Section SCRM
W. Genesee St.
Auburn, N. Y.

Section 21.4 lists other General Electric departments furnishing related electrical and electronic components.

21.1 APPLICATION NOTES

Publication 200.0, "Abstracts of Application Notes," contains content descriptions of the individual titles listed below.

21.1.1 General Applications of Semiconductor Rectifiers and Silicon Controlled Rectifiers

Publication Number	Title
200.2	Rectifier Selection Chart
200.3	Controlled Rectifiers and Radio Interference
200.5	General Electric Selenium Thyrector Diodes
200.8	Accommodating Inrush Currents with Silicon Controlled Rectifiers
200.9	Power Semiconductor Ratings Under Transient and Intermittent Loads
200.10	Overcurrent Protection of Semiconductor Rectifiers
200.11	Rectifier Voltage Transients: Their Generation, Detection and Reduction
200.12	Heatsinks for Stud-Mounted Semiconductors
200.13	Thermal Fatigue and the G-E 1N2154-60 Medium Current Silicon Rectifier
200.19	Using Low Current Silicon Controlled Rectifiers and Silicon Controlled Switches
200.20	Notes on the Application of the G-E 1N3289 Series (4JA70) High Current Rectifier (50-100 Amps)
200.23	PNPN Switches with Gate Turn-off Control (Using the ZJ224 Gate Turn-Off Switch)
200.27	An Introduction to the Controlled Avalanche Silicon Rectifier

200.28	The Rating of SCR's when Switching into High Currents
200.30	Capacitor Input Filter Design with Silicon Rectifier Diodes
200.32	A Variety of Mounting Techniques for Press-Fit SCR's and Rectifiers
R-105F	Suggested Fuses for Short Circuit Protection of G-E Power Semiconductor Components
660.1	Silicon Controlled Rectifiers—Interview With E. E. Von Zastrow
660.2	Rectifiers in High Voltage Power Supplies
660.3	Rating and Application of Germanium and Silicon Rectifiers
660.4	An Up-to-Date Look at Power Semiconductor Load Current Ratings
660.6	Overcoming Turn-on Effects in Silicon Controlled Rectifiers

21.1.2 Rectifier and SCR Circuits

Publication Number	Title
200.1	Characteristics of Common Rectifier Circuits
200.4	Universal Motor Speed Controls
200.6	Silicon Controlled Rectifier High Voltage Power Supply
200.14	The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service
200.18	Fluorescent Lamp Dimming with SCR's and Associated Semiconductors
200.21	Three Phase SCR Firing Circuits for DC Power Supplies
200.22	Voltage Stabilizer Using Silicon Controlled Rectifiers
200.24	An SCR Circuit to Produce High-Frequency Power
200.25	A Full-wave, Speed-Regulating Shunt Wound DC Motor Control
200.26	Simple and Low Cost SCR Trigger Circuits for AC Phase Control
200.31	Phase Control of SCR's with Transformer and Other Inductive AC Loads
200.33	Regulated Battery Chargers Using the Silicon Controlled Rectifiers
201.1	A Plug-In Speed Control for Standard Portable Tools and Appliances
201.2	An All Silicon Semiconductor Output Voltage Regulating Technique for Alternators
201.4	200 Volt to 24 Volt DC Converter
61-718	A Silicon Controlled Rectifier Inverter with Improved Commutation
660.5	Semiconductor Dimmers in Architectural Lighting

21.1.3 Test Circuits

Publication Number	Title
200.15	Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers
200.16	A Portable Transient Voltage Indicator for Semiconductor Circuits
200.17	Test Circuits for Silicon and Germanium Rectifiers
201.3	Portable SCR and Silicon Rectifier Tester

21.2 SPECIFICATION SHEETS

SCR Low Current

C5 (2N2322-29)	150.10
C7 (2N2344-48)	150.11
C8 (2N1929-35)	150.12
C10 (2N1770A-77A)	150.20
C11 (2N1770-78; 2N2619)	150.21
C12	150.25
C20, C22	150.30
G5, G6	150.60

SCR Medium Current

C30	160.27
C35 (2N681-92)	160.20
C36 (2N1842-50)	160.21
C38	160.30
C40	160.25

SCR High Current

C45	170.17
C46	170.17
C50 (2N1909-16)	170.20
C52	170.20
C55	170.21
C60 (2N2023-29)	170.26
C80	170.50
2N1792-98	170.20
6RW71	170.60

SCR Combination Stacks

C1012-13, C1112-13, C1212-13	195.10
C3512-13, C4012-13	and 195.10.1
C5014, C6014	170.40

Light Activated Devices

L8, L9	190.10

21.3 GENERAL ELECTRIC ELECTRONIC COMPONENTS DIVISION SALES OFFICES

All products of the Rectifier Components, Semiconductor Products, and Tube Departments are sold through these O.E.M. Sales Offices. Also, G.E. Authorized Semiconductor Distributors are generally listed in the classified section of local telephone directories.

Ala.: Huntsville
3322 Memorial Parkway S.
205-881-1640 (Direct Military Sales)

Calif.: Los Angeles 64
11840 W. Olympic Blvd.
213-GR9-7763 & 213-BR2-8566

San Diego 12
121 Broadway St.
714-BE3-1329

San Francisco (Palo Alto 5)
701 Welch Road
415-DA1-6771

Colo.: Denver 17
201 University Blvd.
P.O. Box 2331
303-DU8-5771

Conn.: Bridgeport
1285 Boston Ave., 21 ES
203-ED4-1012

Fla.: Orlando
14 W. Gore St.
305-GA4-6280 (Tubes) & 305-CH1-2991 (Semiconductors)

Ill.: Chicago 41
3800 N. Milwaukee Ave.
312-SP7-1600

Ind.: Indianapolis 32
3750 N. Meridian St.
317-WA3-7221

Ky.: Owensboro
316 E. 9th St.
502-MU3-2401 (Tubes)

Mass.: Boston (Newtonville)
701 Washington St.
617-WO9-9420 (Tubes) & 617-WO9-9422 (Tubes) & 617-DE2-7120 (Semiconductors)

Mich.: Detroit (Southfield)
17220 W. Eight Mile Rd.
313-EL6-1075

N. Y.: New York (Clifton, N. J., 200 Main Ave., 201-GR2-8100)
Dial direct from New York City: WIsconsin 7-4065

Garden City 14
600 Old Country Road
516-PI1-4710 (Semiconductors)

Schenectady 5
Bldg. 267
518-FR4-2211, Ext. 5-3433 (Tubes)

Syracuse 12,
Bldg. 7, Room 320
Electronics Park
315-652-5102 (Tubes), 315-456-2062 (Semiconductors)

Syracuse 12,
Bldg. 6, Electronics Park
315-456-2562 & 315-456-2538 (Tubes)

Ohio: Cleveland 14
2111 S. Green Road
216-EV2-5650

Dayton 2
118 W. First St.
513-BA3-7151 (Direct Military Sales)

Pa.: Philadelphia (Bala Cynwyd)
1 Belmont Ave., Room 1103
215-TE9-6075 (Semiconductors) & 215-TE9-6215 (Tubes)

Tex.: Dallas 75205
4447 N. Central Expressway
Room 480
214-LA6-0426 (Semiconductors)

Dallas 22
8101 Stemmons Freeway,
Box 5821
214-ME1-3110 (Tubes)

Minn.: Minneapolis
7710 Computer Ave.
612-927-5456

N. J.: Clifton (New York City)
200 Main Ave.
201-GR2-8100 (Dial direct from New York City—WI7-4065)

Red Bank
43 W. Front St.
201-SH1-8484 (Direct Military Sales)

Va.: Lynchburg
P.O. Box 4217, Carroll Ave.
703-VI7-5504

Wash.: Seattle 17
220 S. Dawson St.
206-PA5-6800

Wash.: 25, D. C.
777-14th St., N. W.
202-EX3-3600 (Direct Military Sales)

IN CANADA, address inquiries to: Canadian General Electric Co., 189 Dufferin St., Toronto, Ontario, Canada, 416-LE4-6316.

Inquiries from outside continental United States, excluding Hawaii and Alaska, should be sent to: Electronic Component Sales, International General Electric Co., 159 Madison Ave., New York 16, N. Y. 212-PL1-1311.

21.4 RELATED GENERAL ELECTRIC DEPARTMENTS

We would like to remind our readers of the great variety of parts and services that our sister departments in General Electric can furnish to meet your SCR circuit needs. Among them are:

—SCR Capacitors for phase control and inverter commutation duty (G-E Capacitor Dept., Hudson Falls, N. Y.)

—Transformers and chokes for inverters and power supply needs (G-E Specialty Transformer Dept., Fort Wayne, Ind.)

—A complete family of G-E Sensors and control elements:

- Cadmium sulfide cells and magnetic reed switches (G-E Tube Dept., Owensboro, Ky.)
- Thermistors and magnetic materials (G-E Metallurgical Products Dept., Edmore Mich.)
- Transistors, Unijunctions, signal diodes and silicon strain gages (G-E Semiconductor Products Dept., Syracuse, N. Y.)

—A complete family of high reliability lamps for activation of light activated SCR's.
(G-E Miniature Lamp Dept., Cleveland, Ohio)

—Silicone potting compounds and joint compounds
(G-E Silicone Products Department, Waterford, New York)

—And, of course, the industry's most complete line of motors and other related electrical and electronic equipment

APPLICATION INDEX

The circuits referred to in the following figure numbers are intended as a starting point for the equipment designer in achieving the detailed requirements of his application. Since these circuits are not necessarily "ultimate" for every application, it is hoped the imaginative designer will use them simply as a jumping-off point for his own development. Likewise, many of these circuits can be used for other functions besides those mentioned in the text. As a guide to some of the various SCR circuits for accomplishing specific tasks, here is a tabulation of figures in this manual classified by possible application (please note that these are *Figure* numbers and not section or paragraph numbers):

Applications	For Basic Circuit Possibilities See *Figure* Number
AC Regulated Supplies	4.15, 4.23, 4.24, 4.33, 8.1, 8.23, 8.24, 8.25, 8.27, 8.37, 8.38, 9.2.7, 9.3.7, 9.3.8, 9.3.10, 11.8
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